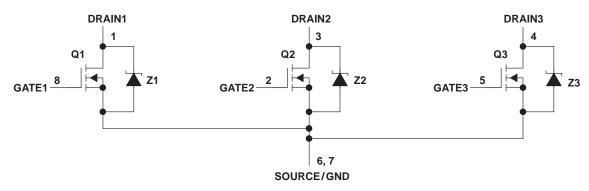
SLIS028B - APRIL 1994 - REVISED SEPTEMBER 1995

 Low r_{DS(on)}0.4 Ω Typ High-Voltage Outputs60 V 	D PACKAGE (TOP VIEW)
Pulsed Current 5 A Per Channel	
Fast Commutation Speed	GATE2 2 7 SOURCE/GND
	DRAIN2 🛛 3 🛛 6 🗍 SOURCE/GND
description	DRAIN3 🛛 4 5 🗍 GATE3
uescription	

The TPIC2302 is a monolithic power DMOS array that consists of three electrically isolated N-channel enhancement-mode DMOS transistors configured with a common source and open drains. The TPIC2302 is offered in a standard 8-pin small-outline surface-mount (D) package.

The TPIC2302 is characterized for operation over the case temperature range of -40°C to 125°C.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)[†]

Drain-to-source voltage, V _{DS}	
Gate-to-source voltage, V_{GS}	
Continuous drain current, each output, all outputs on, $T_C = 25^{\circ}C$	
Pulsed drain current, each output, $T_C = 25^{\circ}C$ (see Note 1 and Figure 6)	
Single-pulse avalanche energy, $T_C = 25^{\circ}C$, E_{AS} (see Figures 4 and 16)	
Continuous total power dissipation at (or below) $T_C = 25^{\circ}C$	0.95 W
Operating virtual junction temperature range, T _J	–40°C to 150°C
Operating case temperature range, T _C	–40°C to 125°C
Storage temperature range, T _{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

⁺ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



SLIS028B - APRIL 1994 - REVISED SEPTEMBER 1995

electrical characteristics, $T_C = 25^{\circ}C$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V(BR)DSX	Drain-to-source breakdown voltage	I _D = 250 μA,	$V_{GS} = 0$	60			V
V _{GS(th)}	Gate-to-source threshold voltage	I _D = 1 mA,	$V_{DS} = V_{GS}$	1.5	1.85	2.2	V
V _{DS(on)}	Drain-to-source on-state voltage	$I_D = 1 A$, See Notes 2 and 3	V _{GS} = 10 V,		0.4	0.475	V
VF(SD)	Forward on-state voltage, source-to-drain	$I_{S} = 1 A,$ $V_{GS} = 0 (Z1, Z2, Z3)$ See Notes 2 and 3	V _{GS} = 0 (Z1, Z2, Z3),		0.9	1.1	V
	Zero-gate-voltage drain current	V _{DS} = 48 V, V _{GS} = 0	T _C = 25°C		0.05	1	μΑ
IDSS			T _C = 125°C		0.5	10	
IGSSF	Forward gate current, drain short circuited to source	V _{GS} = 16 V,	$V_{DS} = 0$		10	100	nA
IGSSR	Reverse gate current, drain short circuited to source	V _{SG} = 16 V,	$V_{DS} = 0$		10	100	nA
	Leakage current, drain-to-GND	V _R = 48 V	$T_C = 25^{\circ}C$		0.05	1	μA
l _{lkg}			$T_{C} = 125^{\circ}C$		0.5	10	
	Chatta duais to commo en atoto registere en	V _{GS} = 10 V, I _D = 1 A,	$T_C = 25^{\circ}C$		0.4	0.475	0
rDS(on)	Static drain-to-source on-state resistance	See Notes 2 and 3 and Figures 6 and 7	$T_{C} = 125^{\circ}C$		0.63	0.7	Ω
9fs	Forward transconductance	V _{DS} = 10 V, See Notes 2 and 3	I _D = 0.5 A,	0.85	1.02		S
C _{iss}	Short-circuit input capacitance, common source				115	145	
C _{OSS}	Short-circuit output capacitance, common source	V _{DS} = 25 V,	$V_{GS} = 0,$		60	75	pF
C _{rss}	Short-circuit reverse-transfer capacitance, common source	f = 1 MHz			30	40	μr

NOTES: 2. Technique should limit T_J – T_C to 10°C maximum, pulse duration ${\leq}5$ ms.

3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, $T_C = 25^{\circ}C$

	PARAMETER	TEST CONDIT	MIN	TYP	MAX	UNIT	
t _{rr(SD)}	Reverse-recovery time	$I_{S} = 0.5 \text{ A}, V_{GS} = 0,$	V _{DS} = 48 V,		65		ns
Q _{RR}	Total diode charge	di/dt = 100 A/µs,	See Figure 1		0.03		μC



SLIS028B - APRIL 1994 - REVISED SEPTEMBER 1995

resistive-load switching characteristics, $T_C = 25^{\circ}C$

	PARAMETER	ר ا	EST CONDITIO	NS	MIN	TYP	MAX	UNIT
t _{d(on)}	Turn-on delay time					21	42	
^t d(off)	Turn-off delay time	V _{DD} = 25 V,		t _{r1} = 10 ns,		20	40	
t _{r2}	Rise time	t _{f1} = 10 ns,				5	10	ns
t _{f2}	Fall time					13	26	
Qg	Total gate charge					3.1	3.8	
Q _{gs(th)}	Threshold gate-to-source charge	V _{DS} = 48 V, See Figure 3	I _D = 0.5 A,	V _{GS} = 10 V,		0.4	0.5	nC
Q _{gd}	Gate-to-drain charge	eee rigare e				1.3	1.6	
LD	Internal drain inductance					5		
LS	Internal source inductance					5		nH
Rg	Internal gate resistance					0.25		Ω

thermal resistance

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with aqual power	See Note 4		130		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance	All outputs with equal power,	See Note 4		44		-C/ W

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink

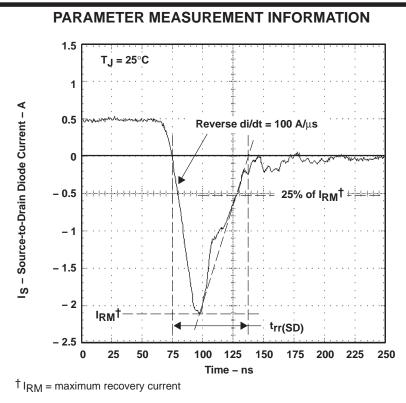
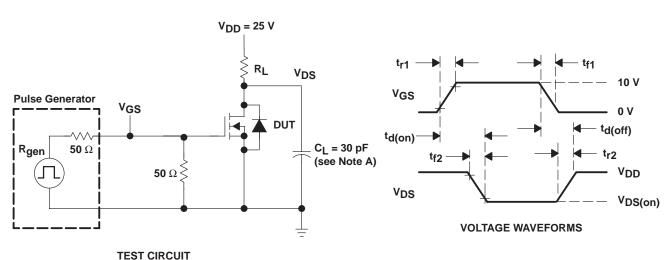


Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode



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PARAMETER MEASUREMENT INFORMATION

NOTE A: CL includes probe and jig capacitance.



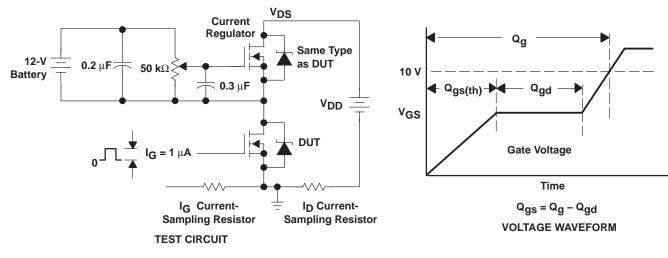
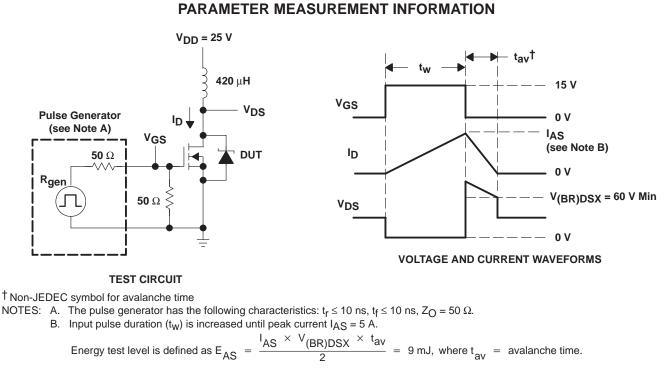


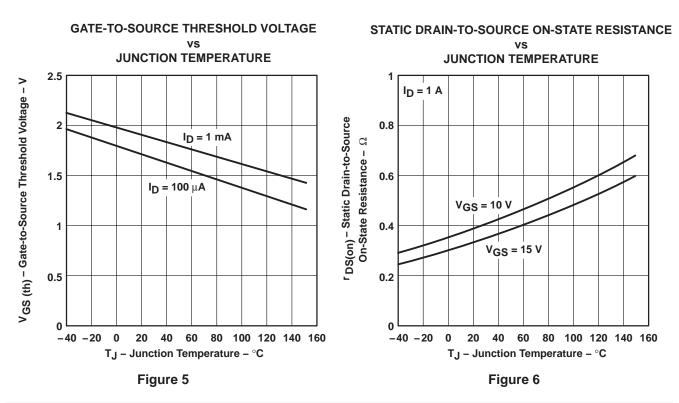
Figure 3. Gate-Charge Test Circuit and Voltage Waveform



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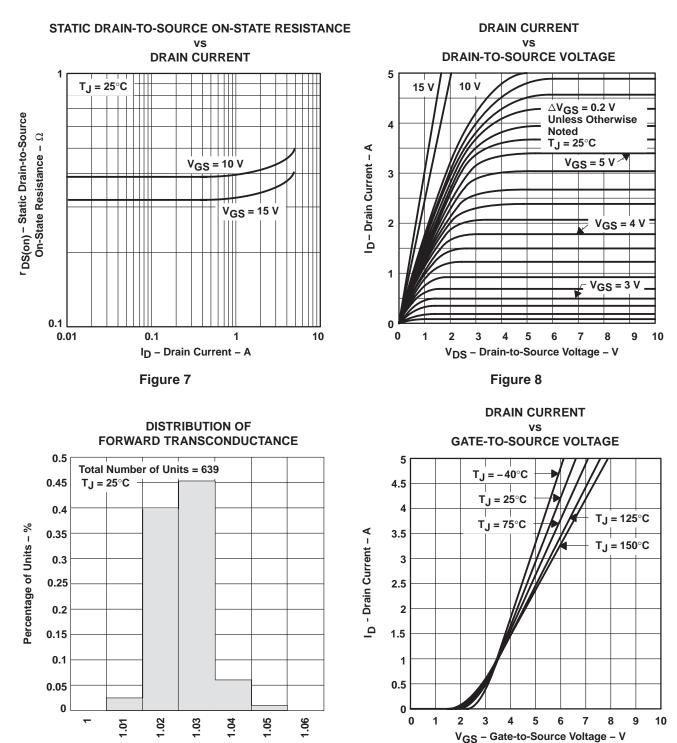




TYPICAL CHARACTERISTICS



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TYPICAL CHARACTERISTICS

Figure 9

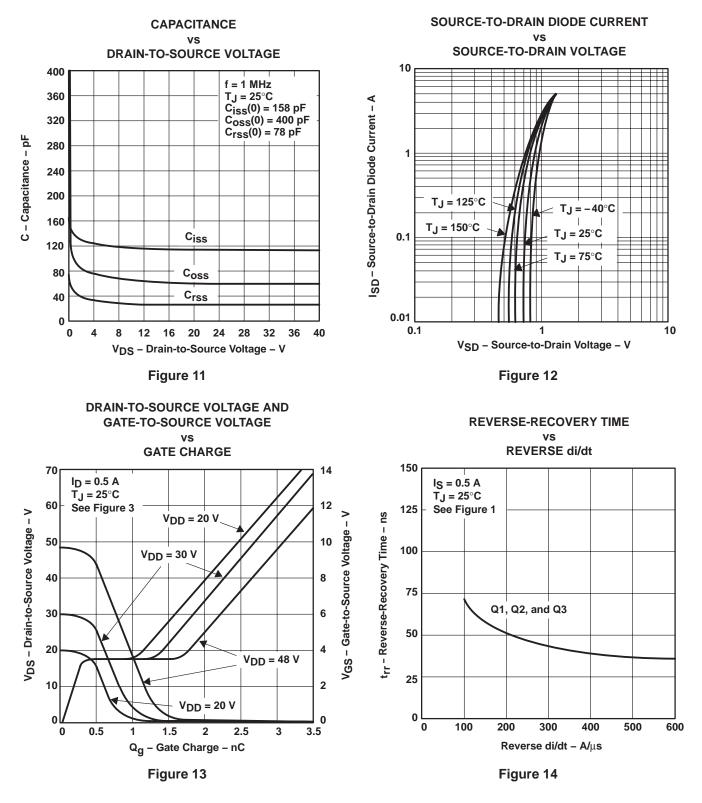
gfs - Forward Transconductance - S

Figure 10



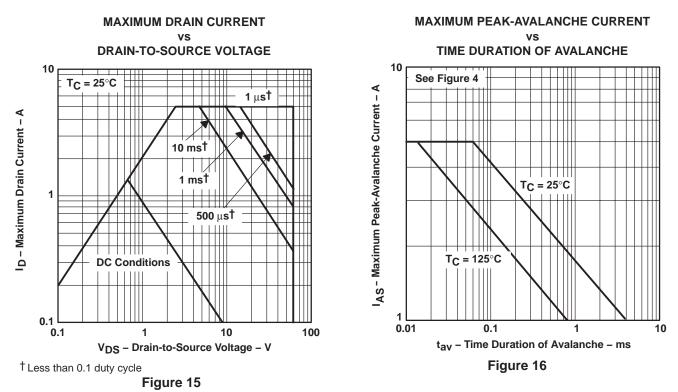
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TYPICAL CHARACTERISTICS





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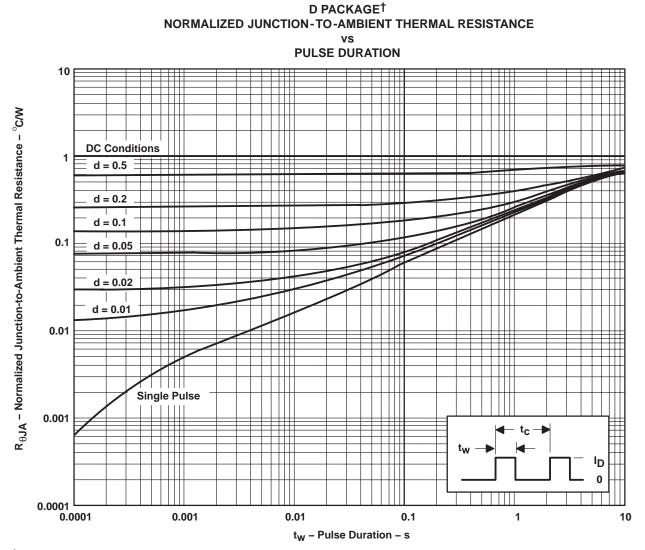


THERMAL INFORMATION



SLIS028B - APRIL 1994 - REVISED SEPTEMBER 1995

THERMAL INFORMATION



[†] Device mounted on FR4 printed-circuit board with no heat sink

NOTE A: $Z_{\Theta A}(t) = r(t) R_{\Theta JA}$ $t_W = pulse duration$

 t_{c} = cycle time d = duty cycle = t_{W}/t_{c}

Figure 17



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPIC2302D	OBSOLETE	SOIC	D	8	TBD	Call TI	Call TI
TPIC2302DR	OBSOLETE	SOIC	D	8	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



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