# Medium-End PIC Microcontroller Instruction Set

| Mnemonic | | Operation | Affects | Cycles |
|---|---|---|---|---|
| *1. Data Transfer* | | | | |
| movf | f, d | f = > d | Z | 1 |
| movwf | f | W = >f | — | 1 |
| movlw | k | k = >W | — | 1 |
| clrf | f | 0 = >f | Z | 1 |
| clrw | | 0 = >W | Z | 1 |
| *2. Arithmetic and Logic* | | | | |
| addwf | f, d | f + W = > d | C, DC, Z | 1 |
| addlw | k | k + W = > W | C, DC, Z | 1 |
| subwf | f, d | f – W = > d | C, DC, Z | 1 |
| sublw | k | k – W = > W | C, DC, Z | 1 |
| incf | f, d | f + 1 = > d | Z | 1 |
| decf | f, d | f – 1 = > d | Z | 1 |
| andwf | f, d | f and W = > d | Z | 1 |
| andlw | k | k and W = > W | Z | 1 |
| iorwf | f, d | f or W = > d | Z | 1 |
| iorlw | k | k or W = > W | Z | 1 |
| xorwf | f, d | f xor W= > d | Z | 1 |
| xorlw | k | k xor W = > W | Z | 1 |
| rlf | f, d | rotate f left through C = > d | C | 1 |
| rrf | f, d | rotate f right through C = >d | C | 1 |
| comf | f, d | #f = > d | Z | 1 |
| swapf | f, d | $f_L \leftrightarrow f_H$ = > d | — | 1 |
| *3. Control Transfer* | | | | |
| goto | a | branch to address | — | 2 |
| btfsc | f, b | branch if f<b> = 0 | — | 1(2) |
| btfss | f, b | branch iff<b> = 1 | — | 1(2) |
| incfsz | f, d | f + 1 = > d, branch if 0 | — | 1(2) |
| decfsz | f, d | f - 1 = > d, branch if 0 | — | 1(2) |
| call | a | call subroutine in address a | — | 2 |
| return | | subroutine return | — | 2 |
| retfie | | interrupt return | — | 2 |
| retlw | k | return from subroutine with k in W | — | 2 |
| *4. Bit Manipulation* | | | | |
| bcf | f, b | 0 = > f<b> | — | 1 |
| bsf | f, b | 1 = > f<b> | — | 1 |
| *5. Other* | | | | |
| nop | | no operation | — | 1 |
| clrwdt | | 0 = > WDT | TO#, PD# | 1 |
| sleep | | go to low power consumption | TO#, PD# | 1 |

*Note:* W, working register; f, data memory register; k, 8-bit constant; a, 11-bit constant; b, bit; d, destination as follows: If d = 0 destination is W and if d = 1 destination is f. C, DC, Z, TO#, and PD 3 are specific bits within the STATUS register.