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Microprocessor-based system for identification of phase sequence and detection of phase unbalance of three-phase ac supply

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A prototype detection system based on 8085 microprocessor / 8751 microcontroller has been developed for identification of phase sequence and detection of phase unbalance. System principle compares self-generating code by hardware circuit with pre-defined specific codes corresponding to positive and negative sequences for successful match in each measuring cycle. System is also capable in detecting phase unbalance, if any. Rule based intricate software algorithm is developed and operates within a cycle. Processor generates signals for detecting phase sequence and phase unbalance up to a recommended value.

Keywords: Microprocessor-based system, Phase sequence, Phase unbalance

Introduction

Identification of phase sequence and detection of phase unbalance for a three phase ac power supply system is an important routine test during installation and commissioning of three phase ac motors and parallel operation of three phase transformers. For identification of phase sequence and detection of phase unbalance, conventional microprocessor / microcontroller based systems operate on induction principle[1-2]. Digital / microprocessor based methods[3] determine sequence of zero crossing instants of three phases[4-7]. This paper presents a new microprocessor 8085 / microcontroller 8751 based detection system for identification of phase sequence and detection of phase unbalance for a three phase ac power supply.

Experimental

Hardware Design

In proposed system (Fig. 1), primary sides of three 230 / 6 volt potential transformers (PTs) are connected with individual phase and neutral of three-phase ac supply. Scaled down sinusoidal voltage signals from secondary side of each PT are fed into three isolated zero crossing detectors (ZCDs). On receiving signal, ZCD emits a series of unipolar rectangular wave signals, in which positive half cycle of sinusoidal voltage signal is converted to rectangular pulse of +5 volt with constant amplitude and negative half cycle is suppressed to 0 volt. Rectangular waves are mutually apart in phase angle of 120° or $2\pi/3$ radian with respect to each other having equal time period (20 ms for 50 Hz supply system). Periodical occurrence of leading edge of each rectangular wave at different time instants for positive and negative phase sequences is generated by ZCDs.

Three rectangular wave signals (R', Y' and B') generated by three ZCDs are applied to three monostable multivibrators (MVs) for triggering at leading edge of rectangular wave signal (Fig. 2). However at each triggering instant MV generates a monoshot pulse of narrow width (1 μ s). Outputs (R*, Y* and B*) obtained from three monoshot circuits are combined through logical OR gate to produce a unique single narrow pulse. During occurrence of rising edge of sinusoidal voltage signal of any phase, OR gate produces a monoshot pulse and output from OR gate has been utilized to activate the interrupt of microprocessor 8085 / microcontroller 8751. Output signals (R', Y' and B') from three ZCDs are fed to three input port lines (P0, P1 and P2) of microprocessor / microcontroller[8-9]. Three output port lines (P3, P4 and P5) are connected with three LED circuits, L1, L2 and L3, respectively.

Embedded Software Design

In proposed system, software algorithm (Appendix – A) performs following functions: i) Detection of zero crossing instants of rising edge of positive half

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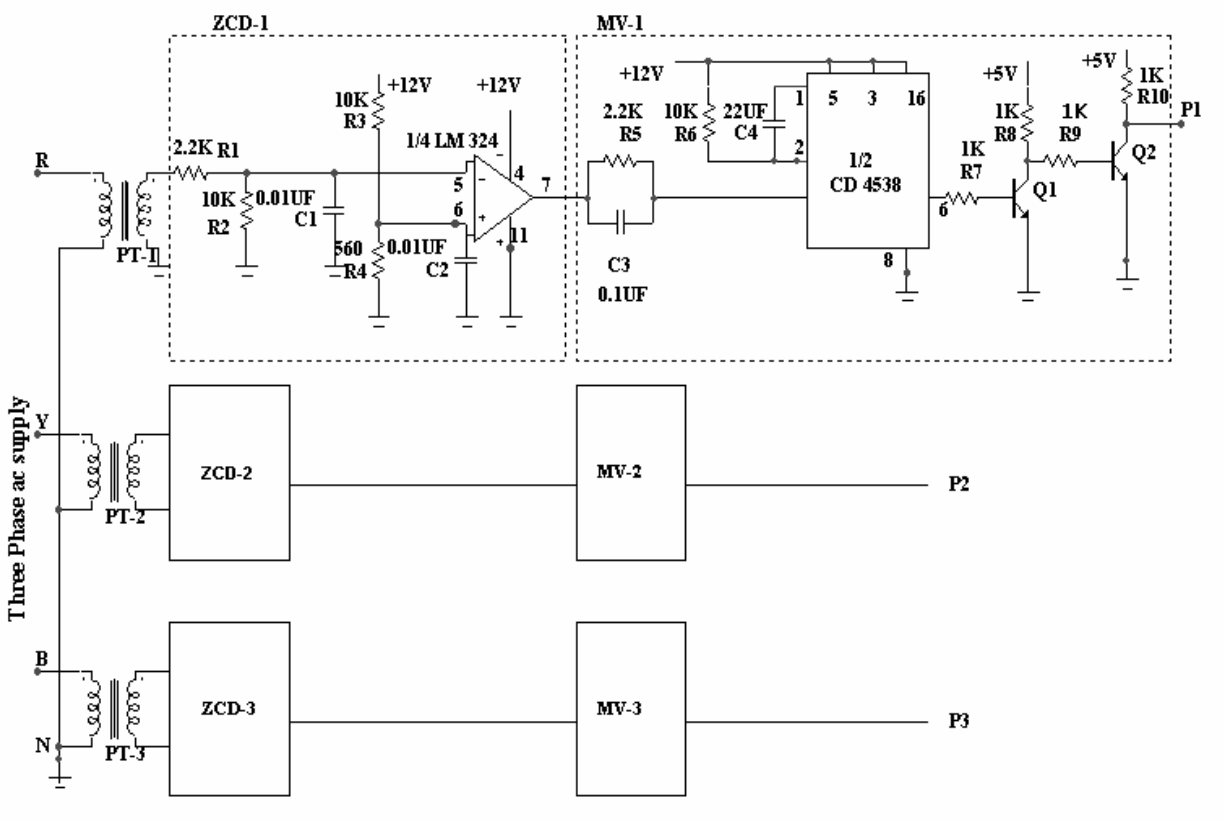


Fig. 1—Circuit design of developed system

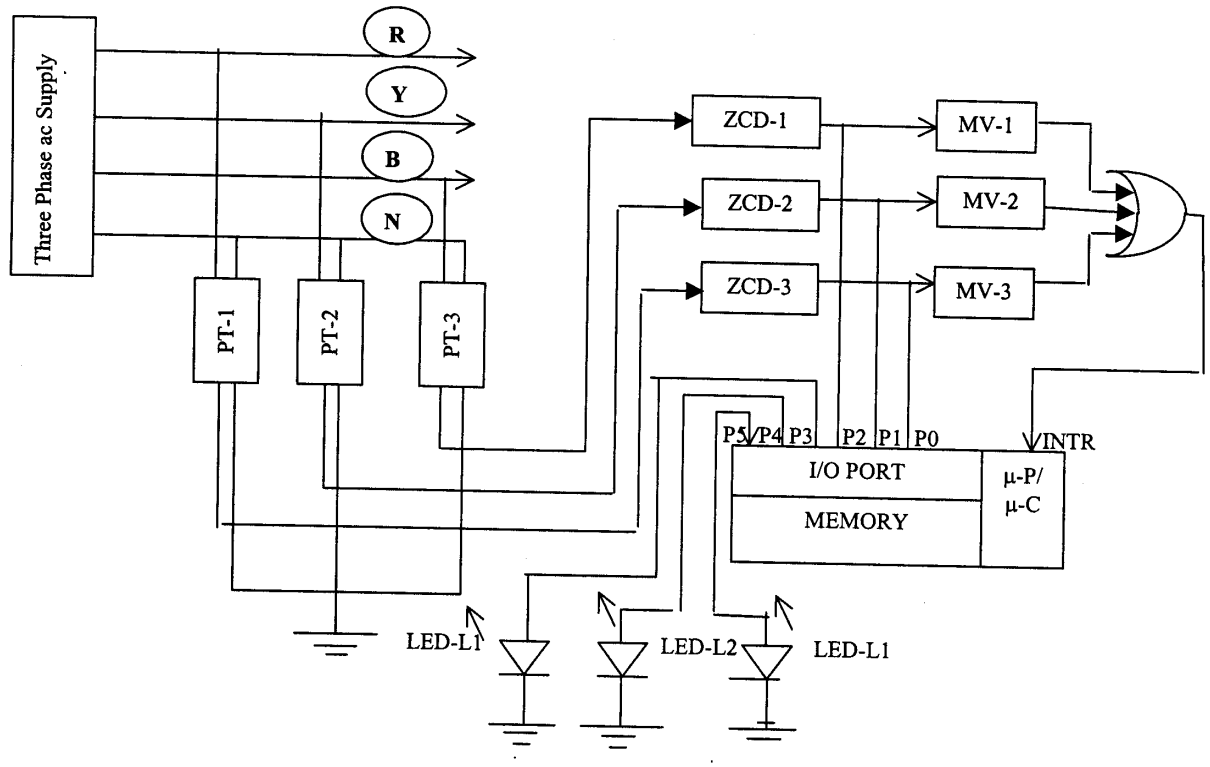


Fig. 2—Schematic diagram of developed system

cycle of three phases and generation of 8-bit binary code corresponding to sequence of appearance of self generated three 3-bit binary code corresponding to three phase signals with either positive or negative sequence; ii) Measurement of time count corresponding to positive half cycle of each of three phase signals and computation of two differential time counts between first and second zero crossing time instants and second and third zero crossing time instants; iii) Comparison of 8-bit code with pre-assigned elements of array code tables stored in the system memory for detection of phase sequence and checking for equality condition of pre-assigned time counts proportional to phase differences in two consecutive phases of three phase ac signals; and iv) Generation of signals for indicating positive or negative phase sequence and any phase unbalance.

Algorithm of software can be divided into two parts [Main program and Interrupt Service Subroutine (ISS)]. Microprocessor / microcontroller initializes all timer variables (T1, T2 and T3) with zero values. Three variables (TFLAG1, TFLAG2 and TFLAG3) are used as timer status variables for controlling operation of three software timers. Initially, these variables are set to enable timers at beginning of measuring cycle. Variable TCODE is used to store 3-bit binary code, which is generated at the occurrence of next timing instants of leading edge of rectangular wave signals (R*, Y* and B*). Variable CODE is used to store 8-bit code generated at the end of measuring cycle. Variable SCODE is used to store cumulative sum of the content in variable TCODE in a given measuring cycle.

For any phase sequence [R-Y-B (Fig. 3) or R-B-Y (Fig. 4)], only three possible combinations of 3-bit code (110, 101 and 011) may occur in sequence with six possible permutations [a) for positive sequence: i) 101, 110, 011; ii) 110, 011, 101; iii) 011, 101, 110; and b) for negative sequence: 110, 101, 011; ii) 101, 011, 110; iii) 011, 110, 101]. In occurrence of any one of the above possible permutations, sequence terminates with generation of next 3-bit code, which is identical with first 3-bit code in a given sequence. In any possible combination, sum of three 3-bit codes for any sequence is always $0E_H$. Variable SCODE is used to store this sum at the end of measuring cycle. FLAG is used by main program for detecting occurrence of leading edge generated by narrow positive pulse by three mono shot circuits (MV-1, MV-2 and MV-3). These leading edge may occur at positive zero crossing instant of three phase ac signals R, Y and B, respectively. In this program, variable FLAG is reset to zero initially. After entering into measuring cycle (FLAG = 0), processor goes on incrementing timer variables (T1, T2 and T3) as software counters as long as timer status variables (TFLAG1, TFLAG2 and TFLAG3) are all reset to zero.

Occurrence of leading edge of any one of three rectangular wave signals (R', Y' and B') will result a narrow pulse (duration, 1 μ s) through mono shot circuits, producing interrupt request signal input to RST-7.5 for microprocessor 8085 or INTR for microcontroller 8751. Interrupt request signal activates ISS, which sets variable FLAG to 1 so as to give signal to main program regarding generation of 3-bit code. ISS also saves code into variable TCODE via input port lines (P0, P1 and P2). Main program concatenates 3-bit codes serially, which is generated in a given sequence and also stores resultant code in variable CODE. Cumulative sum of all 3-bit codes in a given sequence is also computed and stored into variable SCODE. In each time, 3-bit code is generated at intermediate stage of given sequence. Variable FLAG is reset to zero. One of the three timer status variables (TFLAG1, TFLAG2 and TFLAG3) is reset to zero depending on the value of generated 3-bit code in variable TCODE so that incremental value of content of appropriate timer variable (T1, T2 and T3) ceases. While comparing content of variable SCODE with $0E_H$, processor exit from measuring cycle and disables interrupt system. In subsequent phase of algorithm, content of variable CODE is compared with all elements of two array code tables [TABLE1 (I) and TABLE2 (I) (I = 1, 2, 3)] for successful match. TABLE1 (I) refers to three 3-bit codes (73_H, $9D_H$, EF_H) for positive sequence case and TABLE2 (I) to 3-bit code (AB_H, $5E_H$, $F5_H$) for negative sequence case. Accordingly, variable SEQ is set to 1 for negative sequence case or reset to 0 for positive sequence case.

Phase unbalance is detected by comparing relative counts stored in two variables (PH1 and PH2). These relative counts are proportional to two-phase angle differences among R-Y, Y-B and B-R signal pairs in case of positive sequence and R-B, B-Y and Y-R signal pairs in case of negative sequence. According to wave forms of R*, Y* and B* signals for both positive and negative sequences in timing diagram, software has been developed to compute count values for PH1 and PH2 from count values stored into timer variables (T1, T2 and T3) by following a set of rules given as:

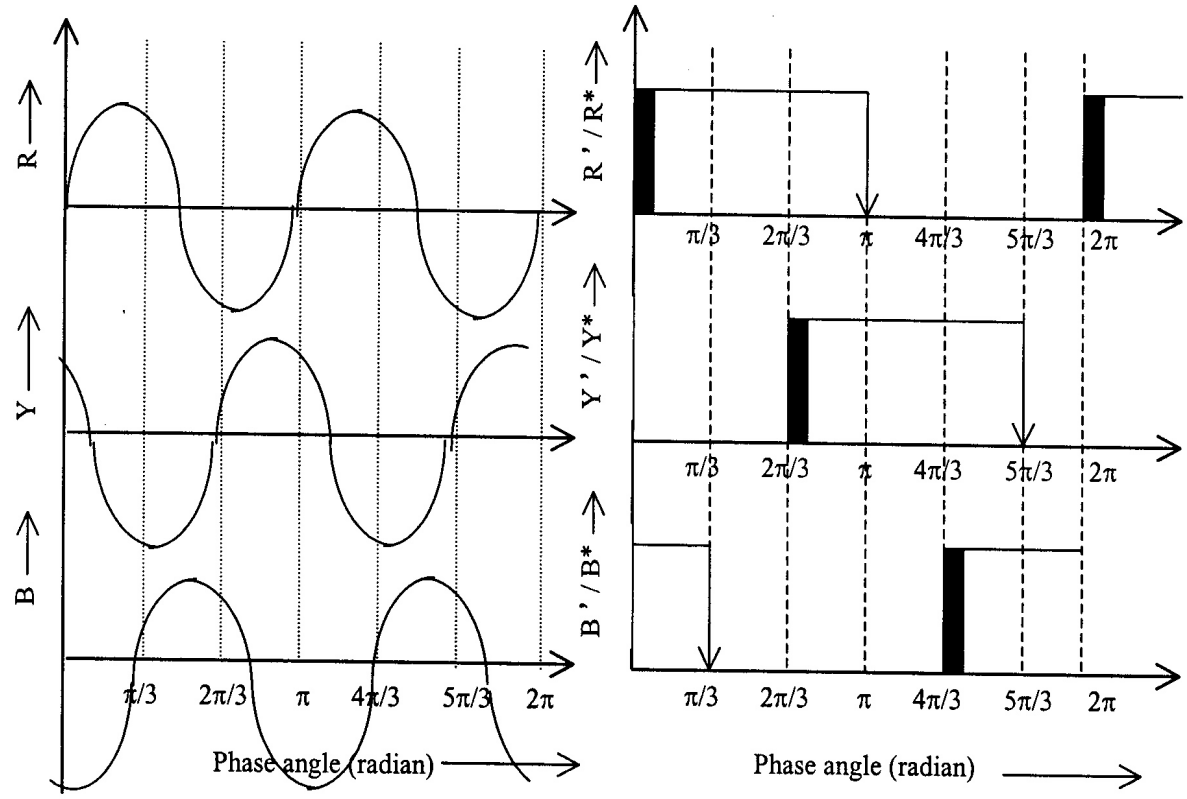


Fig. 3-Timing waveform of three ac signals, ZCD outputs and monoshot outputs at positive (R-Y-B) sequence

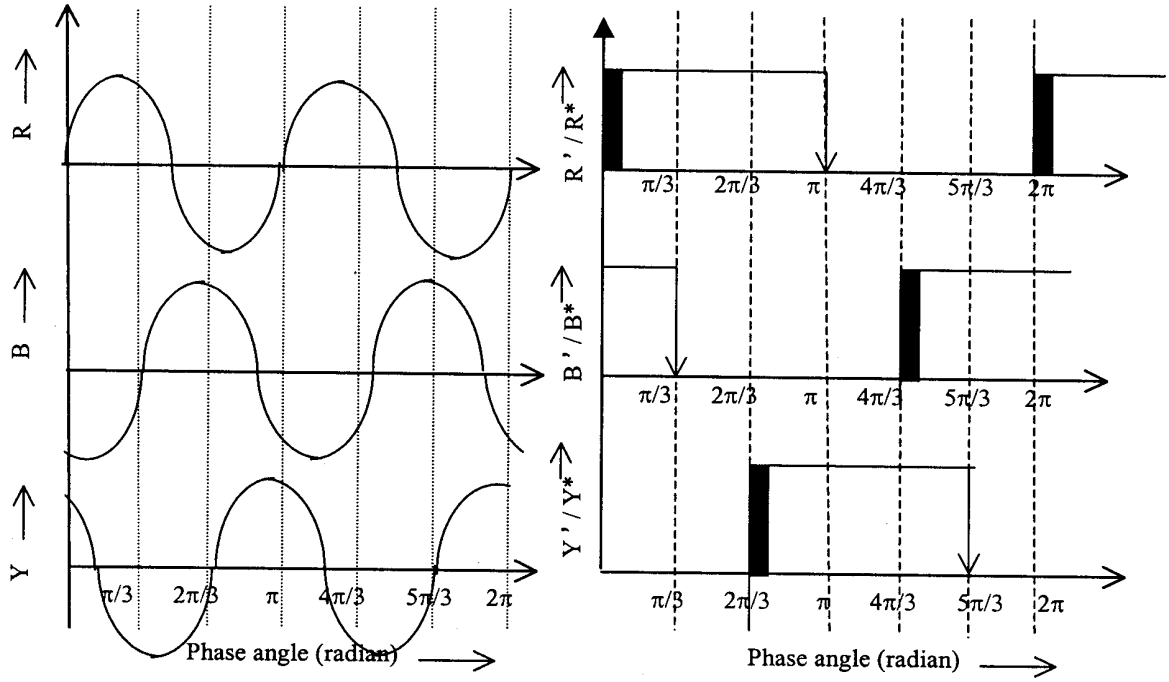
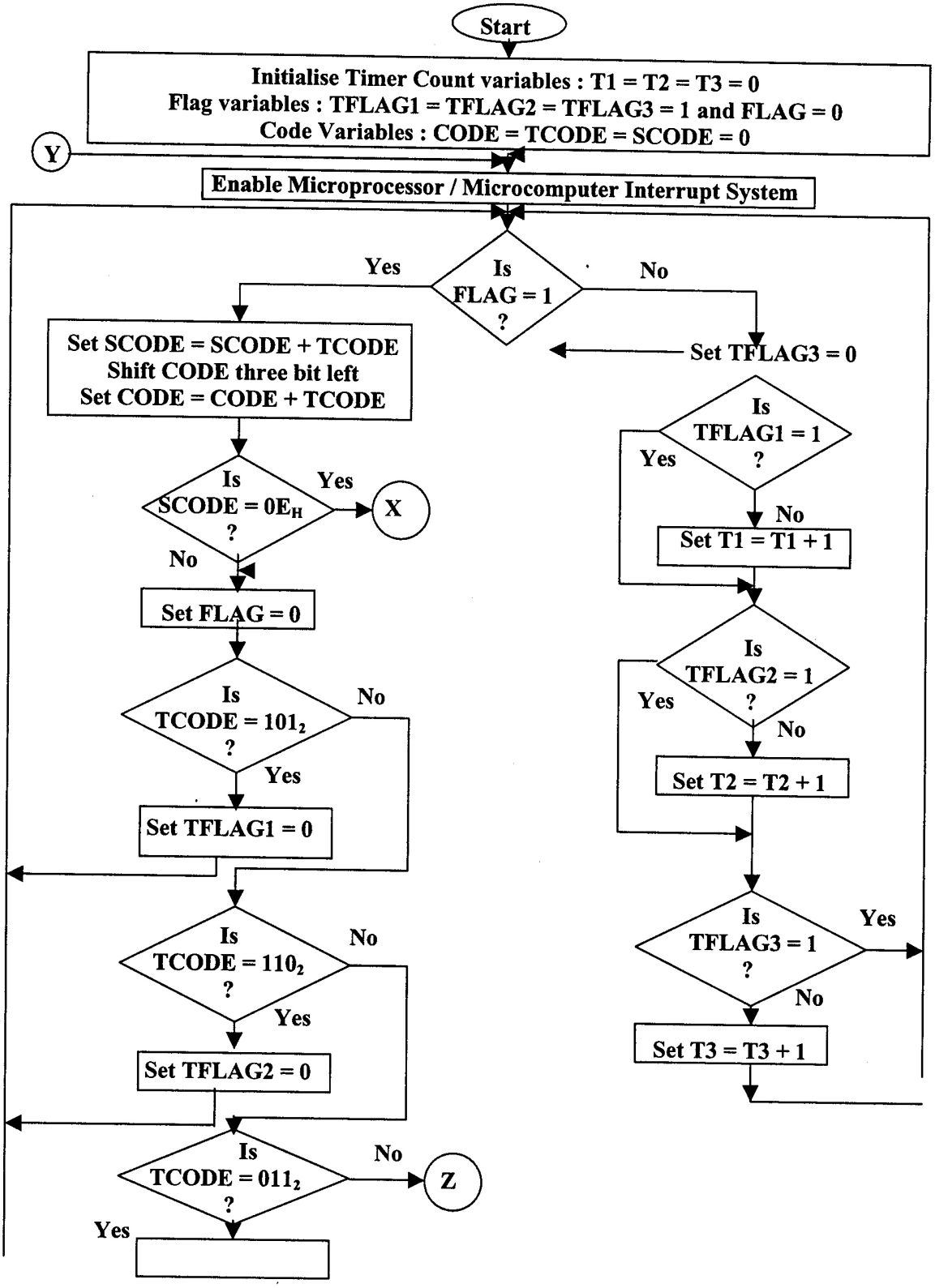
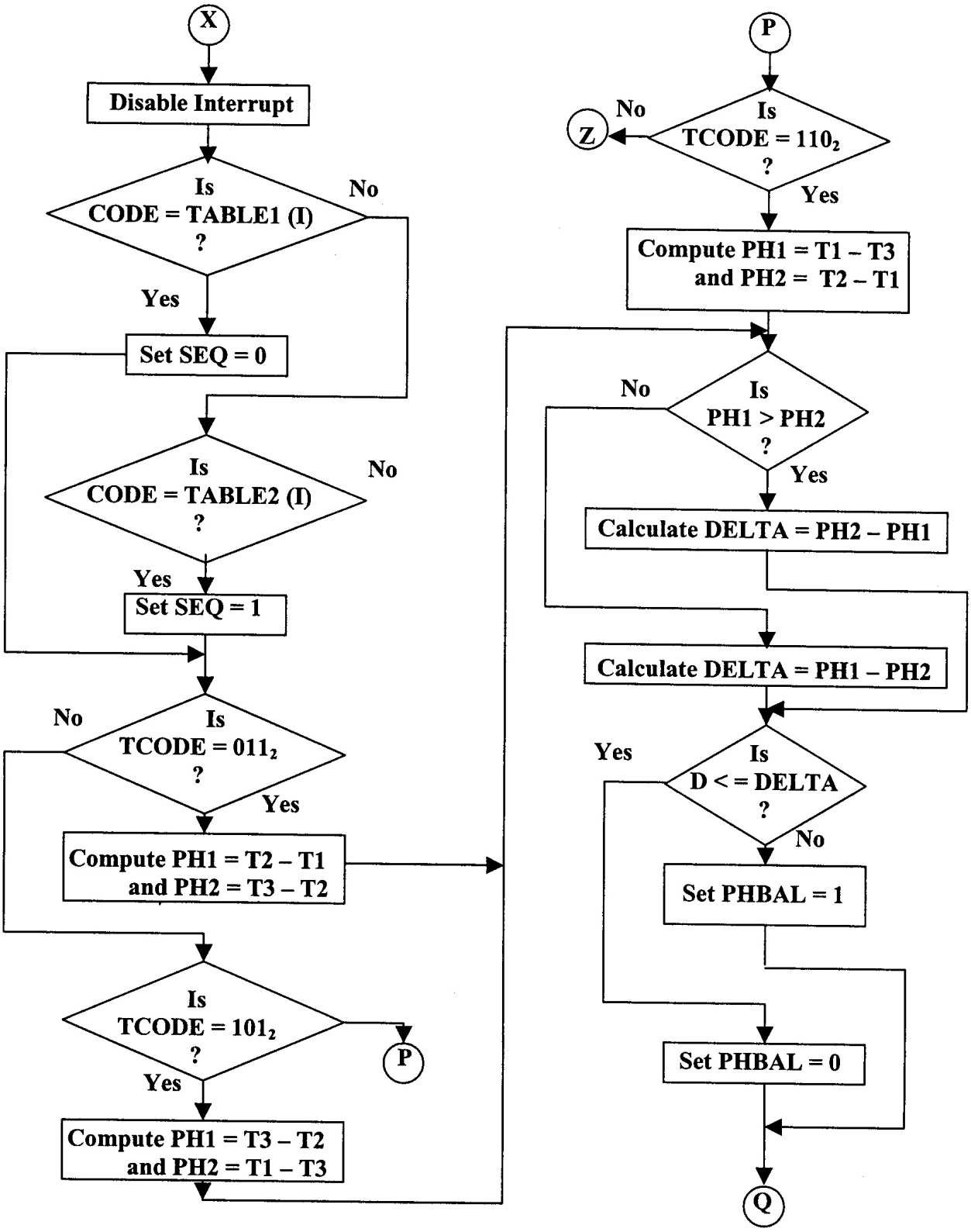


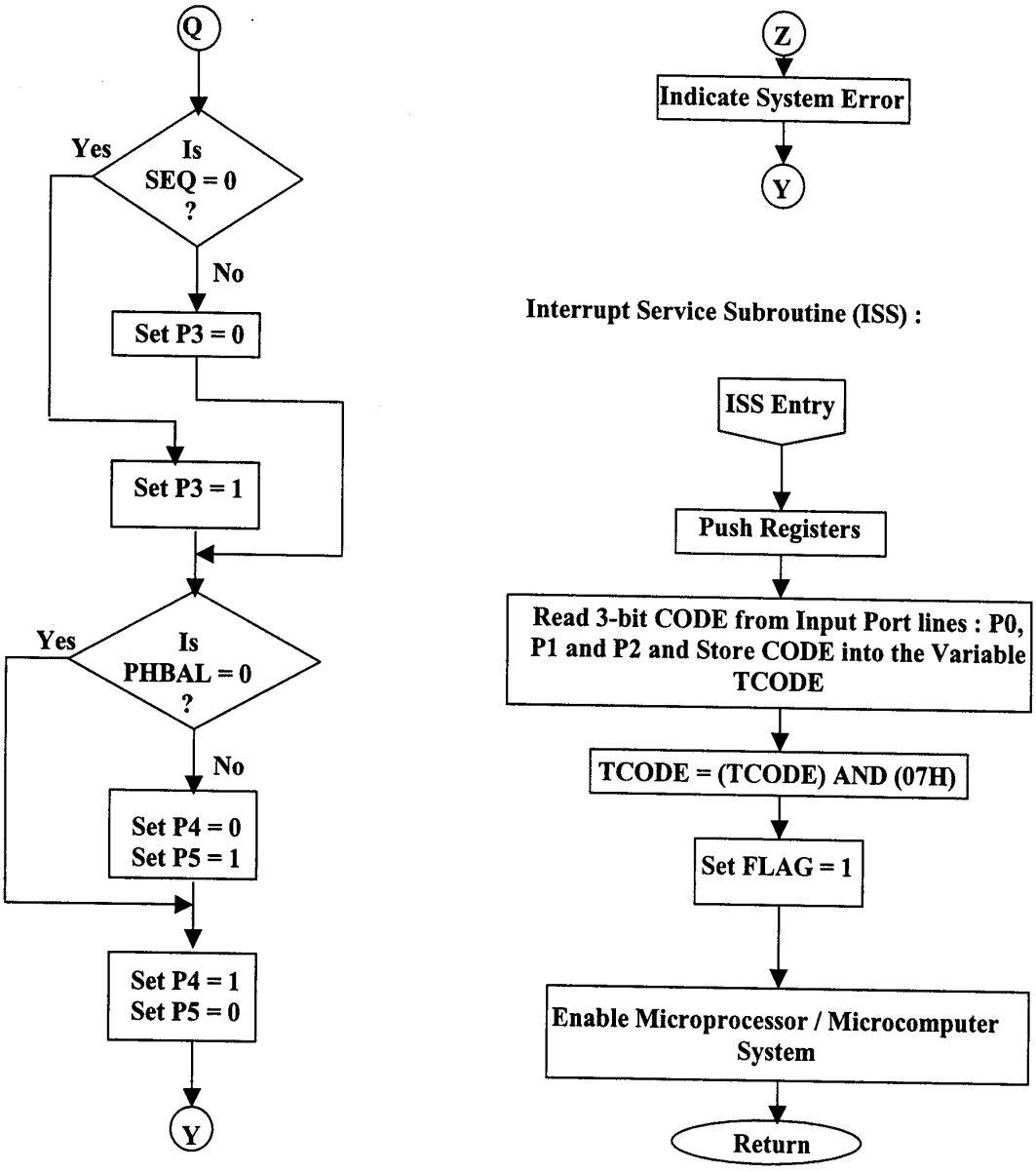
Fig. 4-Timing waveform of three ac signals, ZCD outputs and monoshot outputs at negative (R-B-Y) sequence

Appendix – A

Flow diagram




X
Disable Interrupt
Is CODE = TABLE1 (I) ?
No
Yes
Set SEQ = 0
Is CODE = TABLE2 (I) ?
No
Yes
Set SEQ = 1
Is TCODE = 011₂ ?
No
Yes
Compute PH1 = T2 – T1 and PH2 = T3 – T2
Is TCODE = 101₂ ?
P
Yes
Compute PH1 = T3 – T2 and PH2 = T1 – T3
P
Is TCODE = 110₂ ?
No
Z
Yes
Compute PH1 = T1 – T3 and PH2 = T2 – T1
Is PH1 > PH2 ?
No
Yes
Calculate DELTA = PH2 – PH1
Calculate DELTA = PH1 – PH2
Is D < = DELTA ?
Yes
No
Set PHBAL = 1
Set PHBAL = 0
Q



If <(TCODE) = 011> *Then* <PH1 = T2-T1; PH2=T3-T2>

If <(TCODE) = 101> *Then* <PH1 = T3-T2; PH2=T1-T3>

If <(TCODE) = 110> *Then* <PH1 = T1-T3; PH2=T2-T1>

Subsequently, contents of PH1 and PH2 are compared. If difference of contents of these variables as PH1 and PH2 falls below or equal to the small tolerance count value as specified during calibration of the system, variable PHBAL is reset to 0 otherwise set to 1 indicating balance or unbalance condition of three phase system. On completing loop containing measurement of time intervals and data processing tasks, control in main program returns at the point of initialization of variables for detection of phase sequence and phase unbalance in next cycle.

Results

A detailed study on waveforms shows that in balanced condition of three phase supply system, measured time intervals between zero crossing instants of pairs of sinusoidal phase voltages with either sequences [R-Y-B (Fig. 3) or R-B-Y(Fig. 4)] designated as T_{RY}, T_{YB} and T_{BR} are exactly or very nearly equal to each other. Rectangular waveforms from three ZCDs may be used to form a 3-bit binary code, in which Bit-0, Bit-1 and Bit-2 carry information contained in R, Y and B phases

respectively. Proposed microprocessor based detection system has been found to generate unique codes for different probable permutations for supply system. This system can identify phase sequence during fluctuation of power frequency within recommended value.

Conclusions

A prototype detection system based on 8085 microprocessor / 8751 microcontroller has been developed for identification of phase sequence and detection of phase unbalance. Proposed microprocessor based detection system can generate unique codes for different probable permutations for supply system. System is capable to identify phase sequence of three phase supply system and can identify phase sequence during fluctuation of power frequency within recommended value. System can detect phase sequence within a cycle and can identify and protect system form any unbalance condition instantaneously.

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