HIGH VOLTAGE, HIGH CURRENT, NON-DESTRUCTIVE FBSOA TESTING

By Al Pshaenich

This Application Note provides specifications for a test instrument which can be used to perform non-destructive testing of the Second Breakdown (S.B.) limits of the Forward Bias Safe Operating Area (FBSOA) curve. In addition, this note illustrates typical S.B. portions of the FBSOA and temperature derating curves for various technologies.

INTRODUCTION

A prime concern to both users and suppliers of power transistors is verification of the second breakdown capability of the devices. Second breakdown energy limitation can manifest itself under two operating conditions: active-region safe operating area, commonly referred to as Forward Bias Safe Operating Area (FBSOA); and Reverse Bias Safe Operating Area (RBSOA).

FBSOA is defined for turn-on conditions where the base is forward biased and forward base current, I_{B1}, flows, or when the base is open circuited. RBSOA, on the other hand, occurs when reverse base current, I_{B2}, flows during device turn-off. For either condition, second breakdown (S.B.) is the result of current crowding in the emitter finger due to direction of the lateral field in the base. The field causes current crowding at the periphery of the emitter during forward bias and at the center of the emitter during reverse bias. This greater current density produces a hot spot which eventually causes the transistor to go into second breakdown. If the energy is not quickly removed, the device will be destroyed.

NOTE: The mechanism and theory of S.B. has been under investigation since as early as 1958. Rather than to briefly try to review the complex phenomena, the reader may refer to the references listed at the end of this paper.

This paper will address the non-destruct testing of FBSOA. Since conventional methods of measuring the S.B. limits of the FBSOA curve (Figure 1) invariably result in device failures, the generation of a complete family of curves through destructive testing is costly and time consuming. Generally, the transistor under test (TUT) is measured for S.B. capability in a common base configuration (Figure 2), allowing for easily adjustable and repeatable collector current, collector-emitter voltage and pulse width measurements. To determine the S.B. capability of the transistor, either the voltage or current for a particular pulse width is increased until the device fails. Several transistors are tested in this manner and the failed points recorded. The number of devices tested at each condition is dictated by the degree of clustering of failed parts; it is not unusual for as many as five to ten devices to be tested at each point on an S.B. curve to determine a guaranteed energy level. (The specification $I_{S/B}$ is often listed on the transistor data sheet which defines the one guaranteed point on the FBSOA curve.) For a single pulse width S.B. limitation curve, perhaps four different power levels are tested. A complete family of curves could thus require destructive testing of as many as 100 transistors.

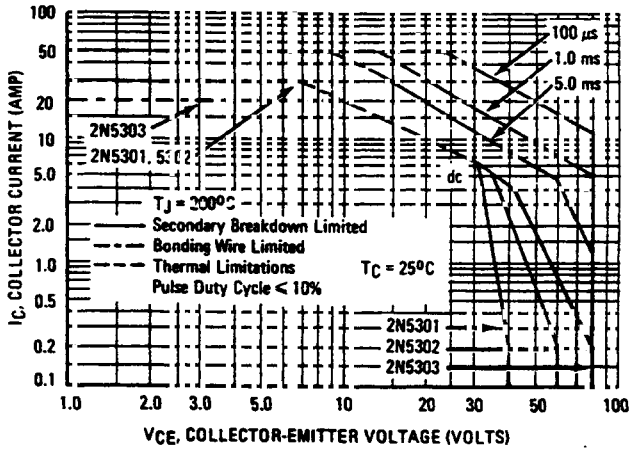

FIGURE 1 – Typical FBSOA Curve

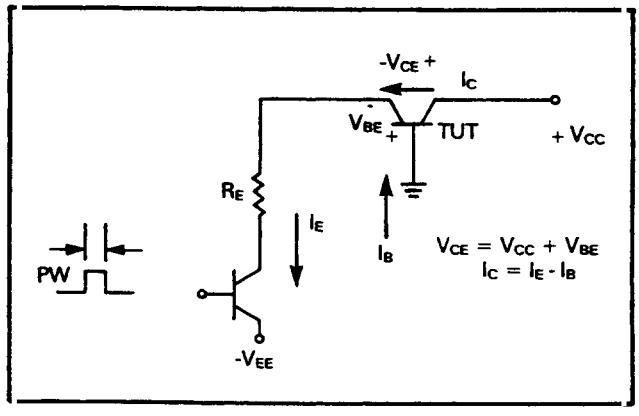

FIGURE 2 – Simplified Common-Base Test Circuit for Measuring FBSOA Second Breakdown

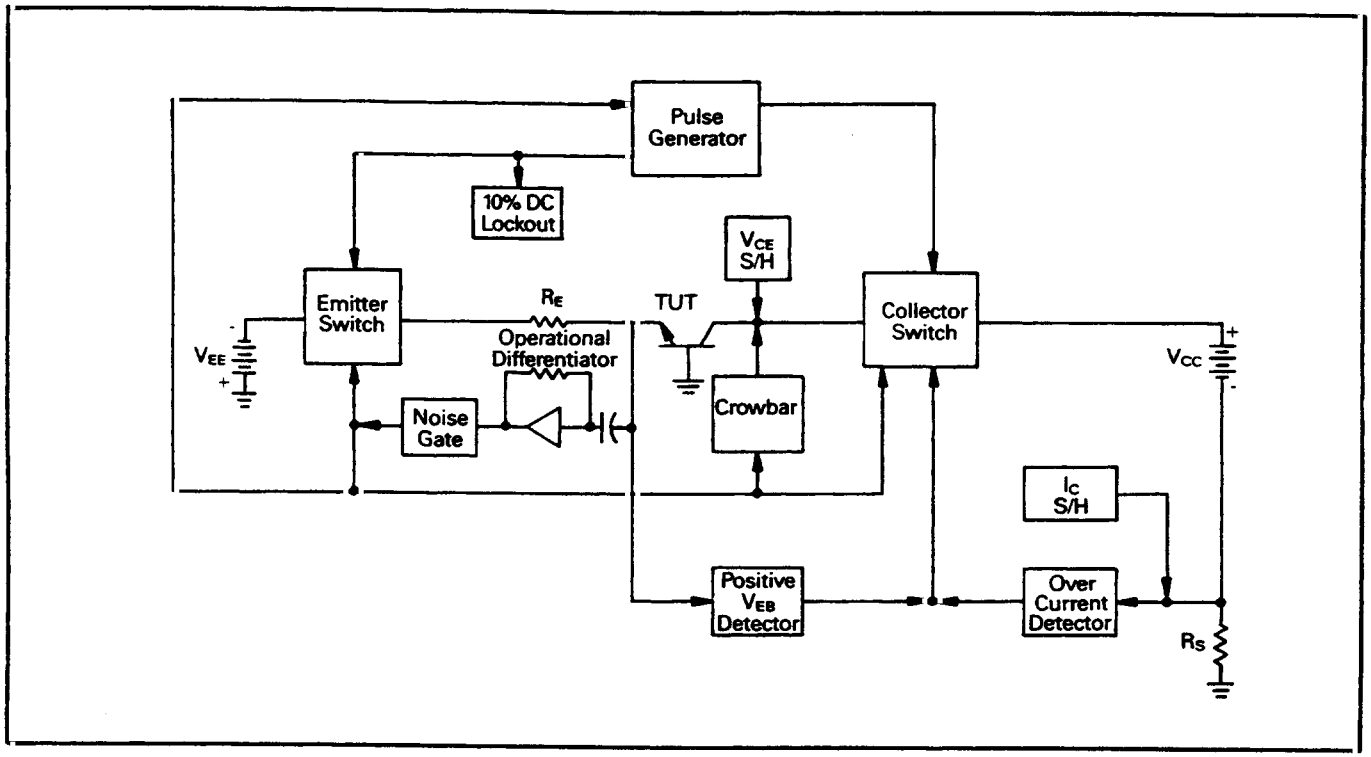

FIGURE 3 – Block Diagram of the Non-Destruct Forward Bias Second Breakdown Tester

To further complicate the picture, if the temperature effects of S.B. are investigated, even more devices must be tested.

If a non-destruct FBSOA tester can be used, then conceivably only one transistor (or perhaps several if the one TUT fails or is degraded) can be used to generate the complete family of curves. This Application Note discusses the design and operation of a Non-Destruct FBSOA Tester for NPN power transistors. In addition, this Note illustrates typical S.B. portions of the FBSOA and temperature derating curves for various technologies.

NON-DESTRUCT TESTERS

Any non-destruct tester, be it FBSOA or RBSOA, requires an energy limitation detection circuit that will measure the onset of S.B. and very rapidly remove this energy from the TUT before it is overstressed. Some commercial testers detect the collapsing collector-emitter voltage when S.B. occurs as measured by a positive going emitter voltage of an NPN transistor connected in a common base configuration.

Another non-destruct tester, developed by Sherwin Rubin and David Blackburn of the National Bureau of Standards[1], measures the onset of thermal instability by monitoring the base-emitter voltage for waveform anomalies. When a stable hot spot starts to develop, the base-emitter voltage will suddenly decrease slightly due to the negative temperature coefficient of the junction. The stable hot spot condition occurs for some power transistors at a somewhat lower energy level than that of second breakdown. By increasing the sensitivity of the detector and monitoring the base-emitter voltage, the stable hot spot can be detected and power can be removed from the device before failure or degradation occurs.

The Motorola non-destruct FBSOA fixture uses the base-emitter voltage monitoring method with the addition of over-voltage and over-current sensing circuitry. Empirical tests of this non-destruct FBSOA fixture reveal that by reducing the detectors sensitivity the small signal indicating a stable hot spot can be ignored, but the larger signal due to second breakdown can be detected. Test measurements were verified by opening the detector loop and ultimately causing the TUT to fail at the same energy level as when the loop was intact. These second breakdown test results also correlated very well with tests performed on a commercial tester.

NON-DESTRUCT SECOND BREAKDOWN TESTER CIRCUIT OPERATION

The block diagram of the Non-Destruct Forward Bias Second Breakdown Tester is shown in Figure 3. As shown in the simplified schematic of Figure 2, the TUT is connected in a common base configuration with both V_{CC} and V_{EE} supplies switchable, allowing variable pulse widths to be applied to the transistor. The other main blocks are the Operational Differentiator, connected to the emitter for detecting V_{BE} anomalies; the Noise Gate for locking out switching transients; a Crowbar circuit for rapidly removing the collector supply from the TUT when second breakdown is detected; and the internal Pulse Generator, designed with CMOS IC's. Other secondary circuits are: the Over-Current Detector; Positive V_{EB} Detector; Greater than 10% Duty Cycle Lockout; and the V_{CE} and I_C Sample and Hold Readout circuits. With the exception of the V_{CC} and V_{EE} supplies, the system is self contained and has a capability of subjecting the TUT with as much as 400 V and 25 A. Pulse widths are variable from about 100 μs to 2 s, either free running at less than 10% duty cycles or single pulsed (1 shot). The complete schematic is shown in Figure 4 (p. 4).

PULSE GENERATOR

The pulse generator is designed with CMOS MC14001, quad 2-input NOR gates, using U1A and U1B as a variable frequency (by means of potentiometer R1) astable multivibrator (MV) clocking a monostable variable Pulse Width (R2) MV (U2A and U2B). Two other MV's are associated with the pulse generator – the Noise Gate MV (U3A and U3B) and the Sample Delay MV (U2C and U2D). Additionally, the Noise Gate, consisting of NOR gates U3C, U3D, and U2C, completes the total 12 gate complement of the three I.C.'s.

For free run operation, switch S1 is in the position as shown, allowing the astable MV to clock the three monostable MV's. Single pulse operation is obtained by throwing S1 to the 1-Shot position and depressing the pushbutton start switch, S2.

Note that these I.C.'s are powered with an internally packaged, -12 V power supply. Thus, the output of the Pulse Width MV (gate U2B) is a positive going pulse referenced to -12 V.

EMITTER SWITCH

The emitter switch, consisting of cascaded NPN transistor Q1, PNP transistor Q2 and power output NPN transistor Q3, amplifies the CMOS pulse width output to current levels as high as 25 A. To minimize internal power supply drain, Darlington transistor Q2 emitter is tied to ground (base drive for Q3 is derived from $-V_{EE}$). Thus the NPN drive transistor Q1 emitter is connected to -12 V, necessitating the CMOS gates' -12 V supply operation.

Emitter current for the TUT is controlled by varying the external $-V_{EE}$ power supply and/or the front panel selectable (by switch S4B) collector load resistors of Q3. Base drive to Q3 is also varied accordingly with switch S4A.

When second breakdown is detected, a trigger pulse is fed to the gate of SCR Q4, clamping off Q3 and thus turning off the emitter switch; (the Pulse Generator is also turned off, as will be subsequently described).

10% DUTY CYCLE LIMIT

Since all transistor stages are direct coupled, the duty cycle (D.C.) must be limited to about 10% maximum to prevent excessive dissipation in the coupling resistors (particularly the 10 ohm, 10 W base current limiting resistor to Q3). This is accomplished by PNP Darlington transistor Q5 and input clamp NPN transistor Q6. As the D.C. increases, the charge builds up on the integrating capacitor in the base circuit of Q5, eventually turning Q5 on. Consequently, the 10% D.C. LED turns on, indicating excessive duty cycle, and Q6 turns on, effectively limiting the input pulse width.

COLLECTOR SWITCH

If the TUT were to fail by shorting, the external, variable, V_{CC} supply would be excessively stressed unless this power supply could be quickly removed from the system. The Collector Switch prevents this condition as this circuit is switched on and off concurrent with the Emitter Switch. This series connected switch must sustain the full V_{CC} supply (400 V max, 25 A max); therefore, its input must be amplified and level translated from the CMOS Pulse Generator output level. This is accomplished by the negative going output pulse of gate U1D turning on, in order, PNP driver Q7, constant current configured NPN level translator Q8, PNP driver Q9, and series switch Q10 and Q11. Transistors Q9, Q10, and Darlington transistor Q11 form a compound configuration requiring only about 3 mA of base drive to Q9 to supply 25 A emitter current from Q11.

Like the SCR clamp in the Emitter Switch, SCR Q12 clamps off Q8 when second breakdown is detected.

OPERATIONAL DIFFERENTIATOR

The operational differentiator is the most unique and important circuit in the system. It monitors the TUT emitter-base voltage, detecting any rapid change in the waveform, as shown in Figure 5. (In reality, it measures V_{EB} plus the forward voltage drop of the reverse base current blocking diode in the base of the TUT). The Pulse Generator output to the Emitter and Collector Switches (Figure 5A) allows propagation-delayed TUT collector current to flow (Figure 5B), with the resultant V_{EB} (Figure 5C). When a hot spot or onset of second breakdown starts to occur, the V_{EB} will suddenly decrease (dotted portion of the curve). The input capacitor to op-amp U4 will differentiate this waveform (Figure 5D), producing the U4 Operational Differentiator output (Figure 5E). The magnitude of this signal is a function of the capacitor chosen by the front-panel selector switch S3 – the larger the capacitor, the greater the differentiator sensitivity. A high gain comparator U5 follows this stage (with input threshold control R3 for noise immunity) setting the quiescent output high.)

The output of U5 will consequently be that of Figure 5F: false switching signals on the leading and trailing edges of the waveform with the true signal, if second breakdown is detected, somewhere in the middle. This signal is then sent to the Noise Gate for discrimination.

NOISE GATE

Utilizing the NOR gate logic and the propagation delay of the Emitter Switch, the Noise Gate can reject the respective leading and trailing edge switching signals. By NORing the positive going Noise Gate MV output, U3B in Figure 5G, with the inverted Pulse Width output, U1D, the waveform of Figure 5H will result. When this waveform, in turn, is NOR'd with the comparator U5 output, the result will be the waveform of Figure 5I – just the signal due to hot spotting or second breakdown will be transmitted. This signal will be amplified by cascaded switching transistors Q13 and Q14 to supply the trigger for all of the shutdown circuits.

CROWBAR

In addition to the two clamp SCR's of the Emitter and Collector Switches being activated by the second breakdown trigger, the Crowbar power MOSFET Q15 is also turned on. This TMOS FET, rated at 500 V and 4 A, is connected from the collector of the TUT to the ground. Being an extremely fast switching device, the FET will quickly divert or crowbar the current from TUT when second breakdown occurs, momentarily shorting out the V_{CC} power supply for the delay time required to open the Collector Switch (about 20 μs). Having high pulsed current ratings, the FET is well able to sustain this energy. Using a FET as a crowbar greatly ensures the survival of the TUT.

Another feature of the tester is the ability to shut down the Pulse Width MV once second breakdown occurs, if so required. This shut down is accomplished by SCR Q16 being fired by the trigger, which turns on (through series connected switches, S6 and S7) the PNP clamp transistor, Q17. This transistor places a logic 1 (ground) to the nor-

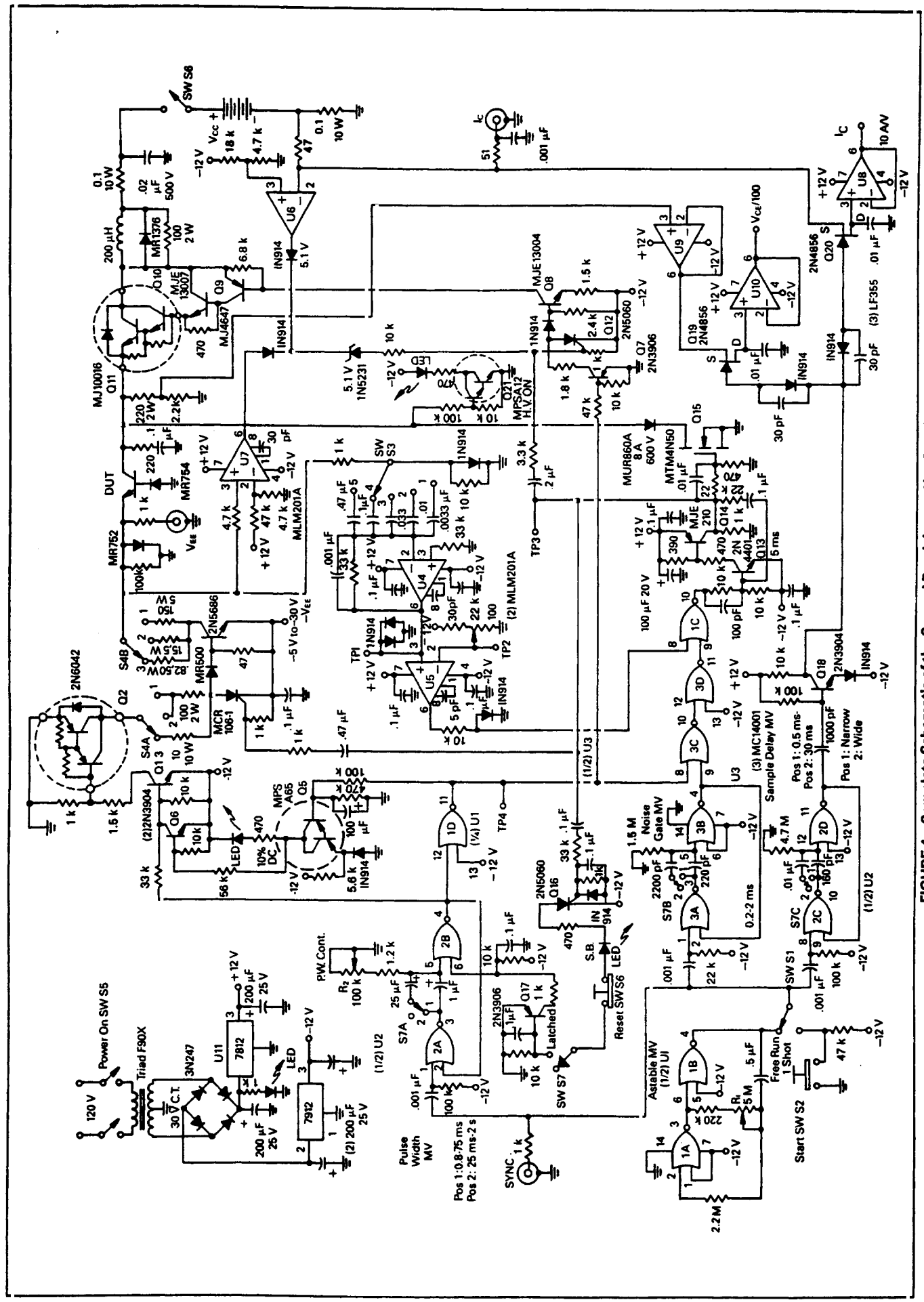

FIGURE 4 – Complete Schematic of the Second Breakdown – Hot Spot Tester

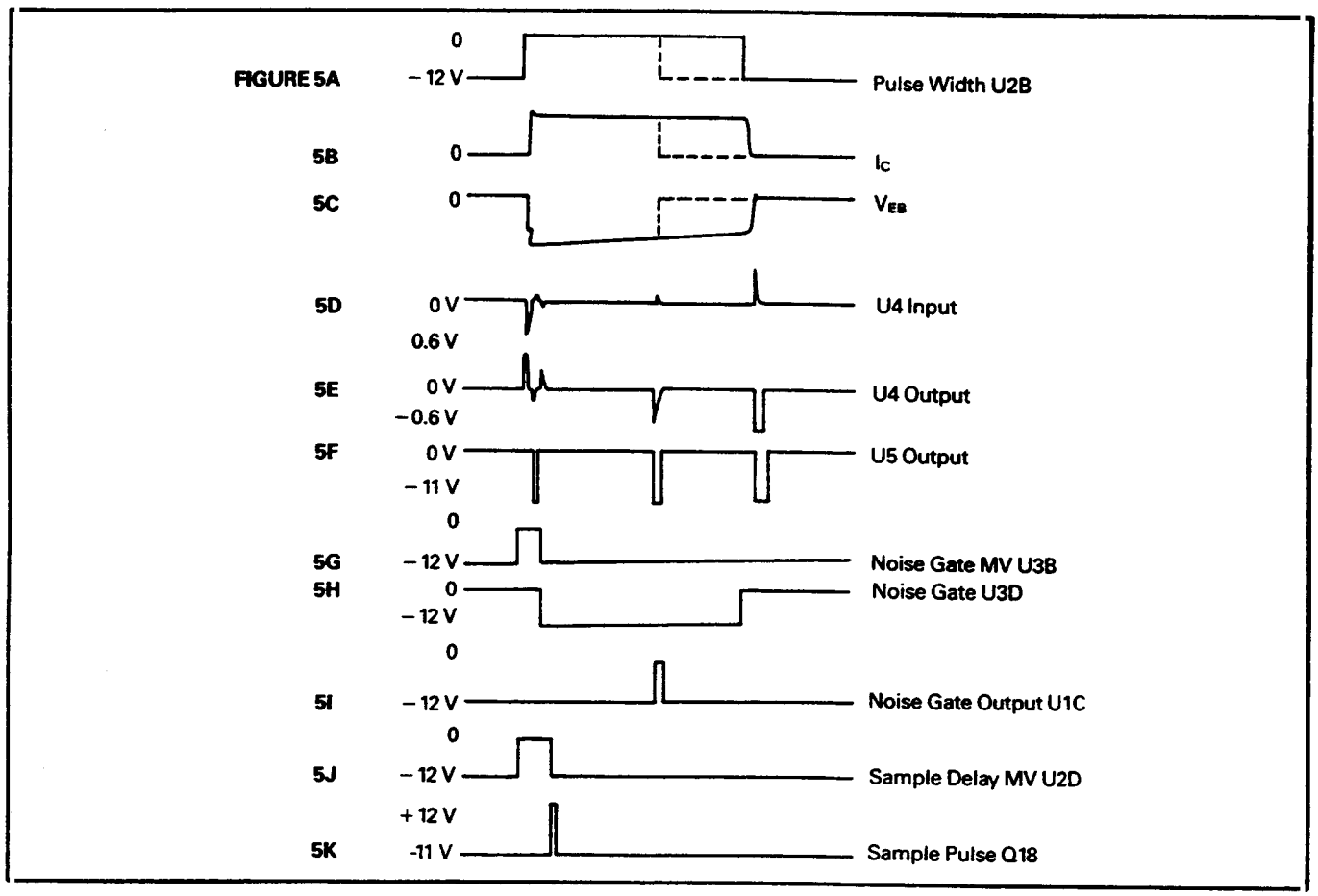

FIGURE 5 – Waveforms of S.B. Non-Destruct Tester

mally low (-12 V) input of NOR gate U1D, inhibiting the monostable MV from pulsing and thus preventing further application of power to the TUT. The system (SCR Q16) is reset be depressing pushbutton Switch S6.

If this latch condition is not required, Switch S7 is thrown open and the system free-runs, although Pulse Widths are shorter than normal due to S.B. Now, the clamp SCR's Q4 and Q12 are reset after every free running pulse.

OVER CURRENT

To ensure that the output stages of the Emitter and Collector Switches operate within their maximum current ratings, a simple comparator circuit is incorporated. The comparator U6 measures the voltage drop across the 0.1 ohm sense resistor in the return leg of the V_{CC} supply. When this total power supply current approaches 25 A, the comparator will switch positively and thus fire clamp SCR Q12. Consequently, the Collector Switch opens, removing the supply from the system.

POSITIVE V_{EB} DETECTOR

Some commercial testers detect second breakdown by monitoring the V_{EB} for a positive going, above ground, voltage. Recall that in the common base configuration, the normal V_{EB} pulse is negative going from ground (Figure 5C).

When second breakdown occurs, the collapsing collector-emitter voltage will force the emitter positive. With the Motorola tester, the clamp diode from TUT emitter to ground prevents this voltage from exceeding one diode drop. This signal is then measured by comparator U7 whose output will also trigger SCR Q12 when V_{EB} goes positive. In effect, this is a redundant detector, offering secondary protection, as the Operational Differentiator normally triggers earlier.

SAMPLE AND HOLD READOUTS

The last of the main blocks of circuits are the TUT collector current, I_C, and collector-emitter voltage, $V_{CE}/100$, readouts. Employing standard Sample and Hold (S/H) circuitry, the I_C circuit samples the voltage drop across the V_{CC} supply sense resistor and the $V_{CE}/100$ circuit measures the attenuated collector-ground voltage of the TUT ($V_{CG} \approx V_{CE}$). (For accurate power measurements, S/H techniques are required as analog measurements integrate the transient responses of the pulsed power supplies.)

Both S/H circuits are driven by a common sample pulse, with the Sample Delay MV (gates U2C and U2D) positioning the sample pulse and transistor Q13 (configured as a half monostable MV) providing the pulse width. Normally on Q18 is turned off by the negative going, trailing edge Sample Delay pulse (Figure 5J). The RC differentiating circuit in the base of Q18 thus dictates the sample pulse width output of Q18 (Figure 5K). The positive going pulse (approximately 40 μs wide) then turns on the respective series conected FET switches (Q19 and Q20) to charge the hold capacitors. Unity gain connected op-amp U9 buffers the high impedance, collector voltage atten-

TABLE 1 – Forward Bias Second Breakdown Derating with Temperature

DEVICE	CASE	PROCESS	APPLICATION DESIGNATION	V_{CEM} (V)	CONDITIONS			% DERATED TO AT 150°C
					V_{CE} (V)	P.W. (ms)	I_C (A)	
2N5301	TO-3	EPI BASE	PWR BASE I	100	80	50 200	2.4 2.0	67%
MJ15003	TO-3	EPI BASE	PWR BASE I	140	100	50 200	4.7 3.7	50%
SJ4008	TO-3	EPI BASE	PWR BASE II	175	100	50	5.8	60%
MJ15052	TO-3	EPI BASE	PWR BASE III	175	100	50	4.5	50%
MJ15022	TO-3	EPI BASE	PWR BASE III	200	150 200 250	200	1.5 0.96 0.64	50%
MJ11032	TO-3	EPI BASE	L.V. DARLINGTON	100	60	50 200	6.5 3.2	60%
2N6282	TO-3	EPI BASE	L.V. DARLINGTON	100	60	50 200	7.5 5.6	52%
					100	50 200	1.4 1.2	58%
MJ10016	TO-3	DBL DIFF EPI COL.	H.V. DARLINGTON	400	100	50	0.9	67%
BU806	TO-220	DBL DIFF EPI COL.	H.V. DEFLECTION	250	70	50	0.75	60%
MJE12026	TO-220	TRIPLE DIFF.	S.M. III	400	200	50 200	0.38 0.35	67% 63%
TIP 121	TO-220	EPI BASE	L.V. DARLINGTON	80	60	50 200	0.69 0.65	55% 60%
2N6488	TO-220	EPI BASE	GEN. PURPOSE AMP & SW	80	60	50 200	2.3 1.8	55%
MJE15030	TO-220	DBL DIFF PLANAR	AUDIO DRIVER	150	70	50 200	0.56 0.47	70% 65%

uating resistors and op-amps U8 and U10 are the Hold amplifiers. These three op-amps have FET inputs to provide the required extremely high input impedance.

POWER SUPPLIES

With the exception of the external, high power, variable V_{CC} and V_{EE} supplies, the S.B. tester is completely self-contained and includes the low power ±12 V supplies which are simple, linear power suplies derived from IC regulators U11 and U12. These regulators easily handle the pulsed current requirements of the system's low level circuitry (about 60 mA max).

SECOND BREAKDOWN TEST RESULTS

Second Breakdown Temperature Derating

FBSOA curves similar to Figure 1 are commonly shown on power transistor data sheets and are generally defined at a given case temperature T_C, junction temperature T_J, or ambient temperature T_A. What is not usually shown is second breakdown temperature derating curves or specifications.

The non-destruct S.B. tester simplifies the generation of the second breakdown temperature derating curve since only one device (or a few, if the TUT is degraded with testing) need be tested with variable temperatures, voltages and/or pulse widths.

A number of Motorola power transistors covering various processes and applications, in TO-3 and TO-220 cases were S.B. tested. Of major interest is the behavior of these TUT's with increasing case temperature. A simple method for varying the transistor case temperature is to elevate the heat sink temperature with power resistors. Then, S.B. can be measured at any case temperature. Figures 6A through 6E describe the actual S.B. detected points on five of the devices. The results are quite linear, with the five devices derated down to about 50% to 65% at 150°C from the 25°C T_C reading.

In a similar manner, temperature data was taken on several other transistors; the test results are shown in Table 1. On the average, the TUT's were derated to about 60%, varying from a high of about 70% to a low of 50%. This admittedly limited test program (only one to three typical transistors of each type were tested) showed that the S.B. of the transistors was in some cases a second order function of V_{CE} and/or pulse width. The conditions listed in the table describe these variables.

Second Breakdown Versus Pulse Width

Also of interest is the behavior of S.B. versus pulse width – the familiar FBSOA curves. Accurate results can now be obtained because the curves are generated from one device. Typical examples are illustrated by the curves of Figures 7A through 7E. These curves should be compared with a plot of failed devices derived from destructive testing, as shown in Figure 8. (The intermixing of points for various pulse tests complicates the drawing of the final, derated curve).

The variation of the second breakdown with large pulse widths – 1 s, 200 ms and 50 ms is shown in Table 2 for several of the devices. This data is of importance particularly when trying to correlate the results from different testers; as an example, some equipment might pulse test at 1 second and another test at 50 ms.

In regard to correlation testing, the results comparing the commercial tester (TES Corporation [Tanaka] 7622-TS Tester and 7623-PU Power Unit) with the lab non-destruct tester were excellent. Twelve BU807 devices were tested on both machines at 100 V and 50 ms; the

FIGURE 6 – Forward Bias Second Breakdown Temperature Derating

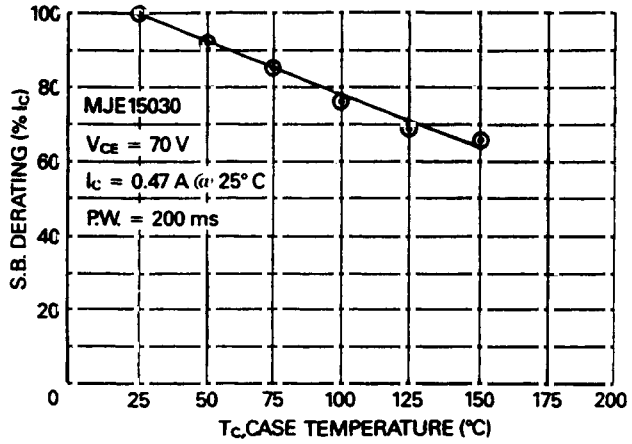

FIGURE 6A – MJE15030

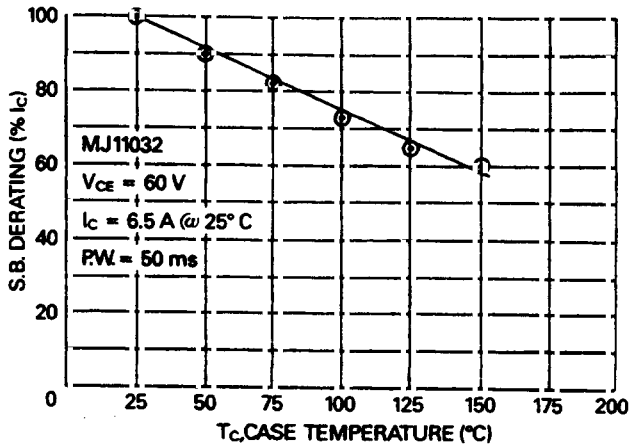

FIGURE 6B – MJ11032

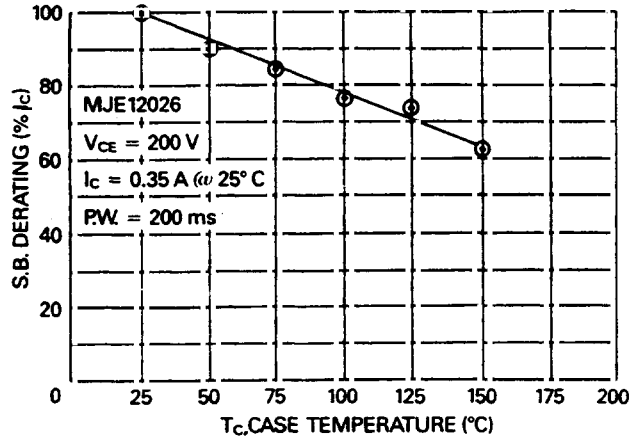

FIGURE 6C — MJE12026

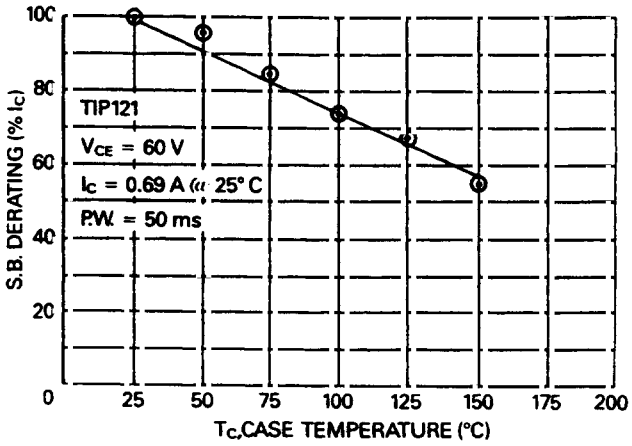

FIGURE 6D – TIP121

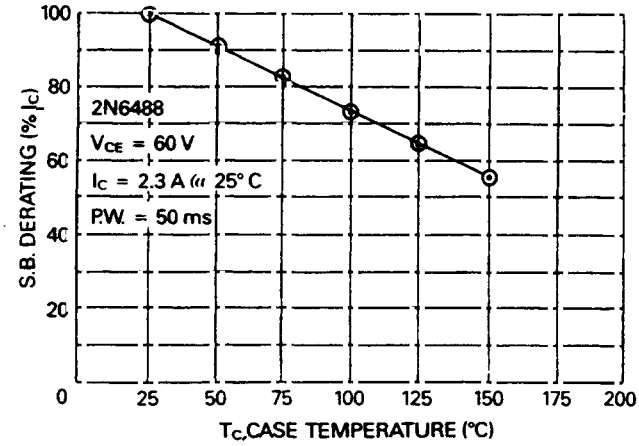

FIGURE 6E – 2N6488

differences in I_C at S.B. were at most 3% (10 mA at 330 mA average). Similar results were obtained when comparing the MJE15030 at 70 V and 50 ms. The TES Tester, however, costs about $20,000 and has only 300 W (200 V at 1.5 A, 30 V at 10 A) capability. All testers, including the Motorola unit described in this paper, have a limited minimum pulse width non-destruct capability. The limitation is primarily due to the response time of the switched power supplies. Any ringing or transients on the switched leading edge can reflect to the detector as an error signal. Consequently, the time for this transient to damp out must be blanked from the detector. For the Motorola tester, the Noise Gate MV provides the blanking period. Empirical testing determined that the minimum blanking time required for the power supplies used should be about 100 μs when testing with narrow pulses. Larger pulse widths can use longer blanking periods. A front-panel switch, S7B, allows selection of either 100 μs or 2 ms blanking time. Sections of this switch (S7A and S7C) are ganged to the Pulse Width MV and Sample Delay MV to change their time accordingly.

A second condition that limits non-destruct pulse width is the time constant of the RC differentiating circuit on the input of the Operational Differentiator. This network must completely recover in the time frame involved. Consequently, for narrow pulse widths, the smallest capacitor must be used, yet it still must provide enough sensitivity to fire the shutdown circuits. For second breakdown protection, the 0.01 μF capacitor was satisfactory for all pulse widths down to 5 ms; for 1 ms pulses, the 0.0033 μF capacitor usually suffices and protects the TUT. Testing with pulses narrower than 500 μs was not generally reliable.

This tester was originally designed to detect stable hot spots in power transistors, and thus required greater dif-

FIGURE 7 – Active Region Safe Operating Area (FBSOA)
Curves Derived with Non-Destruct Tester

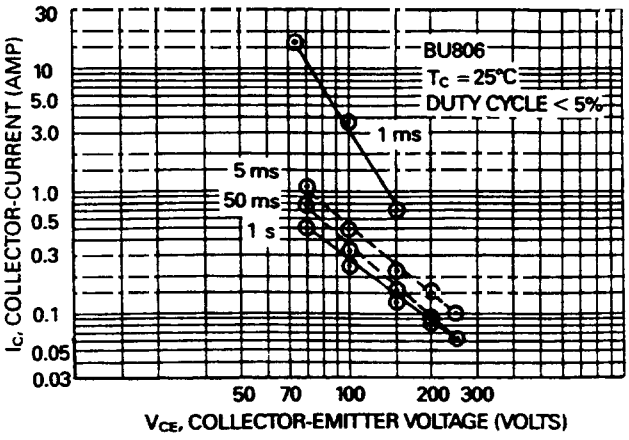

FIGURE 7A – BU806

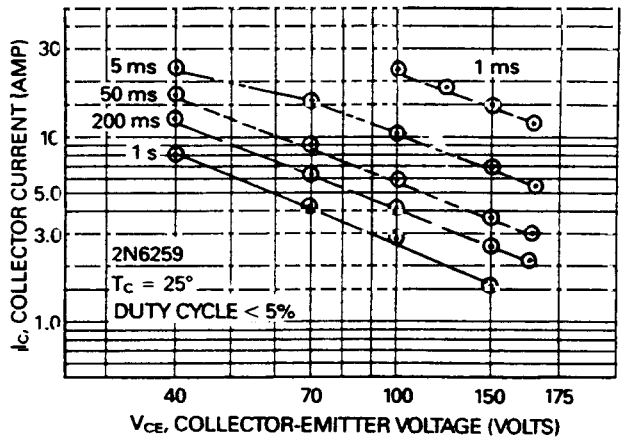

FIGURE 7B – 2N6259

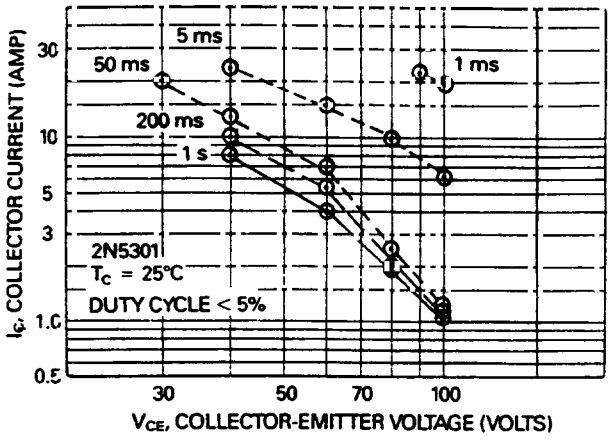

FIGURE 7C – 2N5301

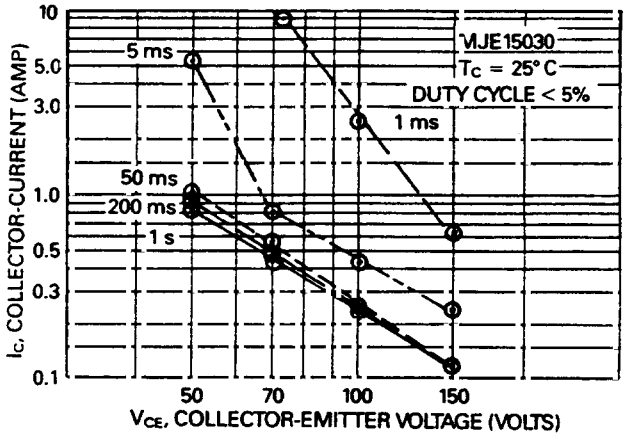

FIGURE 7D – MJE15030

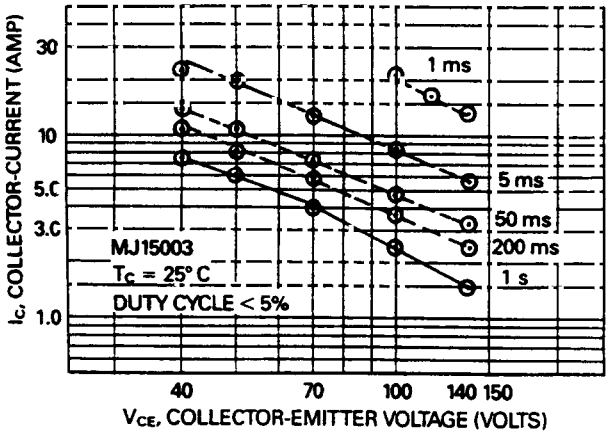

FIGURE 7E – MJ15003

ferentiator sensitivity (0.1 to 0.47 μF). Therefore, the locus of a stable hot spot curve generally falls within the measured second breakdown curve for those transistors that exhibit this phenomenon. (The published S.B. curve should be adequately derated to include hot spotting.) This is illustrated by the curves of Figure 8 and the data of Table 3.

TABLE 2 – The Effect of Pulse Width on Forward Bias Second Breakdown

Device	V_{CE} (V)	I_C @ 50 ms (Amps)	I_C Normalized (T_A = 25° C) Versus Pulse Width		
			50 ms	200 ms	1 s
2N5301	80	2.4	100%	83%	79%
MJ15003	100	4.7	100%	80%	53%
2N6259	70	6.7	100%	70%	52%
MJ15052	100	4.5	100%	72%	57%
MJ11032	60	6.5	100%	49%	42%
2N6282	60	7.5	100%	75%	55%
MJ10016	100	0.85	100%	94%	88%
BU806	70	0.74	100%	78%	72%
MJE12026	200	0.43	100%	91%	70%
TIP121	60	0.69	100%	94%	88%
2N6488	60	2.3	100%	78%	61%
MJE15030	70	0.47	100%	84%	77%

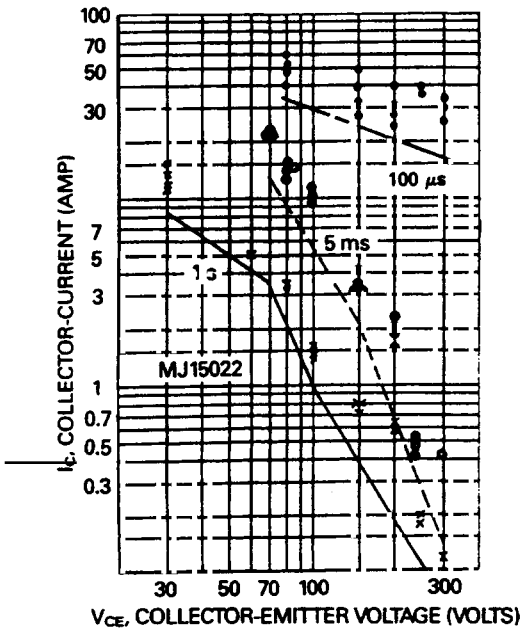

FIGURE 8 – Derivation of the MJ15022 FBSOA Curves

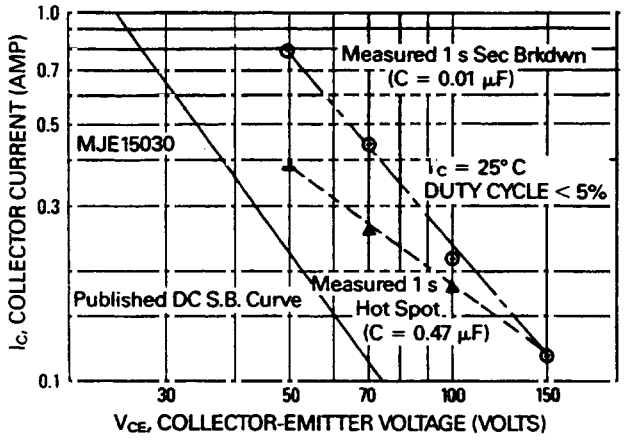

FIGURE 9 – Comparison of FBSOA Second Breakdown Versus Stable Hot Spot for the MJE15030

TABLE 3 – Difference in Collector Current Between Second Breakdown and Hot Spot

DEVICE	V_{CE} (V)	PULSE WIDTH (ms)	I_C @ (A)	
			SEC BRKDWN	HOT SPOT
MJ10016	100	50	0.85	0.51
MJE12026	200	200	0.39	0.12
MJE15030	70	200	0.47	0.27
2N6282	100	50	1.4	1.4

And lastly, the purpose of the non-destruct tester is to test devices without degradation (which generally shows up as an increase in leakage current). No meaningful change in leakage current I_{CES} and I_{CBO} was noted for the several devices measured before and after a number of S.B. stresses.

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