ADC5020/ADC5030

Wide Dynamic Range, High-Speed, 18-Bit Sampling A/D Converters

With Sub-ranging Architecture

Introduction

The ADC5020/ADC5030 18-bit A/D converter, designed with a unique sub-ranging architecture, achieves excellent speed, accuracy, and linearity. For digitizing fast time-varying signals, the ADC5020 has a built-in sample-and-hold amplifier. For applications with multiplexed DC signals or an external sample-and-hold, the more economical ADC5030 is available with a high impedance input buffer in place of the sample-and-hold. With a 144 kHz sampling rate, the ADC5020 can digitize professional audio signals (20 Hz to 20 kHz) at 3X oversampling, minimizing the design complexity of the anti-aliasing filters. The high sampling rate, low noise, low distortion and superior zero-crossing linearity of the ADC5020 optimize this converter for professional audio and spectroscopic applications.

The ADC5020/ADC5030's sub-ranging architecture uses a three-pass recycling technique in a design that both minimizes parts count and yields unprecedented stability, linearity, and accuracy. To achieve this superior performance, the ADC5020/ADC5030 relies on a proprietary reference D/A converter that has inherent 18-bit accuracy and linearity. The D/A converter, in conjunction with logic circuitry in a specialized gate array, detects and corrects inaccuracies and linearity errors that could arise from the flash A/D converter and amplifier circuitry in the conversion path. For applications requiring fine offset and gain adjustments, the converter has provisions for dynamically setting these DC parameters. The ADC5020/ADC5030 also provides easily accessible offset-trim and gain-trim potentiometers. This truly unique product comes in a fully-shielded 3" x 4" module with 0.1" pin spacings for easy installation on printed circuit boards. The specifications of the ADC5020/ADC5030 are fully ensured by thorough, computer-controlled factory tests.

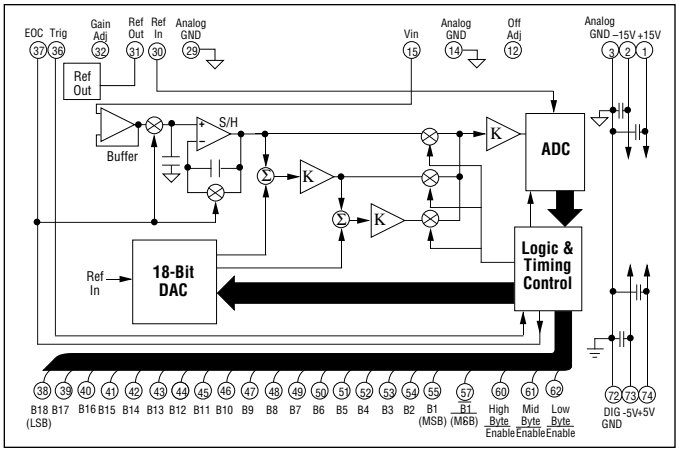
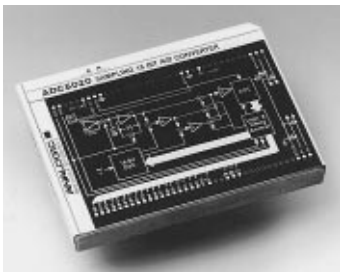


Figure 1. ADC5020 Functional Block Diagram.



Features

- ❑ 18-Bit Resolution
- ❑ 5 µs Conversion Time (ADC5030)
- ❑ 144 kHz Throughput Rate (ADC5020)
- ❑ No Missing Codes
- ❑ Wide Dynamic Range: 108 dB
- ❑ Signal-to-Noise Ratio: 105 dB (1 kHz)
- ❑ Peak Distortion: –110 dB (1 kHz)
- ❑ Total Harmonic Distortion: –105 dB (1 kHz)
- ❑ Ease of Use
- ❑ Built-in S/H Amplifier (ADC5020)
- ❑ TTL Compatibility
- ❑ Low Cost
- ❑ Low Power
- ❑ Electromagnetic/Electrostatic Shielding

Applications

- ❑ Professional Audio Encoding
- ❑ Spectroscopy
- ❑ Digital Telecommunications
- ❑ Automatic Test Equipment
- ❑ High-Resolution Imaging
- ❑ Seismic Instrumentation
- ❑ Medical Data Acquisition
- ❑ Satellite Communications
- ❑ Multiplexed Data Acquisition

ADC5020/ADC5030

Specifications

ANALOG INPUT

Input Range
±10V, ±5V, 0 to +10V [12]

Input Bias Current
500 nA Typ.

Input Capacitance
10 pF Typ.

Input Impedance
100 kΩ Typ.

DIGITAL INPUTS

Logic Levels
Logic "0"
0.8V Max.

Logic "1"
2.0V Min.

Logic Currents
Logic "0"
–0.4 mA

Logic "1"
20 µA

Trigger Pulse Width
50 ns Min.

High Byte Enable
Active Low B1-B8, B1

Mid Byte Enable
Active Low B9-B16

Low Byte Enable
Active Low B17, B18

DIGITAL OUTPUTS

Fan-Out
1 TTL Load Max.

Output Coding [12]
Offset Binary, Complementary Offset Binary, Two's Complement, Binary, Complementary Binary

Output Voltage
Logic "0"
0.4V Max.

Logic "1"
2.4V Min.

End of Conversion (EOC)
High During Conversion

REFERENCE

Internal Reference Output Voltage
–6.5V Typ. (1 mA DC external load)

Recommended Input [2]
–6.5V

Input Impedance
1.6 kΩ Typ.

DYNAMIC CHARACTERISTICS

Maximum Throughput Rate
ADC5020
144 kHz Min.

ADC5030
200 kHz Min.

A/D Conversion Time
5 Ms Max.

Signal-to-Noise Ratio [3, 6, 7]
DC to 10 kHz
105 dB Typ. 100 dB Min.

Peak Distortion [4, 6, 7]
1 kHz
–110 dB Typ., –100 dB Min.

10 kHz
–105 dB Typ., –95 dB Min.

Total Harmonic Distortion [5, 6, 7]
1 kHz
–105 dB Typ., –96 dB Min.

10 kHz
–100 dB Typ., –92 dB Min.

S/H Acquisition
1.9 µs Typ.

S/H Aperture Delay
30 ns Typ., 60 ns Max.

S/H Aperture Jitter
0.2 ns Typ., 0.4 ns Max. RMS

S/H Feedthrough [8]
–100 dB Max.

TRANSFER CHARACTERISTICS

Resolution
18 bits

Quantization Error
±0.5 LSB

Integral Nonlinearity
0.002% FSR Max., 0.0005% FSR Typ.

Differential Nonlinearity
±0.5 LSB Typ., ±0.8 LSB Max.

Offset Error [9, 10]
±1 mV Max.

Gain Error [9, 10]
0.01% FSR Max.

No Missing codes
Guaranteed from 0°C to 60°C

A/D Converter Noise
40 µV RMS ADC5020 [11]
30 µV RMS ADC5030

STABILITY (0°C TO 60°C)

Differential Nonlinearity
±0.5 ppm FSR/°C Max.

Offset Voltage
±10 ppm FSR/°C Max.

Gain
±10 ppm FSR/°C Max.

Warm-Up Time
5 minutes Max.

Supply Rejection
Offset
±5 ppm FSR/% Typ.

Gain
±5 ppm FSR/% Typ.

POWER REQUIREMENTS [14]

Supply Range
±15V Supplies [13]
11.65V Min., 15.45V Max.

±5V Supplies
4.75V Min., 5.25V Max.

±15V Current Drain
ADC5020
52 mA Typ.

ADC5030
42 mA Typ.

+5V Current Drain
40 mA Typ.

–5V Current Drain
70 mA Typ.

Power Consumption
ADC5020
2.11W Typ.

ADC5030
1.96W Typ.

ENVIRONMENTAL & MECHANICAL

Temperature Range
Rated Performance
0°C to 60°C

Storage
–25°C to 80°C

Relative Humidity
0 to 85% Non-condensing up to 60°C

Dimensions
3" x 4" x 0.44"

Shielding
Electromagnetic 5 sides, Electrostatic 6 sides

Case Potential
Ground

Notes:

1. Unless otherwise noted, all specifications apply at 25°C. Supplies are ±15V and ±5V. Full scale range is ±5V.
2. Reference input is optional. If it is not used, Ref In must be jumpered to Ref Out.
3. Signal-to-Noise Ratio represents the ratio of the RMS value of the signal to the total RMS noise below the Nyquist rate. The total RMS noise is computed by: (1) summing the noise power in all frequency bins not correlated with the test signal; (2) estimating the total noise power contained in all harmonic frequency bins; and (3) computing the RMS noise from the sum of (1) and (2).
4. Peak Distortion represents the ratio of the highest spurious frequency component below the Nyquist rate to the signal. Note that in computing Peak Distortion the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed. See Note 3.
5. Total Harmonic Distortion represents the ratio of the RMS sum of all harmonics up to the 100th harmonic to the RMS value of the signal. Note that in computing Total Harmonic Distortion the estimated noise allocated to the harmonic frequency bins in computing SNR is first removed. See Note 3.
6. Analysis bandwidth is DC to 20 kHz with 3.5V RMS input signal.
7. ADC5030 tested and guaranteed with Analogic's SHA2410 Sample-and-Hold.
8. Measured with 10V p-p at 25 kHz.
9. Refer to "Output Coding and Trim Procedure" for field adjustable gain and offset procedures.
10. With use of internal reference only.
11. Includes noise from S/H and A/D converter.
12. See Ordering Guide.
13. For 0 to 10V range (ADC5020/ADC5030-1) Min. supplies are ±14.55V.
14. Analogic highly recommends the use of linear power supplies with its high performance, high resolution A/D converters. However, if system requirements provide only a +5V supply and limited space, the use of the Analogic SP7008 DC-to-DC converter will provide a low noise solution which will not degrade the ADC5020/ADC5030 performance.

Specifications subject to change without notice.

ADC5020/ADC5030 SPECIFICATIONS

Output Coding and Trim Procedure

Figure 2 shows the output coding of the ADC5020/ADC5030 A/D converter. The symbol * in Figure 2 indicates a bit that is undergoing a 0/1 or 1/0 code transition at the indicated analog input voltage.

To trim the offset of the ADC5020/ADC5030, apply 19 µV to the analog input. Adjust the offset trim potentiometer such that the digital output corresponds to the truth table of Figure 2.

To trim the gain of the ADC5020/ADC5030, apply +4.999981V for the bipolar option or +9.999943V for the unipolar option. Adjust the gain trim potentiometer such that the digital output corresponds to the truth table of Figure 2.

In addition to the internal offset and gain potentiometers, provisions have been made to dynamically null out DC errors by use of external potentiometers or DACs. The ratio of A/D converter DC shift to the external control voltage is 500 µV/V. A 10V swing from a DAC on Pin 12 produces a 5 mV offset shift, a 10V swing on Pin 32 produces a 5 mV gain shift.

Truth Table

Input Voltage	Digital Outputs	
	Comp. Offset Binary MSB LSB	Straight Offset Binary MSB LSB
Bipolar		
5.000000V	0000000000000000	1111111111111111
4.999981V	000000000000000*	111111111111111*
4.999962V	0000000000000001	1111111111111110
+0.000038V	0111111111111111	1000000000000000
+0.000019V	**********	**********
0.000000V	1000000000000000	0111111111111111
–4.999924V	1111111111111110	0000000000000001
–4.999943V	111111111111111*	000000000000000*
–4.999962V	1111111111111111	0000000000000000
Unipolar		
9.999962V	0000000000000000	1111111111111111
9.999943V	000000000000000*	111111111111111*
9.999924V	0000000000000001	1111111111111110
+5.000000V	0111111111111111	1000000000000000
+4.999981V	**********	**********
+4.999962V	1000000000000000	0111111111111111
+0.000038V	1111111111111110	0000000000000001
+0.000019V	111111111111111*	000000000000000*
+0.000000V	1111111111111111	0000000000000000

Figure 2. Output Coding for the ADC5020/ADC5030.

Timing Considerations

The timing diagram in Figure 3 shows the timing characteristics of the ADC5020/ADC5030 A/D converter. Upon a low-to-high transition of the Trigger Input, the end of conversion (EOC) line also switches high. The EOC line in turn switches the internal sample-and-hold amplifier to Hold mode; the S/H amplifier remains in Hold mode for the 5 µs duration of the A/D conversion period. At the end of the 5 µs A/D conversion period, the EOC line goes low and switches the sample-and-hold amplifier to Sample mode. At the 144 kHz throughput rate shown in Figure 3, the sample-and-hold amplifier then has 1.9 µs to sample (acquire) a new signal level for the next conversion cycle. The TTL-level Trigger input should have a minimum pulse width of 50 ns. Note that the data for a given conversion cycle becomes valid approximately 20 ns before the respective high-to-low transition of the EOC line.

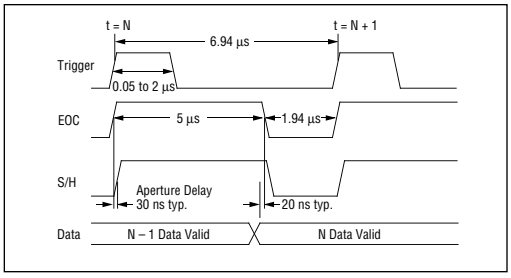


Figure 3. ADC5020/ADC5030 Timing Diagram.

Layout Considerations

Because of the ADC5020/ADC5030 A/D converter's extremely high resolution, it is necessary to pay careful attention to the printed circuit layout for the device. It is, for example, important to separate the analog and digital grounds and to return them separately to the system power supply. Digital grounds are often noisy or "glitchy", and these glitches can have adverse effects on the performance of the ADC5020/ADC5030 if they are introduced to the analog portions of the A/D converter's circuitry. At 18-bit resolution, the size of the voltage step between one code transition and the succeeding one is only 38 µV, so it is evident that any noise in the analog ground return can result in erroneous or missing codes. It is therefore important to configure a low-impedance ground-plane return on the printed circuit board. Note that the ground-potential metal case used for the ADC5020/ADC5030 provides shielding against electromagnetic interference on five sides and against electrostatic interference on six sides.

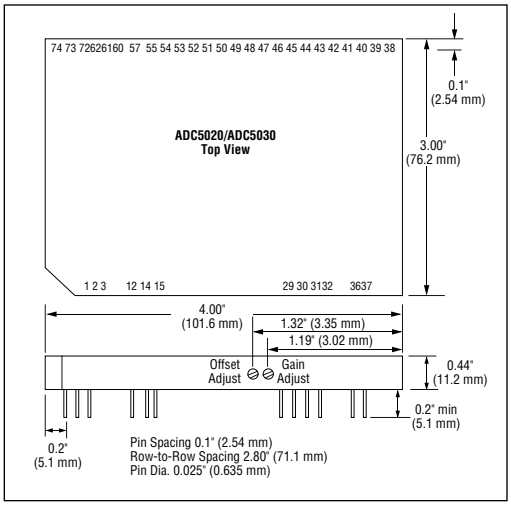


Figure 4. ADC5020/ADC5030 Outline Drawing & Pinouts.

PRINCIPLES OF OPERATION

To understand the operating principles of the ADC5020/ADC5030 A/D converter, refer to Figure 5. The simplified block diagrams in paths a, b, and c in Figure 5 illustrate the three successive passes in the sub-ranging conversion scheme of the ADC5020/ADC5030. For all three passes, the lines labeled "From Input" come either from the output of the sample-and-hold amplifier (in the ADC5020) or from the output of the input buffer amplifier (in the ADC5030). All three passes use the same 8-bit flash A/D converter with the first and second pass utilizing only the first six bits. In the first pass (a), a switched-gain amplifier attenuates the input signal by a factor of five. It thus converts the 10V full scale range of the input to the 2V full scale range of the 6-bit flash A/D converter. The 6-bit A/D converter then digitizes the six MSBs of the input signal. The outputs of the A/D converter drive the six MSBs of the D/A converter. The six output lines of the A/D converter are actually latched into the logic circuitry of a specialized gate array, which drives the input lines of the D/A converter.

In the second pass (b), a difference amplifier subtracts the D/A converter's output voltage from the input voltage, then amplifies this difference by a factor of 3.2. The switched-gain amplifier now has a gain of two, and thus amplifies the difference voltage further. The output of the switched-gain amplifier again provides the input signal for the 8-bit flash A/D converter. The A/D converter's outputs are latched into the gate array which supplies the next lower-order bits of the D/A converter. In the gate array, the A/D converter's MSB in the second pass "overlaps" the LSB from the first pass. The resolution of the A/D conversion in the second pass is thus 11 bits (not 12).

In the third pass (c), the gain-of-3.2 difference amplifier subtracts the D/A converter's output voltage from the input voltage. In this pass, an amplifier with a gain of 32 provides additional amplification of the difference signal. The eight outputs of the 8-bit flash A/D converter are latched into the gate array; the MSB of this conversion cycle "overlaps" the LSB of the previous cycle. The effective resolution of the conversion is thus 6 + 5 + 7, or 18 bits. Using the "overlap" structure, logic circuitry in the gate array adds the digital words produced in the three passes and produces the corrected output word. This digital error-correction technique thus provides an output word that is accurate and linear to within the full resolution of the A/D converter. The method corrects for any gain and linearity errors in the amplifying circuitry, as well as in the 8-bit flash A/D

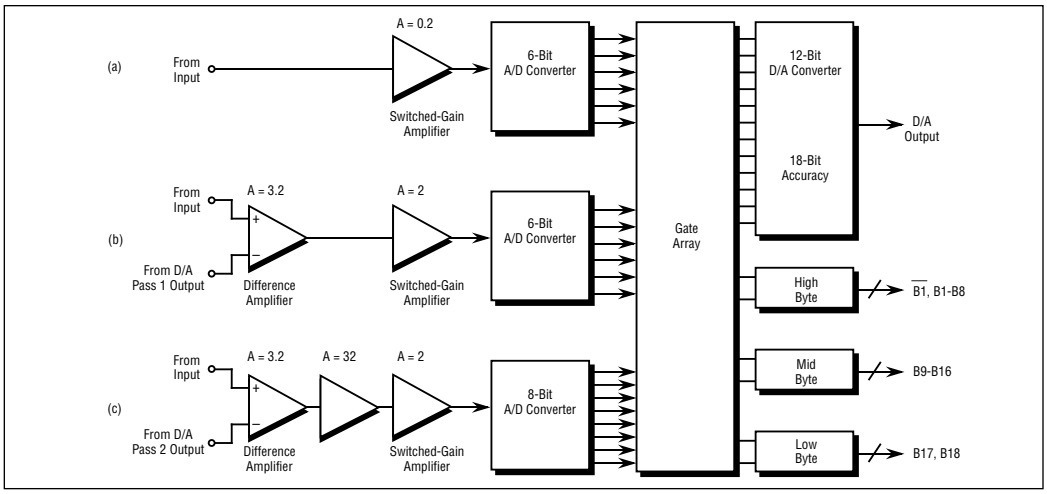


Figure 5. Operating Principle of the ADC5020/ADC5030.

converter. Without the error-correction technique, it would be necessary that all the components in the ADC5020/ ADC5030 — the difference amplifier, the switched-gain amplifier, and the 8-bit flash A/D converter — be accurate and linear to an 18-bit level. While such a design might be possible to realize on a laboratory benchtop, it would be clearly impractical to achieve in production. The key to the ADC5020/ ADC5030's conversion scheme is the 18-bit-linear D/A converter, which serves as a reference element for the conversion passes as well as for the error-correction mechanism.

The ADC5020/ADC5030 has a tri-state output structure. Users can enable the eight MSBs, the eight middle bits, the two LSBs, or all bits by using the High-Byte Enable, Mid-Byte Enable, or the Low-Byte Enable pins (all three are active low). This feature makes it possible to transfer data from the ADC5020/ADC5030 to an 8-bit microprocessor bus. However, to prevent the coupling of high frequency noise from the microprocessor bus into the A/D converter, the output data must be buffered (see Figure 6).

TYPICAL APPLICATION

Figure 6 shows a typical application circuit for the ADC5020/ADC5030 A/D converter. This circuit provides simultaneous sampling for two professional audio analog-input channels. Simultaneous sampling is a necessity in conversion systems in which the phase, as well as amplitude relationship between different signals, is an important parameter. One example is in seismic measurements where it is crucial to know the phase relationship between the signals generated by different sensors. Another application where the phase and amplitude relationships are critical is professional digital audio, described in Figure 6. This application circuit performs simultaneous sampling by "freezing" the signal levels of both analog-input channels at the same instant of time. The amplitude relationship is maintained by the input Programmable Gain Amplifiers that are operated differentially to eliminate the possibility of errors arising from common mode voltages. The Anti-Aliasing Filters of Figure 6 reduce the out-of-band products coming in the front end that would mix with the sampling frequency and create audible in-band by-products.

A pair of low-noise, low-distortion Sample-and-Hold Amplifiers that have been optimized for audio bandwidths to obtain 18-bit linearity, Analogic's SHA2410s simultaneously sample the analog inputs and multiplex these signal levels to the buffer stage. A high input impedance buffer stage is required following a multiplexer to minimize the inherent nonlinearities of the switch-on-resistance with respect to current variations. The ADC5020 sequentially digitizes the two channels and transmits the buffered data to the minicomputer or microprocessor. The data buffer is necessary to prevent the coupling of high frequency noise from the processor bus into the A/D converters. Because the SHA2410s provide the sample-and-hold function in this circuit, the ADC5030, which does not include a sample-and-hold amplifier, is an appropriate choice.

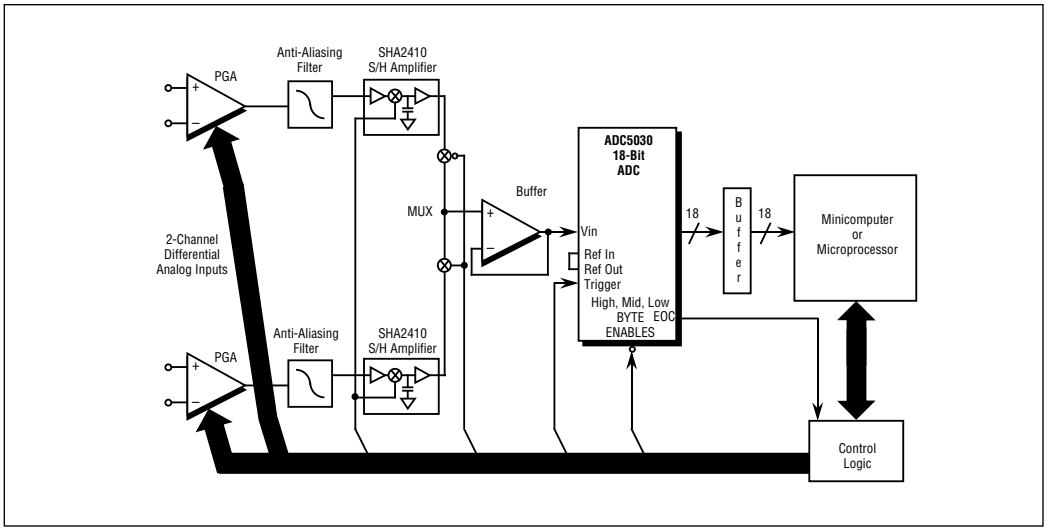


Figure 6. Typical Application Circuit for the ADC5030.

Ordering Guide

ADC50 –M

20	On-board S/H
30	Buffered input
1	0 to +10V input
2	±10V input
4	±5V input
S	Straight data
C	Complementary data

DC-to-DC Converter.....**SP7008**