

P455-A01 DT SKU7 Board

P455-A01, G71-GT2, 512MB 16Mx32 GDDR3 (700Mhz),
DVI - I - DL, DVI - I - DL, HDTV w/ HDCP

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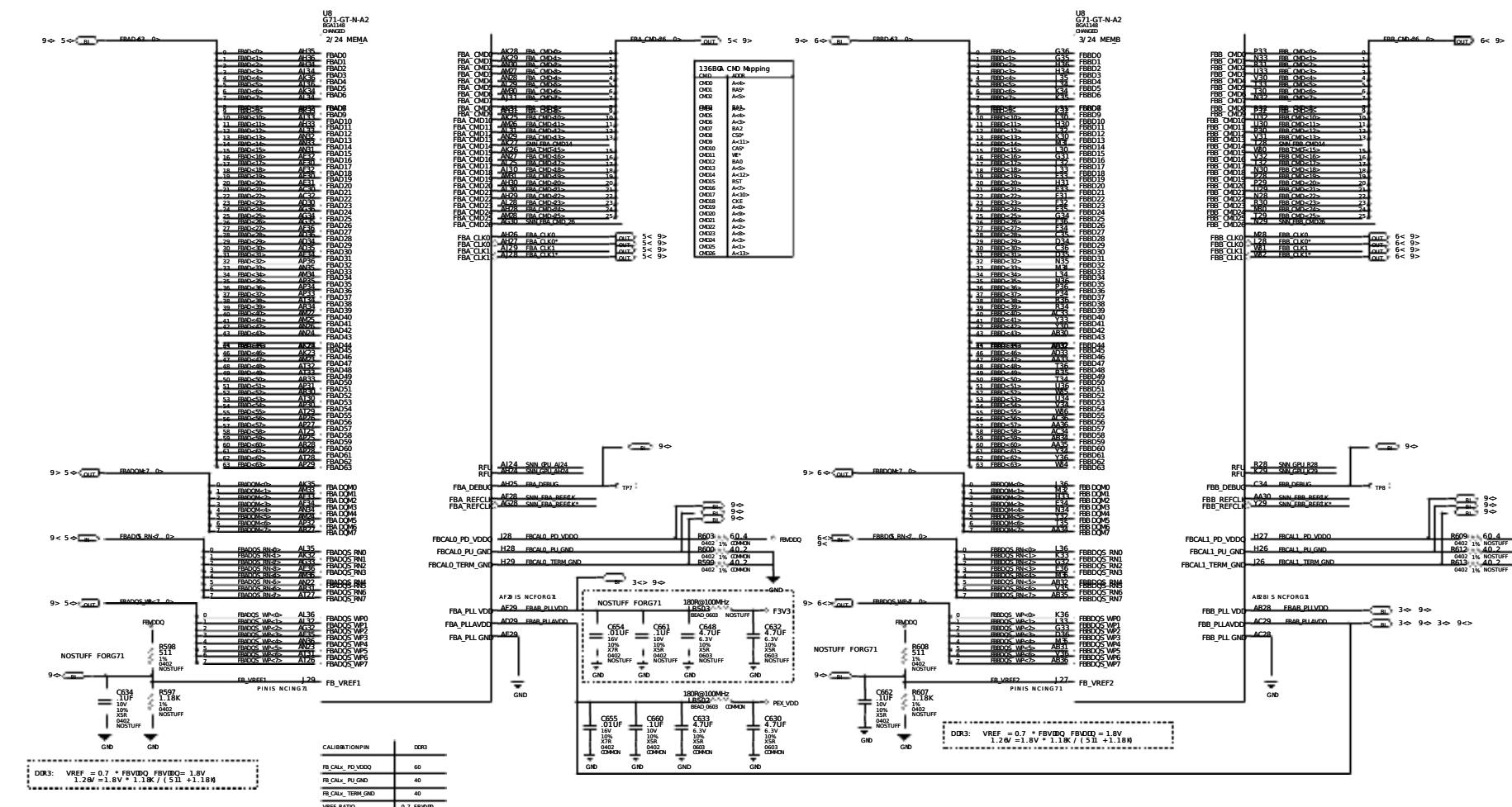
REVISION HISTORY:

X1 RevA: Initial Release

SKU	VARIANT	NPN	ASSEMBLY
B	BASE	600-10455-base-100	P455 - BASE LEVEL. GENERIC SCHEMATIC ONLY. COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL.
1	SKU0000	600-10455-0000100	G71-GT - 256MB 8Mx32 DDR3, DVI-I-DL + DVI-I-DL + HDTV, 450/700 MHz
2	SKU0002	600-10455-00002100	G71-GT - 256MB 8Mx32 DDR3, DVI-I-DL + DVI-I-DL + HDTV, 450/700 MHz for Dell HNA
3	SKU0500	600-50455-0500100	G71GL-U - 256MB 8Mx32 DDR3, DV-I-DL +DVI-I-DL +HDTV, 375/600 MHz
4	SKU0501	600-50455-0500100	G71GL-SID - 256MB 8Mx32 DDR3, DV-I-DL +DVI-I-DL +HDTV, 375/600 MHz
5	SKU0505	600-50455-05005100	G71GT2-H - 512MB 16Mx32 GDDR3, DVI-I-DL + DVI-I-DL + HDTV, 550/700 MHz
6	SKU0007	600-10455-00007100	G71GT2-H 512MB 16Mx32, DDR3, DVI-I-DL + DVI-I-DL + HDTV, 550/700 MHz
7	<UNDEF NED>	<UNDEF NED>	<UNDEF NED>
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9	<UNDEF NED>	<UNDEF NED>	<UNDEF NED>
10	<UNDEF NED>	<UNDEF NED>	<UNDEF NED>
11	<UNDEF NED>	<UNDEF NED>	<UNDEF NED>
12	<UNDEF NED>	<UNDEF NED>	<UNDEF NED>
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14	<UNDEF NED>	<UNDEF NED>	<UNDEF NED>
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ID	design
NAME	I.Farasati
PAGE	1 OF 24
DATE	30-JUN-2006

Page3: MEMORY: GPU Partition A/B



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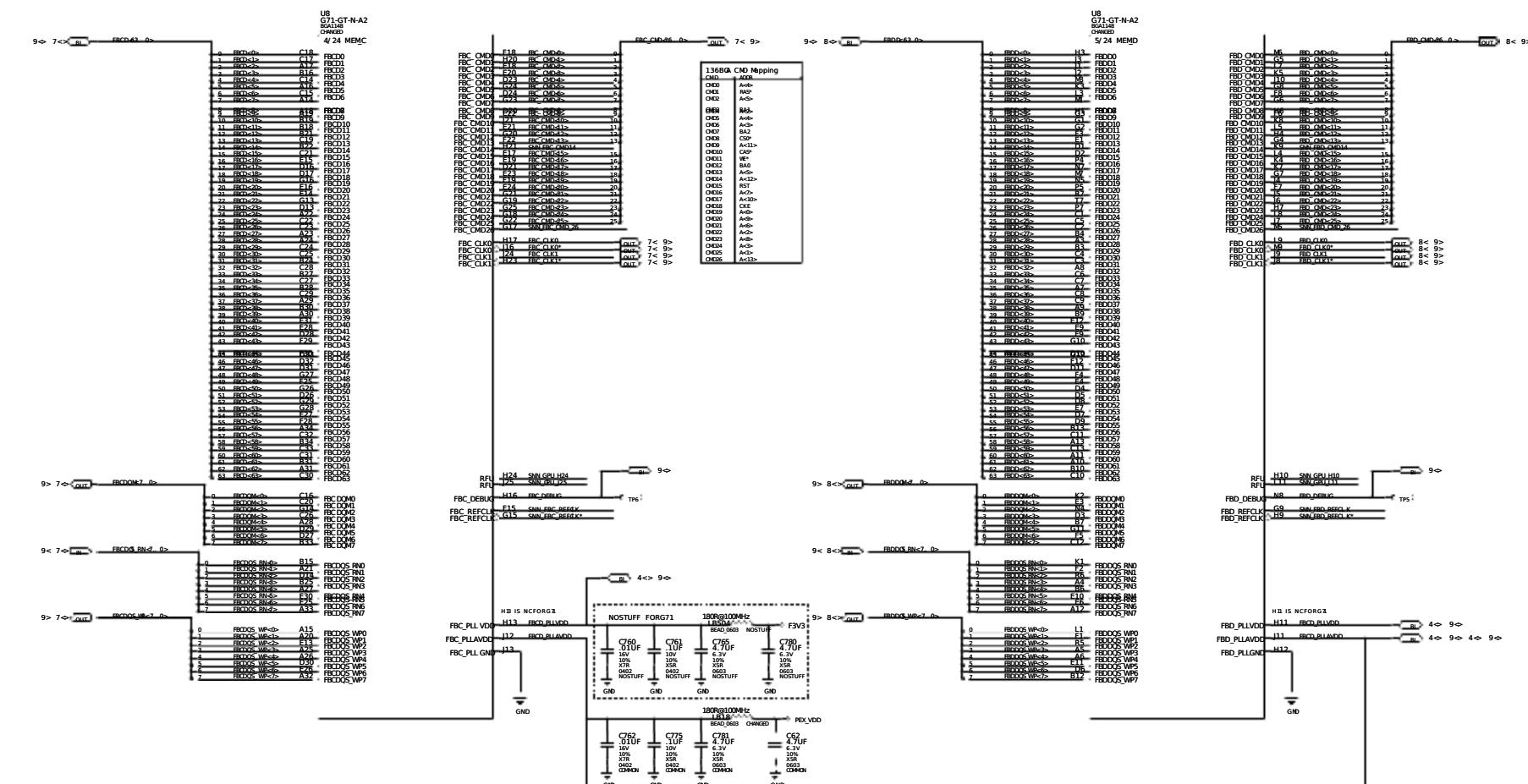
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J.D. design PAGE 3 OF 24
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Page4: MEMORY: GPU Partition C/D



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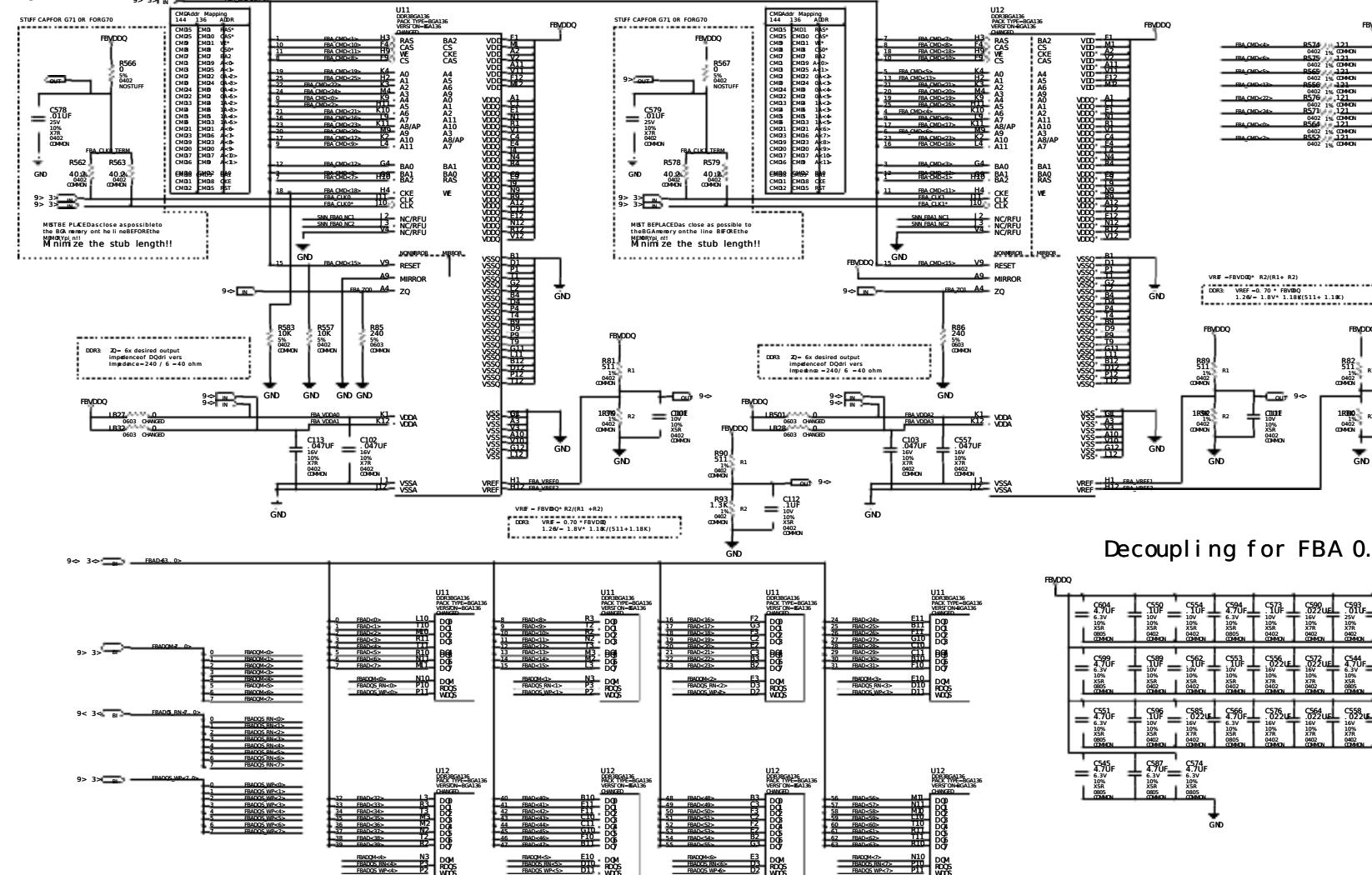
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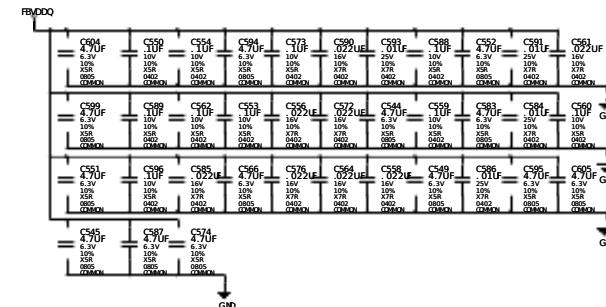
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Page5: FBA Partition



Decoupling for FBA 0..31



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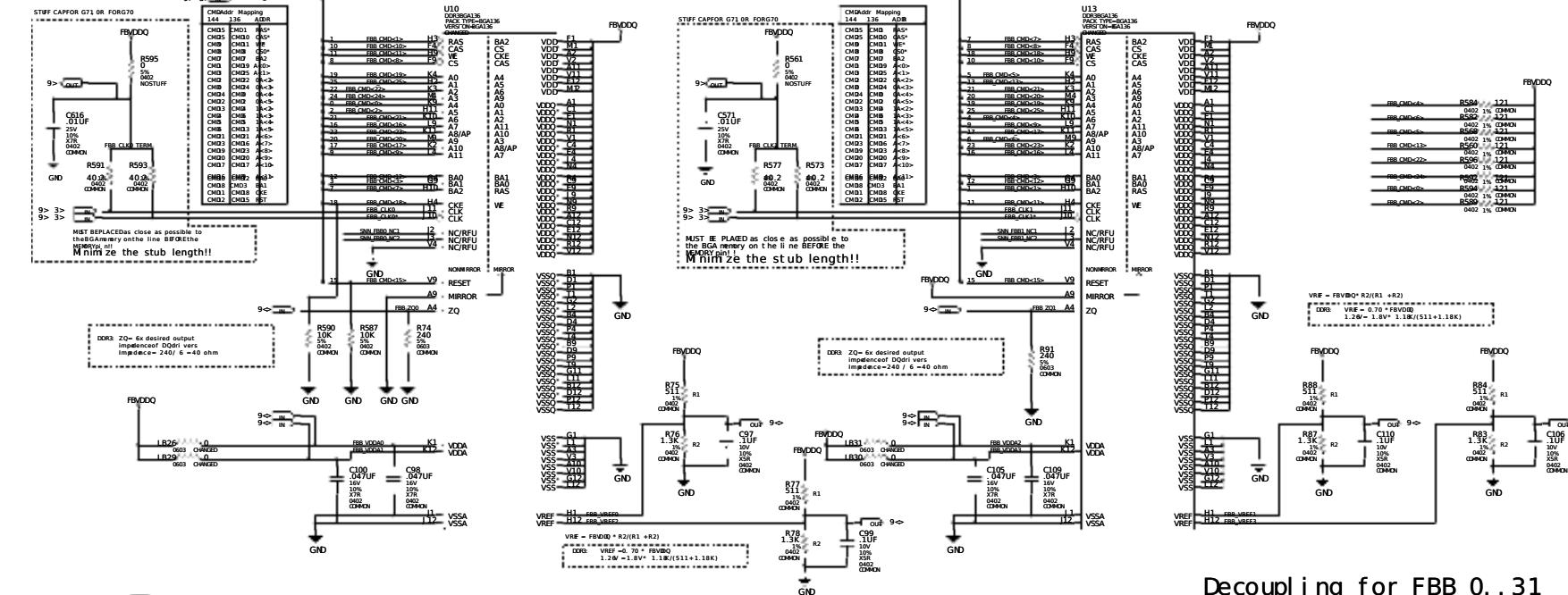
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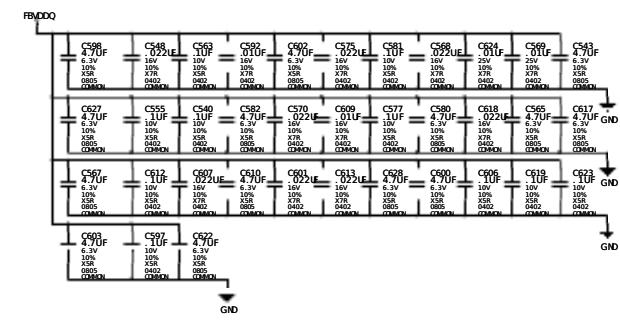
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NAME I.Farasati DATE 13-OCT-2006

Page6: FBB Partition



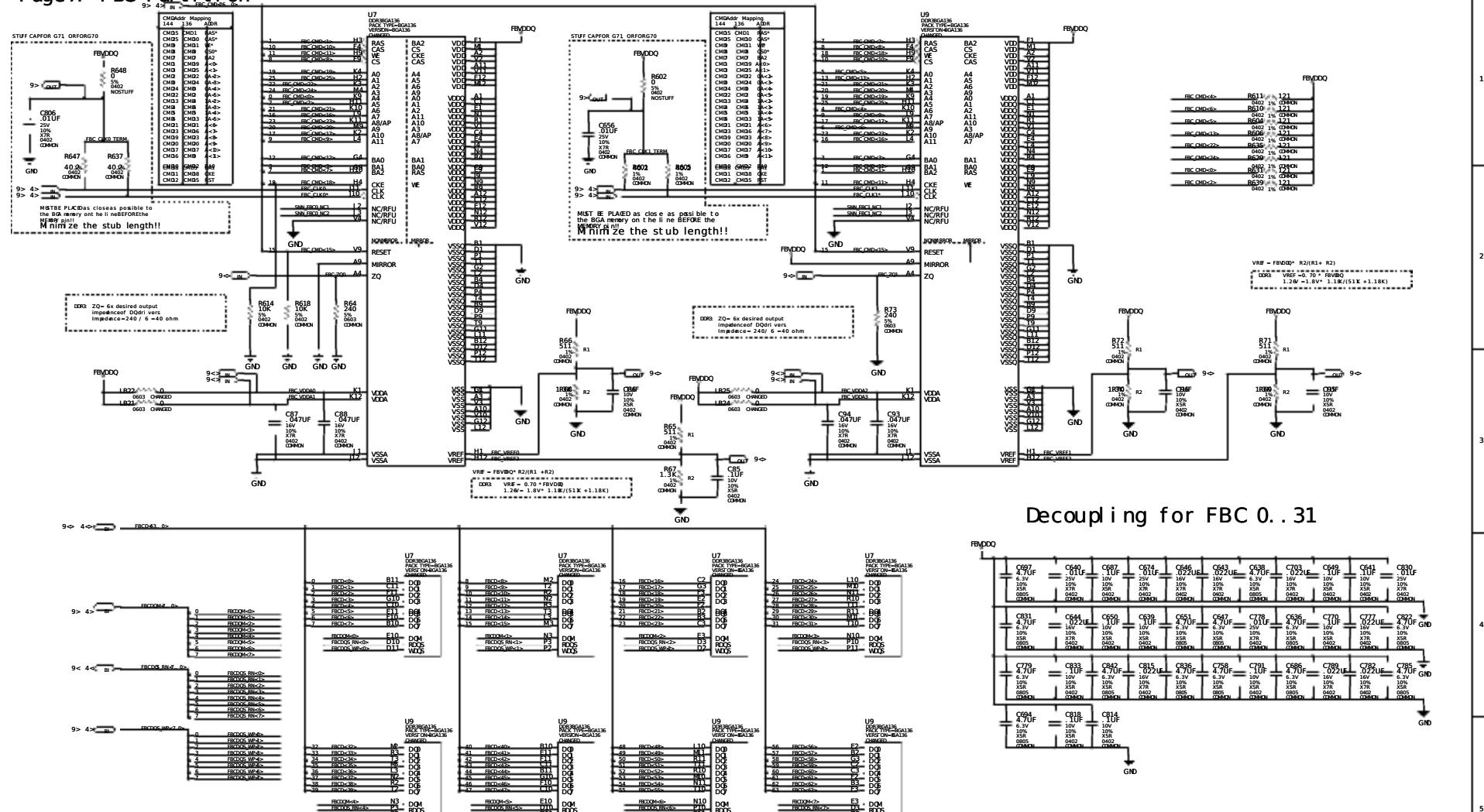
Decoupling for FBB 0..31



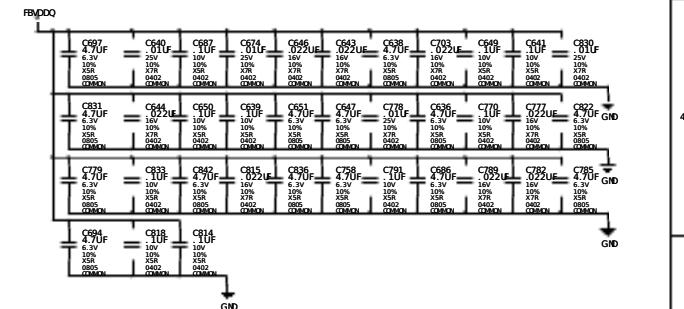
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Page 7: FBC Partition



Decoupling for FBC 0 . 31



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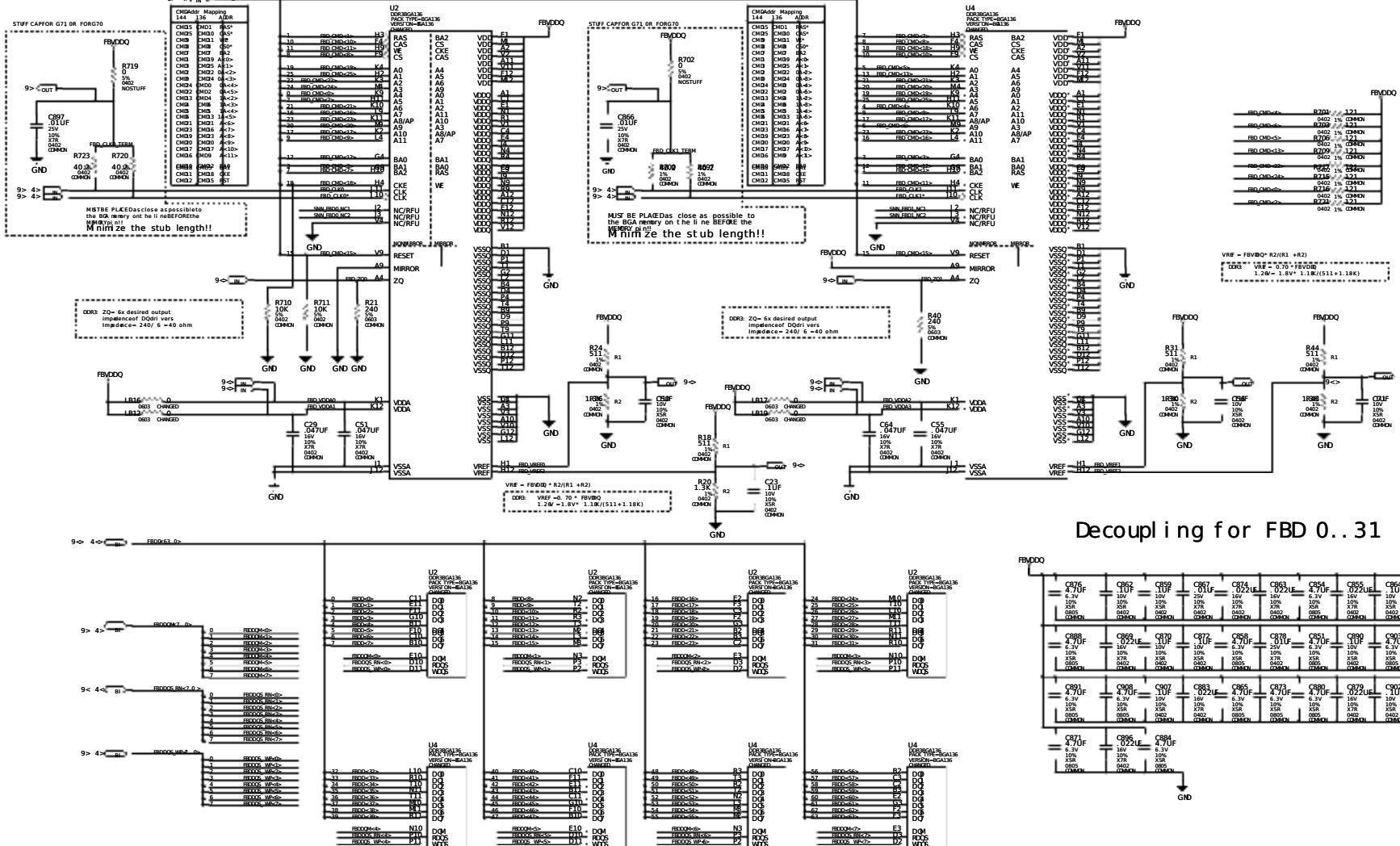
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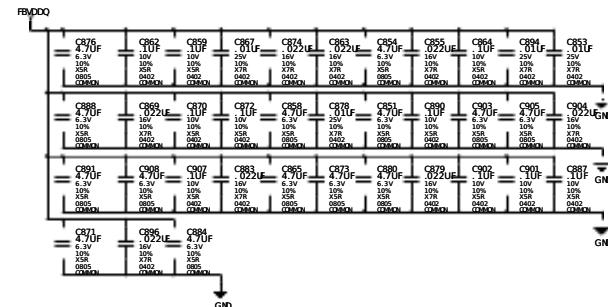
* ASSEMBLY
PAGE DETAIL
FBC Partition

G71GT2H 512N 16Mx32 QD83, DVI-I-DL + DVI-I-DL + HDV, w/HDP, 550/700 MHz

Page8: FBD Partition



Decoupling for FBD 0..31



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Page9: FrameBuffer Net Properties

NET RULES for FrameBuffer A/B					
NET	NV_CRTI_CAL	NV_I_IMPEDANCE	DIFFPAIR		
5< 3> OUT FBA_CLK0	FBA_CLK0	1	SOOCIE	FBA_CLK0	
5< 3> OUT FBA_CLK0_TERM	FBA_CLK0_TERM	1	ACOAM		
5< 3> OUT FBA_CLK1	FBA_CLK1	1	SOOCIE	FBA_CLK1	
5< 3> OUT FBA_CLK1_TERM	FBA_CLK1_TERM	1	ACOAM	FBA_CLK1	
5< 3> OUT FBA_CLK26_D0	FBA_CLK26_D0	1	SOOCIE		
5< 3> OUT FBA_CLK26_D1	FBA_CLK26_D1	1	SOOCIE		
5< 3> OUT FBA_CLK26_D2	FBA_CLK26_D2	1	SOOCIE		
5< 3> OUT FBA_CLK26_D3	FBA_CLK26_D3	1	SOOCIE		
5< 3> OUT FBA_CLK26_D4	FBA_CLK26_D4	1	SOOCIE		
5< 3> OUT FBA_CLK26_D5	FBA_CLK26_D5	1	SOOCIE		
5< 3> OUT FBA_CLK26_D6	FBA_CLK26_D6	1	SOOCIE		
5< 3> OUT FBA_CLK26_D7	FBA_CLK26_D7	1	SOOCIE		
6< 3> OUT FBA_CLK4	FBA_CLK4	1	SOOCIE	FBA_CLK4	
6< 3> OUT FBA_CLK4_TERM	FBA_CLK4_TERM	1	ACOAM		
6< 3> OUT FBA_DFB46_D0	FBA_DFB46_D0	1	SOOCIE		
6< 3> OUT FBA_DFB46_D1	FBA_DFB46_D1	1	SOOCIE		
6< 3> OUT FBA_DFB46_D2	FBA_DFB46_D2	1	SOOCIE		
6< 3> OUT FBA_DFB46_D3	FBA_DFB46_D3	1	SOOCIE		
6< 3> OUT FBA_DFB46_D4	FBA_DFB46_D4	1	SOOCIE		
6< 3> OUT FBA_DFB46_D5	FBA_DFB46_D5	1	SOOCIE		
6< 3> OUT FBA_DFB46_D6	FBA_DFB46_D6	1	SOOCIE		
6< 3> OUT FBA_DFB46_D7	FBA_DFB46_D7	1	SOOCIE		
NET	NV_CRTI_CAL	NV_I_IMPEDANCE	DIFFPAIR		
3< 3> BI FBC_VREF0	FBC_VREF0	1	SOOCIE	FBC_VREF0	
3< 3> BI FBC_VREF1	FBC_VREF1	1	SOOCIE	FBC_VREF1	
3< 3> BI FBC_VREF2	FBC_VREF2	1	SOOCIE	FBC_VREF2	
3< 3> BI FBC_VREF3	FBC_VREF3	1	SOOCIE	FBC_VREF3	
3< 3> BI FBA_Z00	FBA_Z00	1	SOOCIE	FBA_Z00	
3< 3> BI FBA_Z01	FBA_Z01	1	SOOCIE	FBA_Z01	
3< 3> BI FBA_VDDA0	FBA_VDDA0	1	SOOCIE	FBA_VDDA0	
3< 3> BI FBA_VDDA1	FBA_VDDA1	1	SOOCIE	FBA_VDDA1	
3< 3> BI FBA_VDDA2	FBA_VDDA2	1	SOOCIE	FBA_VDDA2	
3< 3> BI FBA_VDDA3	FBA_VDDA3	1	SOOCIE	FBA_VDDA3	
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3< 3> BI FBA_VREF2	FBA_VREF2	1	SOOCIE	FBA_VREF2	
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5< 3> BI FBA_VDD0	FBA_VDD0	1	SOOCIE	FBA_VDD0	
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5< 3> BI FBA_VDD2	FBA_VDD2	1	SOOCIE	FBA_VDD2	
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5< 3> BI FBA_VREF2	FBA_VREF2	1	SOOCIE	FBA_VREF2	
5< 3> BI FBA_VREF3	FBA_VREF3	1	SOOCIE	FBA_VREF3	
6< 3> BI FBB_Z00	FBB_Z00	1	SOOCIE	FBB_Z00	
6< 3> BI FBB_Z01	FBB_Z01	1	SOOCIE	FBB_Z01	
6< 3> BI FBB_VDD0	FBB_VDD0	1	SOOCIE	FBB_VDD0	
6< 3> BI FBB_VDD1	FBB_VDD1	1	SOOCIE	FBB_VDD1	
6< 3> BI FBB_VDD2	FBB_VDD2	1	SOOCIE	FBB_VDD2	
6< 3> BI FBB_VDD3	FBB_VDD3	1	SOOCIE	FBB_VDD3	
6< 3> BI FBB_VREF0	FBB_VREF0	1	SOOCIE	FBB_VREF0	
6< 3> BI FBB_VREF1	FBB_VREF1	1	SOOCIE	FBB_VREF1	
6< 3> BI FBB_VREF2	FBB_VREF2	1	SOOCIE	FBB_VREF2	
6< 3> BI FBB_VREF3	FBB_VREF3	1	SOOCIE	FBB_VREF3	
3< 3> BI FB_UVREF1	FB_UVREF1	1	SOOCIE	FB_UVREF1	
3< 3> BI FB_UVREF2	FB_UVREF2	1	SOOCIE	FB_UVREF2	

NET RULES for FrameBuffer C/D					
NET	NV_CRTI_CAL	NV_I_IMPEDANCE	DIFFFPAIR		
7< 4> OUT FBC_CLK0	FBC_CLK0	1	SOOCIE	FBC_CLK0	
7< 4> OUT FBC_CLK0_TERM	FBC_CLK0_TERM	1	ACOAM		
7< 4> OUT FBC_CLK1	FBC_CLK1	1	SOOCIE	FBC_CLK1	
7< 4> OUT FBC_CLK1_TERM	FBC_CLK1_TERM	1	ACOAM	FBC_CLK1	
7< 4> OUT FBC_CLK26_D0	FBC_CLK26_D0	1	SOOCIE		
7< 4> OUT FBC_CLK26_D1	FBC_CLK26_D1	1	SOOCIE		
7< 4> OUT FBC_CLK26_D2	FBC_CLK26_D2	1	SOOCIE		
7< 4> OUT FBC_CLK26_D3	FBC_CLK26_D3	1	SOOCIE		
7< 4> OUT FBC_CLK26_D4	FBC_CLK26_D4	1	SOOCIE		
7< 4> OUT FBC_CLK26_D5	FBC_CLK26_D5	1	SOOCIE		
7< 4> OUT FBC_CLK26_D6	FBC_CLK26_D6	1	SOOCIE		
7< 4> OUT FBC_CLK26_D7	FBC_CLK26_D7	1	SOOCIE		
8< 4> OUT FBD_CLK0	FBD_CLK0	1	SOOCIE	FBD_CLK0	
8< 4> OUT FBD_CLK0_TERM	FBD_CLK0_TERM	1	ACOAM		
8< 4> OUT FBD_CLK1	FBD_CLK1	1	SOOCIE	FBD_CLK1	
8< 4> OUT FBD_CLK1_TERM	FBD_CLK1_TERM	1	ACOAM	FBD_CLK1	
8< 4> OUT FBD_DEBUG	FBD_DEBUG	1	SOOCIE		
8< 4> OUT FBD_DEBUG	FBD_DEBUG	1	SOOCIE		
NET	VOLTAGE	MAX_CURR_BNT	MN_WDT_H		
4< 3> BI FB_S1_VDD	FB_S1_VDD	3.3V	0.04A	12MS	
4< 3> BI FB_S1_VDD0	FB_S1_VDD0	3.3V	0.12A	12MS	
FB_VREF0	1.26V	0.02A			
FB_VREF1	1.26V	0.02A			
FB_VREF2	1.26V	0.02A			
FB_VREF3	1.26V	0.02A			
FB_Z00	1.26V	0.02A			
FB_Z01	1.26V	0.02A			
FB_VDD0	1.8V	0.02A			
FB_VDD1	1.8V	0.02A			
FB_VDD2	1.8V	0.02A			
FB_VDD3	1.8V	0.02A			
FB_VREF0	1.26V	0.02A			
FB_VREF1	1.26V	0.02A			
FB_VREF2	1.26V	0.02A			
FB_VREF3	1.26V	0.02A			
FB_Z00	1.26V	0.02A			
FB_Z01	1.26V	0.02A			
FB_VDD0	1.8V	0.02A			
FB_VDD1	1.8V	0.02A			
FB_VDD2	1.8V	0.02A			
FB_VDD3	1.8V	0.02A			
FB_VREF0	1.26V	0.02A			
FB_VREF1	1.26V	0.02A			
FB_VREF2	1.26V	0.02A			
FB_VREF3	1.26V	0.02A			
FB_Z00	1.26V	0.02A			
FB_Z01	1.26V	0.02A			
FB_VDD0	1.8V	0.02A			
FB_VDD1	1.8V	0.02A			
FB_VDD2	1.8V	0.02A			
FB_VDD3	1.8V	0.02A			
FB_UVREF1	1.26V	0.02A			
FB_UVREF2	1.26V	0.02A			

ASSEMBLY G71GT2-H_512MB_16M32_D083_DVI_I-DL + DVI-II-DL + HDPW_550/700 MHz

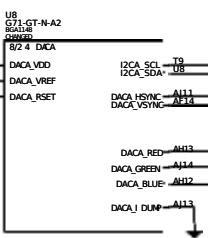
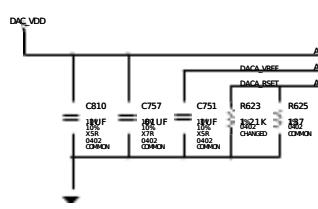
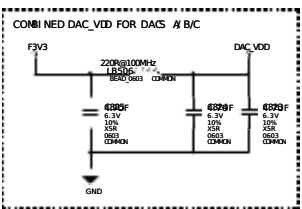
PAGE DETAIL FrameBuffer Net Properties

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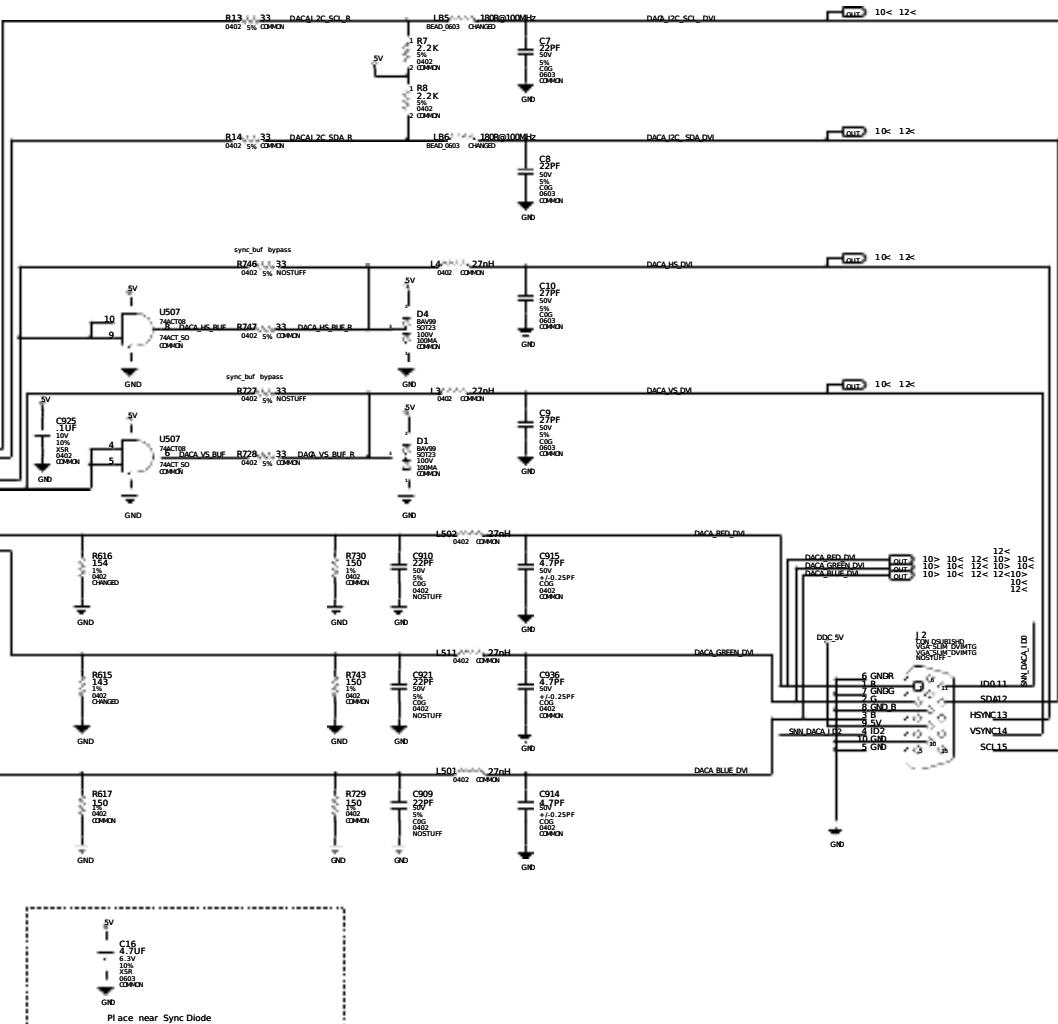
Page10: DACA Interface



DACA NET RULES

NET	NV_CRT1_CAL	NV_I impedance	ECSet
DACA_RED	1	20Ωm	DAC_RED_CST
DACA_GREEN	1	20Ωm	DAC_GREEN_CST
DACA_BLUE	1	20Ωm	DAC_BLUE_CST
DACA_HSYNC	2	50Ωm	
DACA_VSYNC	2	50Ωm	
DACA_HS_B	2	50Ωm	
DACA_HS_E	2	50Ωm	
DACA_HS_D	2	50Ωm	
DACA_HS_E	2	50Ωm	
DAA_DC_SCL			
DAA_DC_SD			
DAA_DC_SCL_R			
DAA_DC_SD_R			
DAA_DC_SCL_DVI			
DAA_DC_SD_DVI			

NET	VOLTAGE	MAX CURRENT	MIN WIDTH
DAC_VDD	3.3V	0.25A	16μm



* ASSEMBLY PAGE DETAIL
 G71 GT2-H S12N 16M32 QD03, DVI-I-DL + DVI-I -DL + HDTV, w/HDCP, 550/700 MHz
 DACI Interface

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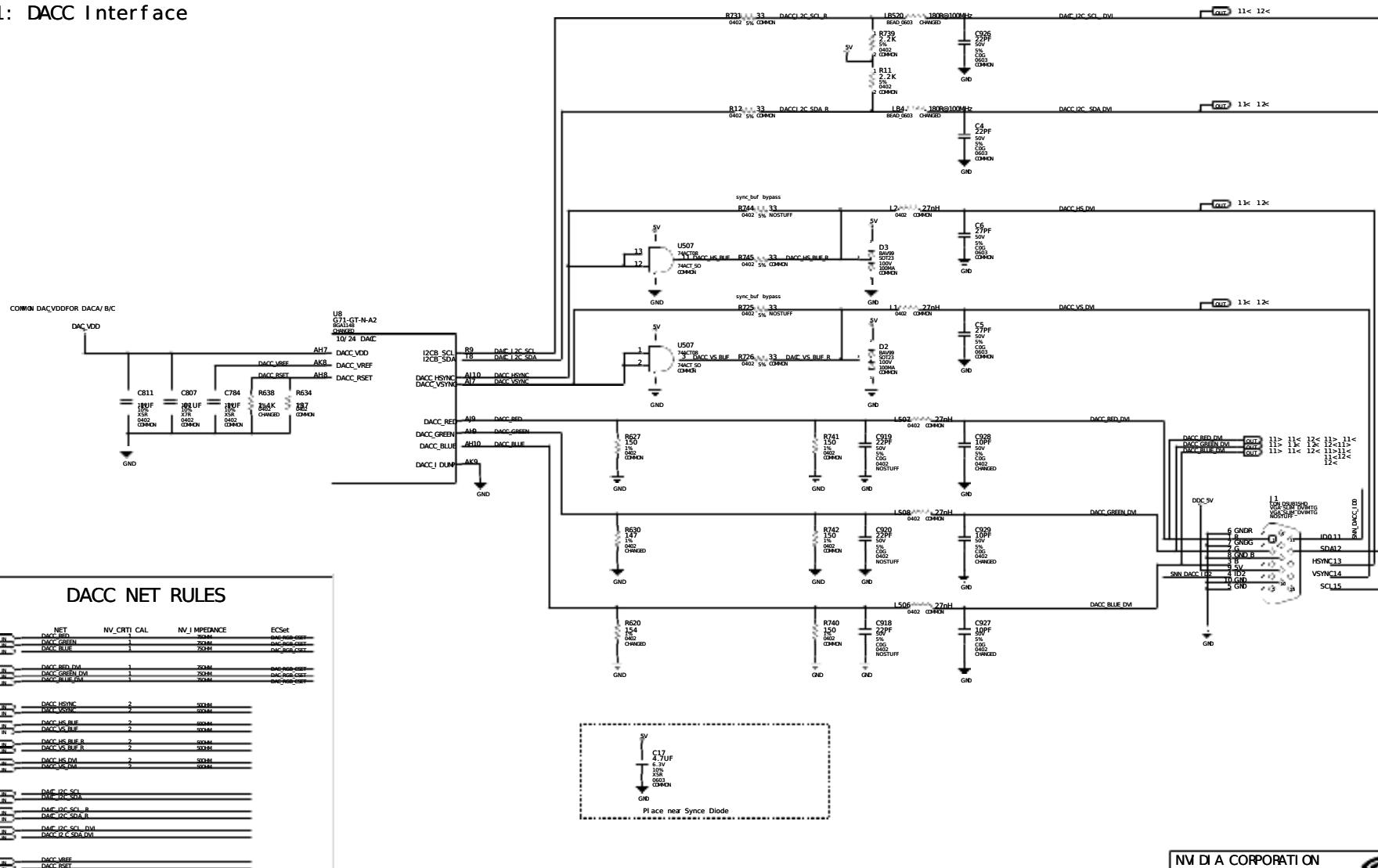
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Page11: DACC Interface



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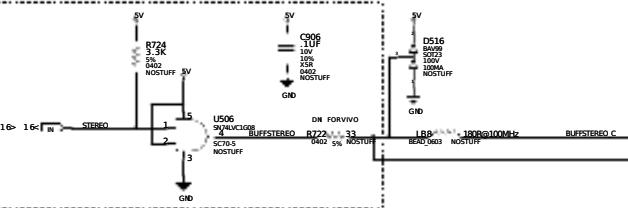
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NV_PN 600-10455-0007-100_A
J.D. design PAGE 111 OF 24
NAME I.Farasati DATE 10-JUN-2006

* ASSEMBLY PAGE DETAIL
G71GT2-H 512B 16Mx32 QDRI, DVI-I-DL + DVI-I-DL + HDTV, w/HDCP, 550/700 MHz
DACCI interface

Page13: DACB and Stereo Interface

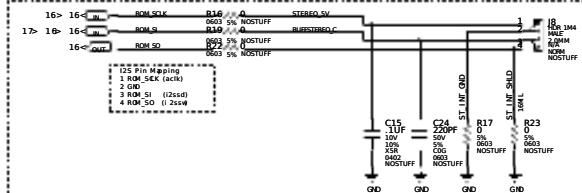
Stereo 3D



Stereo 5V



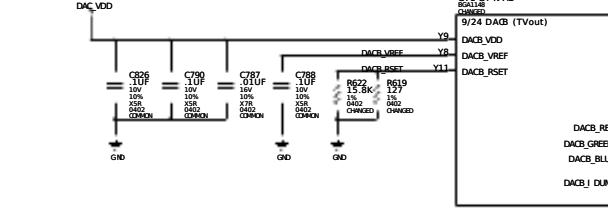
Internal Stereo Out/ I2S (Optional)



DACB & STEREO NET RULES

NET	NV_CRTI_CAL	NV_I impedance	ECSet
COUT	1	Z0MM	DACB_GND_CSET
IN	1	Z0MM	DACB_GND_CSET
CVBSIN	1	Z0MM	DACB_GND_CSET
MON_INOUT_C	1	Z0MM	DACB_GND_CSET
MON_BROUT_C	1	Z0MM	DACB_GND_CSET
MON_INOUT_C	1	Z0MM	DACB_GND_CSET
MON_BROUT_C	1	Z0MM	DACB_GND_CSET
CVBSYN	1	500M	1
MON_INOUT_C	1	500M	1
MON_BROUT_C	1	500M	1
CHROMIN	1	500M	1
CHROMIN_R	1	500M	1
I2CC_SCI_BUFFSTEREO_R	1	500M	1
MON_INOUT_STEREO	1	500M	1
BUFFSTEREO_C	1	500M	1
MON_GND	1	10MIL	1
DACB_VREF	1	10MIL	1
DACB_POT	1	10MIL	1
MON_GND	1	10MIL	1

COMMON DAC_VDD FOR DACA/B/C



9/24 DAB (TVout)



DACB_RED AA8, DACB_GREEN AA9, DACB_BLUE AA9, DACB_BIASET, DACB_I_DUM V8



14< 13< CVBSYN R729 1B CVBSYN R L510 1.8uH



FILTER CIRCUIT



fromcodec 0.56uH/270pF to DIN connector



ASSEMBLY PAGE DETAIL
G71GT2-H S12# 16M32 D03. DVI-I-DL + DVI-I-DL + HDTV. w/HDD. 550/700 MHz
D/A/Band Stereo Interface

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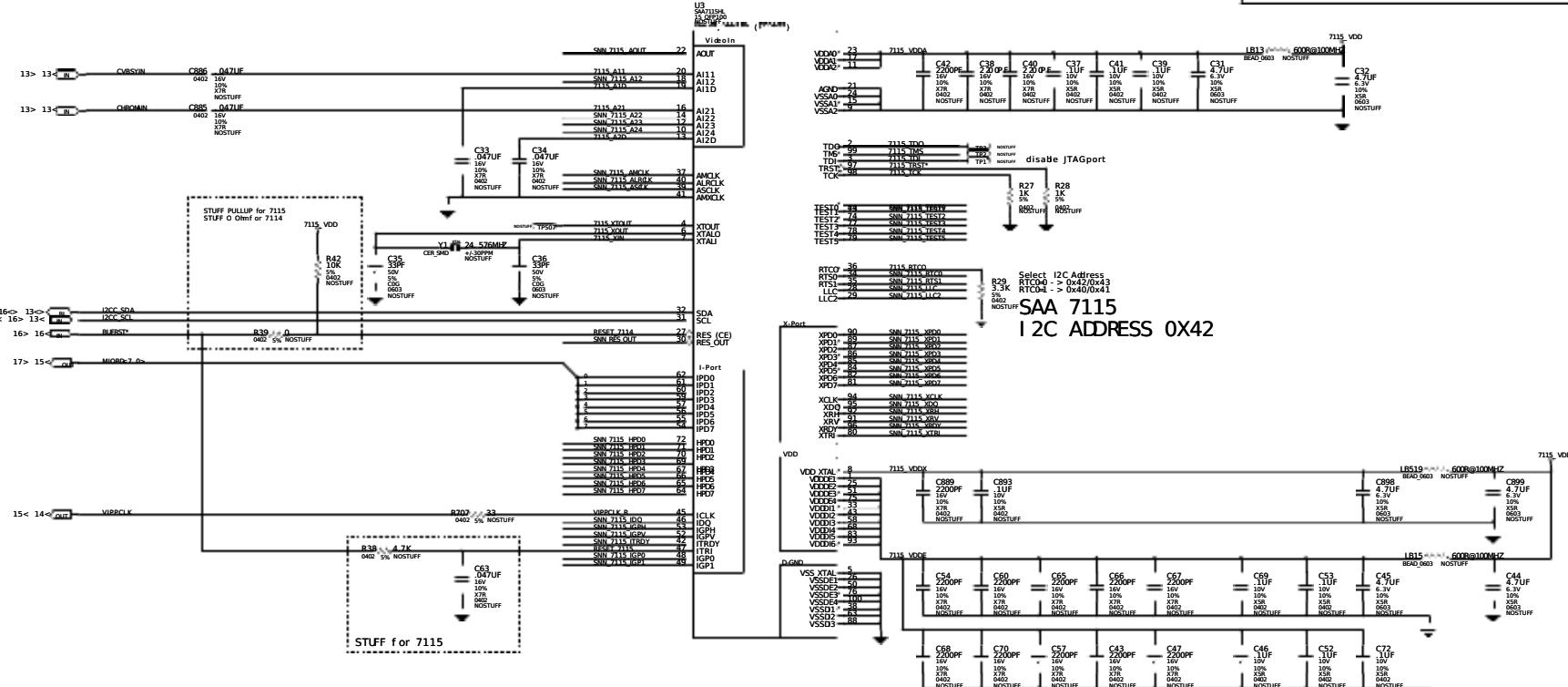
NV_PN 600-10455-0007-100_A
J.D. design PAGE 13 OF 24
NAME I.Farasati DATE 30-JUN-2006

G H

SAA7115 NET RULES

NET	NV_CRTI CAL	NV_I IMPEDANCE	DIFFPAR
VIPCLK_R	1	50Ωm	
1115_411	2	50Ωm	
1115_410	2	50Ωm	
1115_420	2	50Ωm	
1115_421	2	50Ωm	
1115_YOUT	1	50Ωm	
1115_XIN	1	50Ωm	
RESET_7115	2	50Ωm	
1115_RSTS	2	50Ωm	
1115_I2C	2	50Ωm	
1115_TSNS	2	50Ωm	
1115_XOUT			
NET	VOLTAGE	MAX_CUR_BAT	N N_WDT H
7115_VDD	3.3V	0.00A	10mA
7115_VDDX	3.3V	0.00A	10mA
7115_VDDY	3.3V	0.01A	16mA

VIDEO CAPTURE



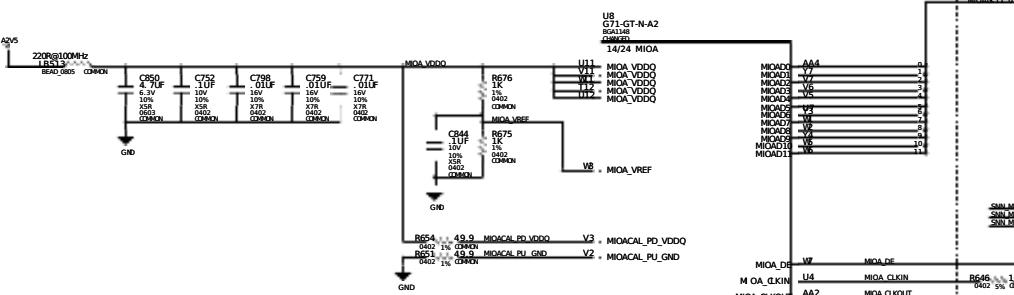
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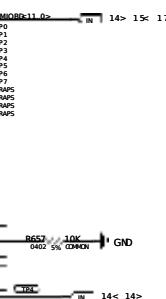
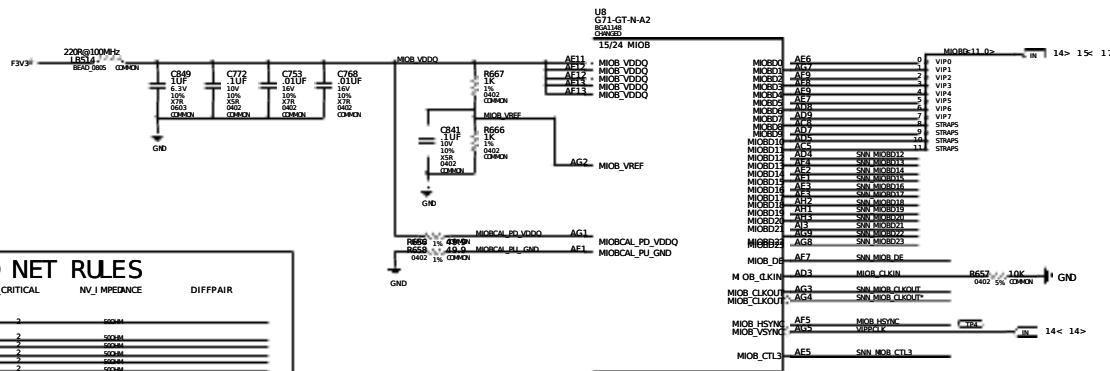
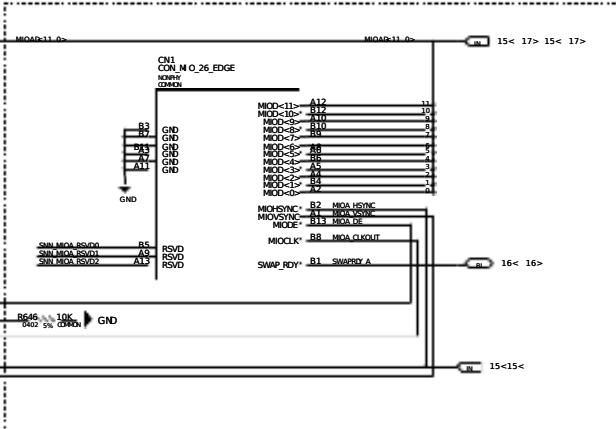
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J.D. design PAGE 14 OF 24
NAME: Farsatli DATE: 30-JUN-2006

Page 15: Multi-use I/O (MO) Interface



MO Feature Connector



MO NET RULES

NET NV_CRITICAL NV_IMPEDANCE DIFFPAIR

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
15<- MIOA-11_06	3	500m	
MIOA_CLKIN	2	500m	
MIOA_CLKOUT	2	500m	
MIOA_VSYNC	2	500m	
MIOA_VSSNC	2	500m	
17> MIOA-11_06	3	500m	
MIOB_CLKIN	2	500m	
MIOB_CLKOUT	2	500m	
MIOB_VSYNC	2	500m	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOA_VDDO	3.3V	0.80A	16W1
MIOA_VDD	1.65V	12mA	12W1
MIOA_VREF	1.65V	0.6V	12W1
MIOA_VSS	3.3V	0.03A	12W1
MIOA_VSSNC	3.3V	12mA	12W1
MIOA_VSSNC	0.0V	12mA	12W1

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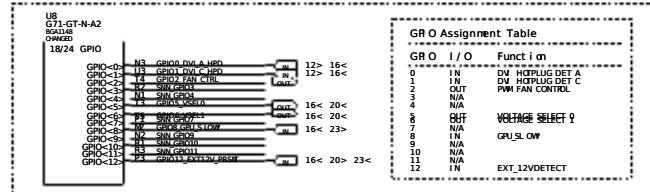
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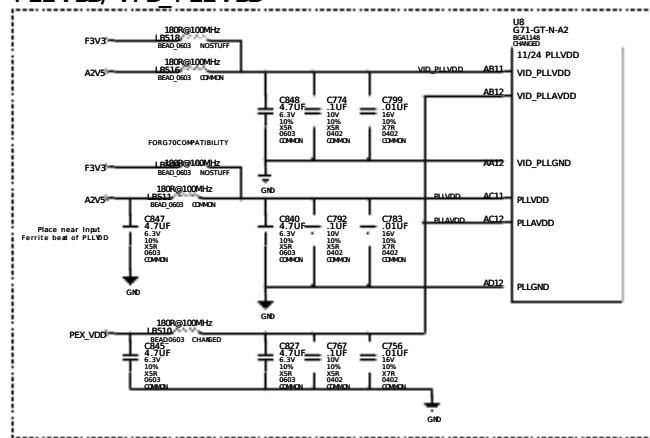
J.D. design PAGE 15 OF 24
NAME: Farsati DATE: 30-JUN-2006

Page16: M SC: GPIO, I2C, ROM, HDCP, HDMI and XTAL

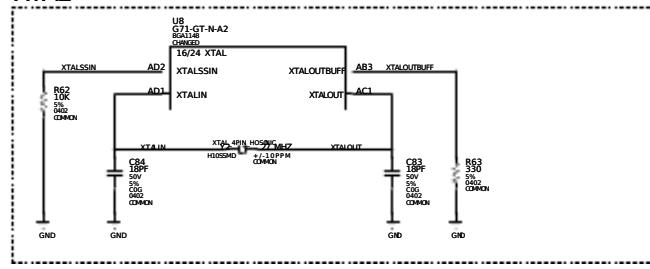
GPIO



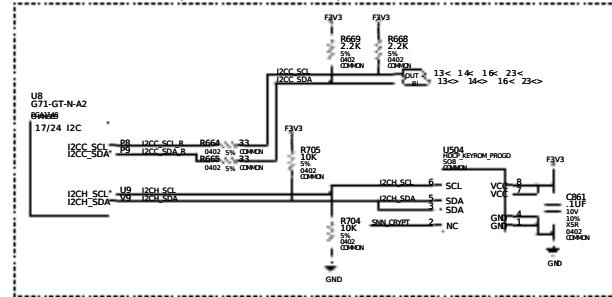
PLL VDD / VID D PLL VDD



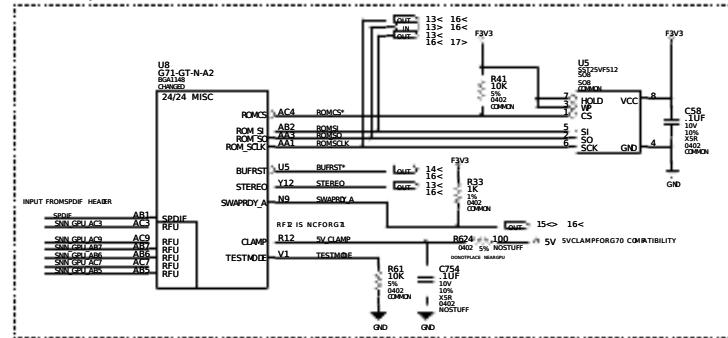
XTAL



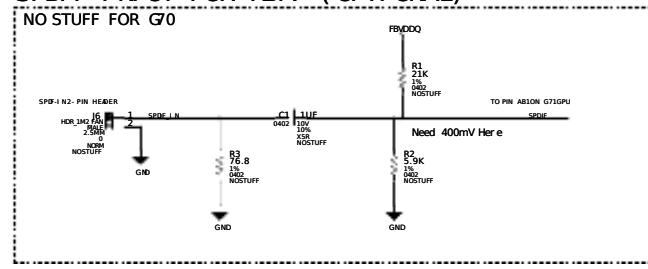
I2CC / I2CH(+HDCP ROM)



ROM / M SC (BUFRST/STEREO/SWAPRDY/TESTMODE)



SPDI F/I INPUT FOR HDMI (OPTIONAL)



M SC NET RULES

NET NV_CRI TI CAL NV_IMPEDANCE

FFPAR

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
VID_BLVDD	2.5V	0.03A	12MIL
PLLVDD	2.5V	0.03A	10MIL
SV_CLAMP	5V		16MIL

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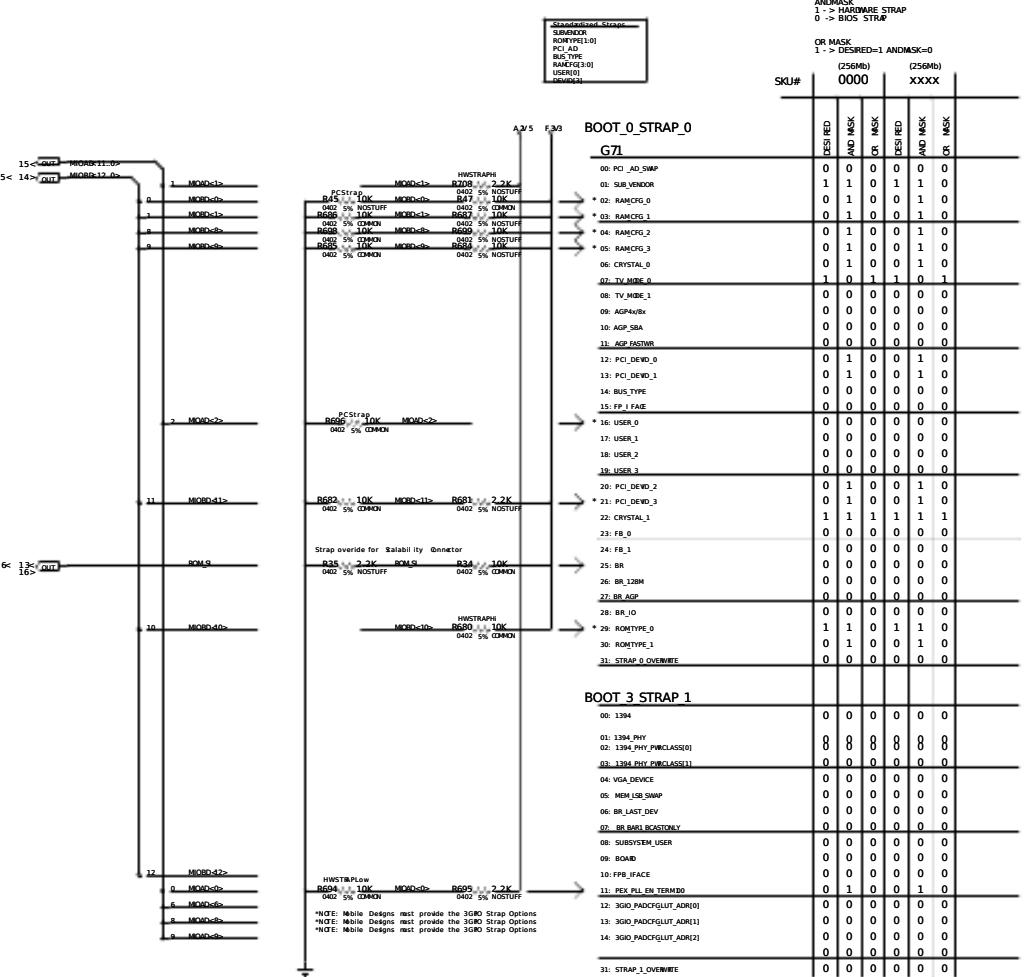
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J.D. design PAGE 16 OF 24

Name I.Farasati Date 30-JUN-2006

Page17: Strapping Configuration

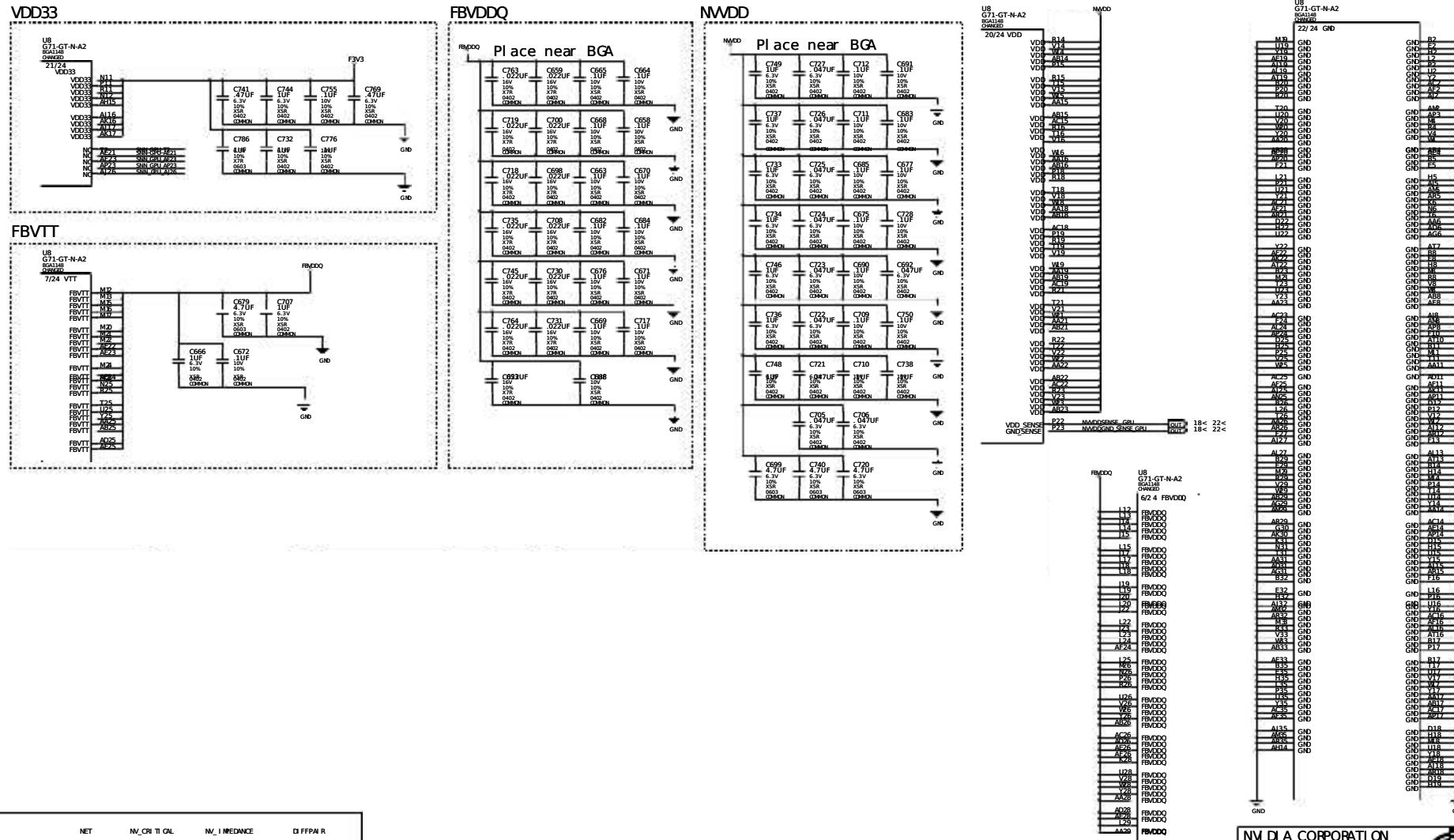


G71 Strap Mapping

	NV_STRAP_0	NOMAL PIN (RTL Name)
HW0default	BIT FUNCTION	
0	PCI_1AD	'NV_PEXTIV_BO0_0_STRAP_PCI_1AD_NORMAL
1	RAM[2:0]	'MICRO1(Cr_ra_data[4:0])
2	RAM[1:1]	'MICRO1(Cr_ra_data[3:0])
3	RAM[0:0]	'MICRO1(Cr_ra_data[2:0])
4	RAM[4:3]	'MICRO1(Cr_ra_data[4:3])
5	CRYSTAL_0	'MICRO1(Cr_ra_data[5:1])
6	TV_MIRE_0	'MICRO1(Cr_ra_data[7:1])
7	AGP_ASWAP	'AGP_AX
8	ROMTYPE_0	'NV_PEXTIV_BO0_0_STRAP_ROMTYPE_0_DISABLED
9	ROMTYPE_1	'NV_PEXTIV_BO0_0_STRAP_ROMTYPE_1_DISABLED
10	ROMTYPE_2	'NV_PEXTIV_BO0_0_STRAP_ROMTYPE_2_DISABLED
11	AGP_FASTW	'MICRO8(Cr_gb_data[4:0])
12	PCI_DEWO[0]	'MICRO8(Cr_gb_data[4:0])
13	PCI_DEWO[1]	'MICRO8(Cr_gb_data[4:0])
14	PCI_DEWO[2]	'MICRO8(Cr_gb_data[4:0])
15	FACEx	'MICRO8(Cr_gb_data[4:0])
16	USB[0]	'MICRO1(Cr_ra_data[5:0])
17	USB[1]	'MICRO1(Cr_ra_data[4:0])
18	USB[2]	'MICRO1(Cr_ra_data[4:0])
19	USB[3]	'MICRO1(Cr_ra_data[4:0])
20	ROMTYPE[2]	'MICRO8(Cr_gb_data[4:0])
21	PCI_DEWO[32:11]	'MICRO8(Cr_gb_data[11])
22	PCI_DEWO[31:11]	'MICRO8(Cr_gb_data[11])
23	FBI[0]	'MICRO8(Cr_gb_data[4:0])
24	BR_128B	'ROMSI (Romsi)
25	BR_128M	'NV_PEXTIV_BO0_0_STRAP_BR_128M_DISABLED
26	BR_AGP	'NV_PEXTIV_BO0_0_STRAP_BR_AGP_DEV_DISABLED
27	BR_IO	'NV_PEXTIV_BO0_0_STRAP_BR_IO_DEV_DISABLED
28	BR_VD	'MICRO8(Cr_gb_data[4:0])
29	ROMTYPE[1]	'MICRO8(Cr_gb_data[4:0])
30	ROMTYPE[0]	'MICRO8(Cr_gb_data[4:0])
31	STRAP_0_OVERRIDE	'HWMsInternal10Kstrap, need 1kto override
	NV_STRAP_1	NOMAL PIN (RTL Name)
0	BIT FUNCTION	NOMAL PIN (RTL Name)
1	1394	'NV_PEXTIV_BO0_1_3TRAP_1_1394_DISABLED
2	1394_PHY	'NV_PEXTIV_BO0_1_3TRAP_1_1394_PHY_DISABLED
3	1394_PHY_PUBLASS0	'MICRO8(Cr_gb_data[4:0])
4	1394_PHY_PUBLASS1	'MICRO8(Cr_gb_data[4:0])
5	VGA_DEVICE	'NV_PEXTIV_BO0_1_3TRAP_1_VGA_BUCE_ENABLED
6	MEM_LS_SWAP	'MEMLS_SWAP
7	BR_BAR1CASTONLY	'NV_PEXTIV_BO0_1_3TRAP_1_BR_BAR1CASTONLY_ENABLED
8	SUBSYSTEM_USER	'NV_PEXTIV_BO0_1_3TRAP_1_SUBSYSTEM_USER_Disabled
9	PCI_1AD	'MICRO8(Cr_gb_data[4:0])
10	PCI_DEWO[32:11]	'MICRO8(Cr_gb_data[11])
11	PCI_DEWO[31:11]	'MICRO8(Cr_gb_data[11])
12	3GIO_PADCFGUT[ADR0]	'MICRO8(Cr_gb_data[6])
13	3GIO_PADCFGUT[ADR1]	'MICRO8(Cr_gb_data[6])
14	3GIO_PADCFGUT[ADR2]	'MICRO8(Cr_gb_data[6])
15	FBI[1]	'128bit
16	FBI[0]	'24bit (Default)
17	PEX_PLL_EN_TERM100	'PARALLEL internal 100ohmTer
18	3GIO_PADCFGUT_LUT[ADR[2:0]]	'DI SABED
19	STRAP_OVERRIDE	'0 = DEFAULT

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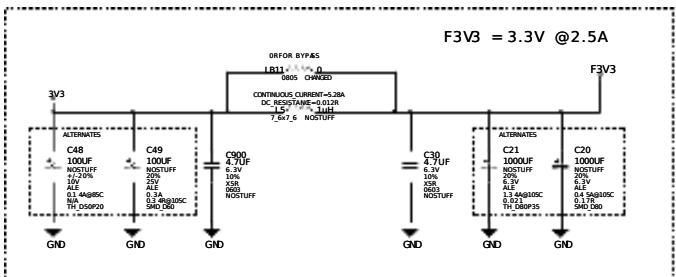
Page18: Power/GND and Decoupling



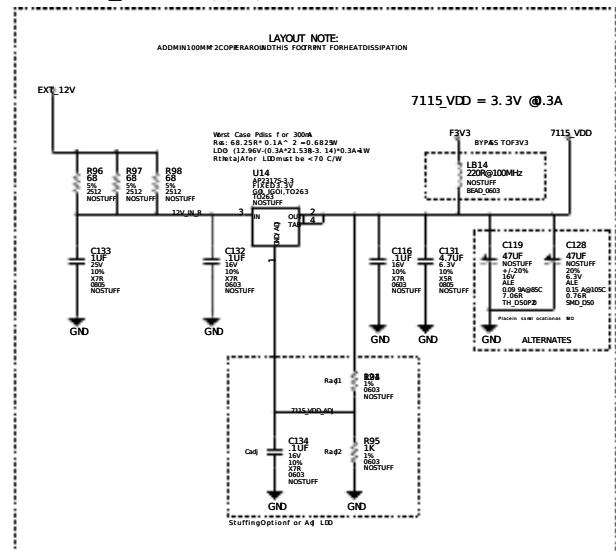
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Page19: Power Supply I: A2V5, DDC5V, SAA7115, TMDS Supplies

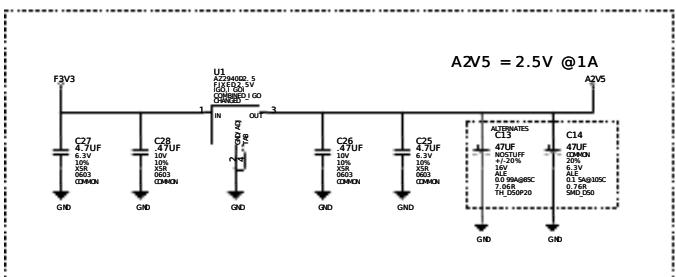
F3V3 Supply



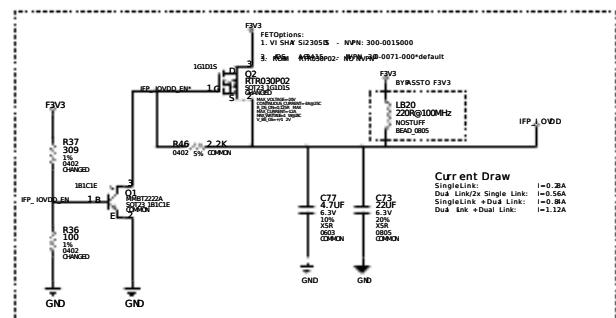
SAA7115_VDD Supply



A2V5 Supply



TMDS I/OVDD Backdrive Prevention



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POWER NET RULES

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
F3V3NETRULES	3.3V	2.5A	10MIL
7115_VDD	3.3V	0.3A	12MIL
IPF_I_OVDD	3.3V	1.2A	16MIL
SVand DDC5VNETRULES	5V	0.1A	16MIL
DDC5V	5V	0.1A	16MIL
A2V5NETRULES	2.5V	1.0A	16MIL
A2V5	2.5V	1.0A	16MIL

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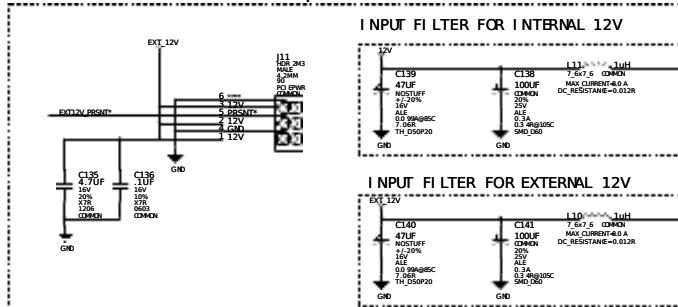
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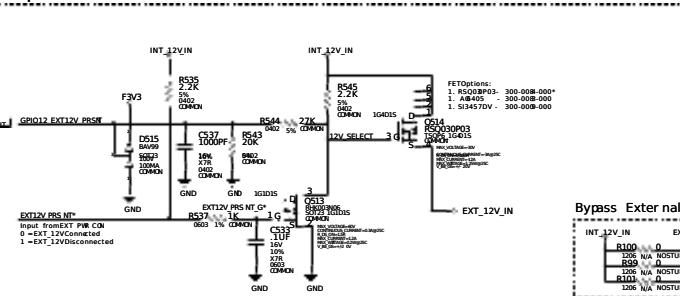
J.D. design PAGE 19 OF 24
NAME: Farasati DATE: 30-JUN-2006

Page 20: Power Supply II: PEX Input Filters, External 12V Power, NVDD VID Control

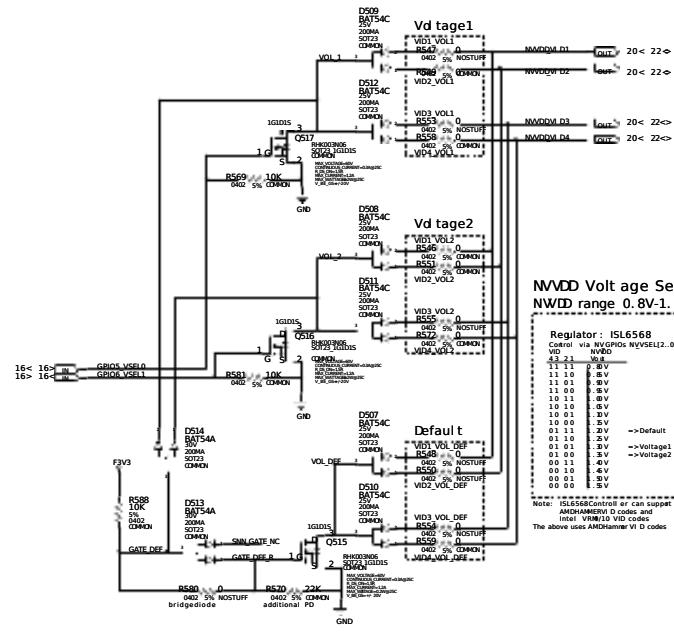
Internal & External 12V Input Filters



12V Input Selection for NVDD



NVDD VID CONTROL



Default select for NVDD.VID[4..1]

NET	VOLTAGE	MAX_CURRENT	M_N_LINE_WIDTH
EXT_12V	12V	5.5A	S0M1
INT_12V_IN	12V	8A	S0M1
EXT_12V_IN	12V	8A	S0M1
NET	NV_CRITICAL	NV_IMPEDANCE	FFPAIR
VOL_1	IN	NMDD01_D1	
VOL_1	IN	NMDD01_D2	
VOL_1	IN	NMDD01_D3	
VOL_1	IN	NMDD01_D4	
VOL_2	IN	VOL1_VOL1	
GATE_DEF	IN	VOL1_GATE_R	
GATE_DEF	IN	VOL1_GATE_R	
12V_SELECT	EXT_12V_BRENTE		
12V_SELECT	EXT_12V_BRENTE		

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ASSEMBLY PAGE DETAIL G71GT2-H S128 16M32 QD93, DVI-I-DL + DVI-DL + HDMI, w/HDD, 550/700 MHz
Power Supply II: PEX Input Filter, External 12V Power, NVDD VID Control

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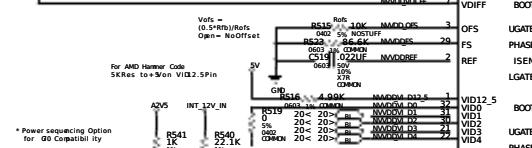
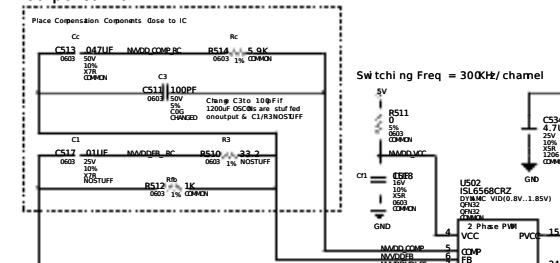
J.D. design PAGE 120 OF 24

Name I.Farasati

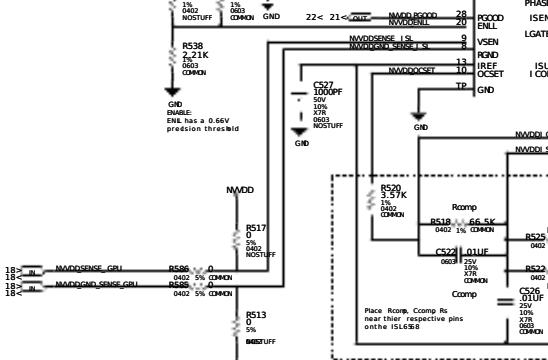
Date 30-JUN-2006

Page22: Power Supply I V: NVDD

Compensation

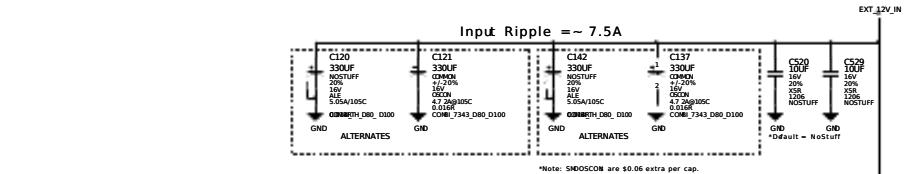


* Power sequencing Option for G6 compatibility



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Input Ripple = ~ 7.5A



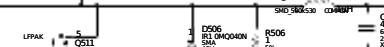
*Note: SMDOSCON are \$0.06 extra per cap.

Placer near Drain of TopMafet

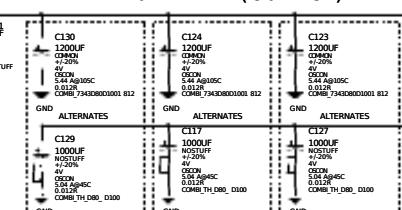


Output 1 Inductor Options:
1. Delta H0113P1R0W - 131-0014000
2. Vishay ILHP5050E2B1H0 - 131-0003-000

CONTINUOUS CURRENT=2A
DC RESISTANCE<0.0015 MAX



NVDD = 1.0V..1.2V (30..45A)



Place in same location as SM0

Placer near Drain of TopMafet



Output Inductor Options:
1. Delta H0113P1R0W - 131-0014000
2. Vishay ILHP5050E2B1H0 - 131-0003-000

CONTINUOUS CURRENT=2A
DC RESISTANCE<0.0015 MAX



Place in same location as SM0

Placer Bottom

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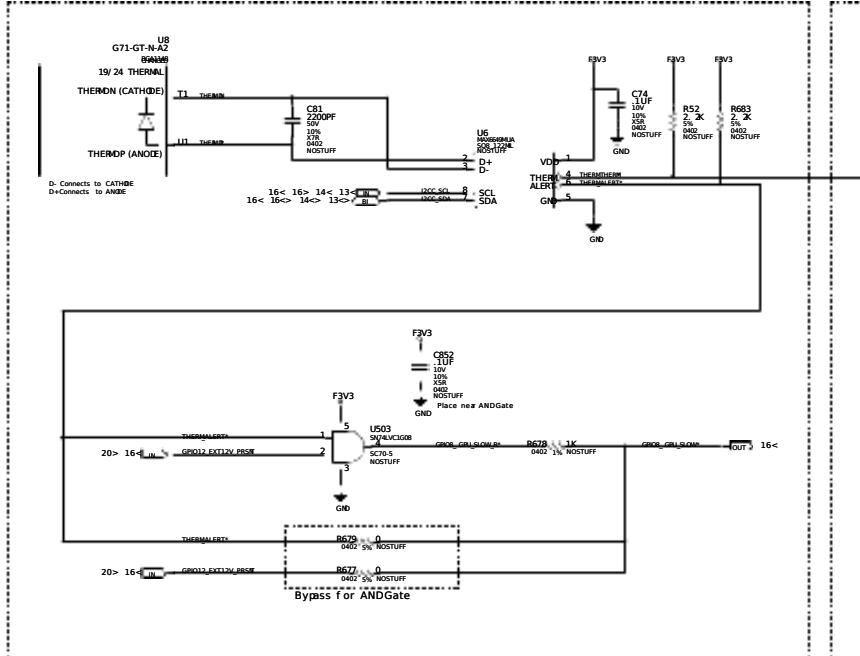
SANTA CLARA, CA 95050 USA

NV_PN 600-10455-0007-100_A

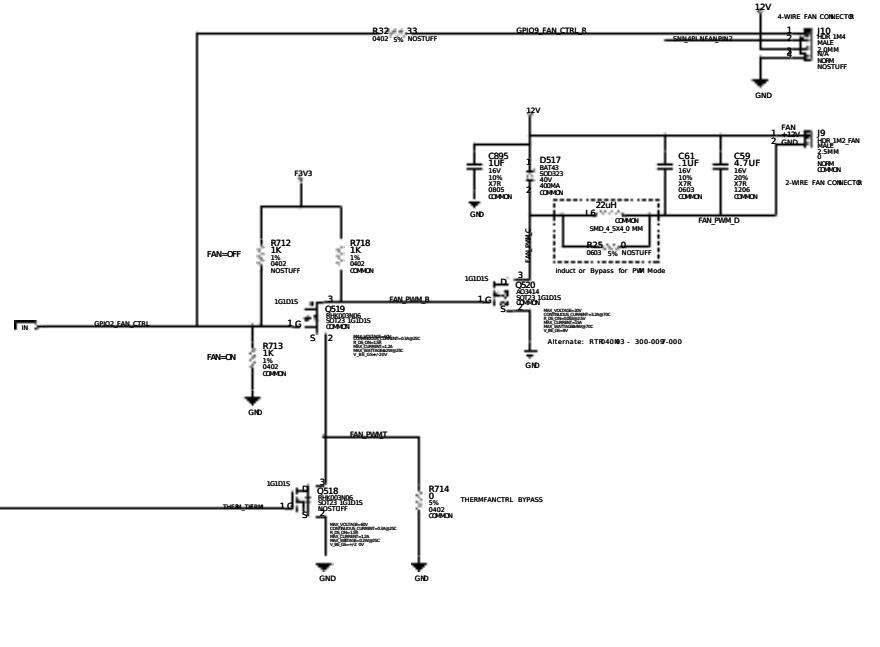
J.D. design PAGE 122 QE 24

Name: J.Farasati DATE 10-JUN-2006

1 EXTERNAL THERMAL DIODE



2 FAN CONTROL



NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
FAN_PWM_B			
FAN_PWM_C			
FAN_PWM_D			
FAN_PWM_T			
23	THERMAL_B		
	THERMAL_T		
	GPO9_SMD_SQ_DW		
NET		MIN_WIDTH	
THEINP		10mil	
THEIRP		10mil	

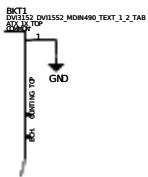
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A B C D E F G H

Page24: Mechanical: Bracket/ Thermal Solution

1 Brackets:

151-10001-0006-000 DVI, DVI, MDIN (text - 1-South, 2-North)
 151-10001-0006-002 DVI, DB15, MDIN



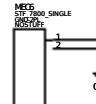
2 Connect or Screws

MEC1
HEX JACK SCREW
GND
MEC2
HEX JACK SCREW
GND
MEC3
HEX JACK SCREW
GND
MEC4
HEX JACK SCREW
GND

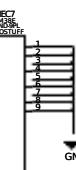
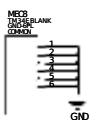
Bracket Screw

MEC5
PHL4.4X0.1875 SCREW
COMMON
newLF screw - 155-0001-000.
RHScrew - 154-0003-700.

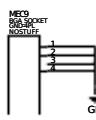
Stiffener for W5 SKUs



3 Heat sink



4 BGA Socket



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NV_PN	600-10455-0007-100_A	ID	design
NAME	I.Farasati	DATE	30-JUN-2006