AT818

3.0A Ultra Low Dropout Regulator



Immense Advance Tech.

FEATURES

- Adjustable Output from 0.8V
- Input Voltage as Low as 1.8V
- Enable Pin
- 250mV Dropout @2A
- Over Current and Over Temperature Protection
- 5µA Quiescent Current in Shutdown
- P-CH Design to Reduce the Operation Current
- Full Industrial Temperature Range

APPLICATION

- Notebook computers
- Battery Powered Systems
- Motherboards/Peripheral Cards
- Telecom/Networking Cards
- Industrial Applications
- Set Top Boxes
- Wireless Infrastructure
- Medical Equipment

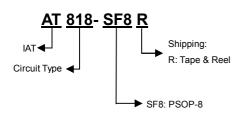
DESCRIPTION

The AT818 is a high performance positive voltage regulator designed for use in applications requiring very low input voltage and very low dropout voltage at up to 3A amps. It operates with a V_{IN} as low as 1.8V, with output voltage programmable as low as 0.8V. The AT818 features ultra low dropout, ideal for applications where V_{OUT} is very close to V_{IN} . Additionally, the AT818 has an enable pin to further reduce dissipation while shut down. The enable pin may be tied to V_{IN} if it is not required for ON/OFF control. The AT818 provides excellent regulation over variations in line, load and temperature.

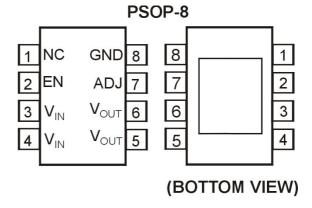
The AT818 is available in the PSOP-8 (Exposed Die Pad) package. The output can be programmed from 0.8V to 5V with two external resistive divider.

The optimum thermal condition has to consider the layout, placement and application to achieve it to satisfy high output current requirement.

ORDER INFORMATION



PIN CONFIGURATIONS (TOP VIEW)



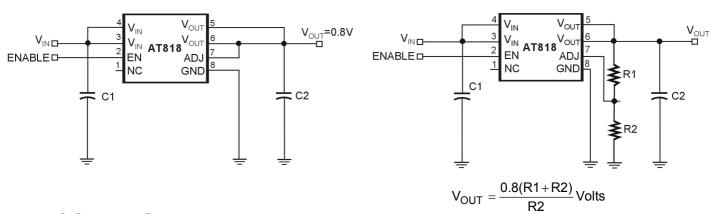
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PIN DESCRIPTIONS

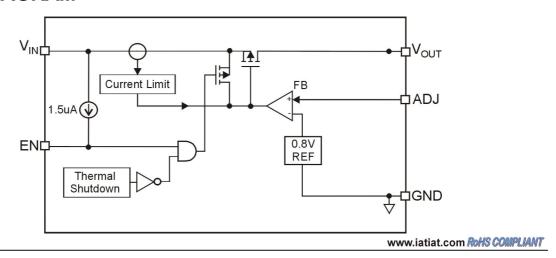
Pin Name	Pin Description		
NC	No Connect.		
	Enable Input. Pulling this pin below 0.4V turns the regulator off, reducing the quiescent		
EN	current to a fraction of its operating value. The device will be enabled if this pin is left open.		
	Connect to V _{IN} if not being used.		
\ <u>/</u>	Input Voltage. A large bulk capacitance should be placed closely to this pin to ensure that		
V _{IN}	the input supply does not sag below 1.8V.		
Vout	The pin is the power output of the device.		
	ADJ pin is the input to the error amplifier. The ADJ reference voltage is 0.8V referenced to		
ADJ	ground. The output range is 0.8V to 5V: $V_{OUT} = \frac{0.8(R1+R2)}{R2}$ Volts		
GND	Reference Ground.		
THERMAL	Pad for heatsinking purposes. Connect to ground plane using multiple vias. Not electrically		
PAD	connected internally.		

TYPICAL APPLICATION CIRCUITS



BLOCK DIAGRAM

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Para	ameter	Symbol	Max Value	Unit		
Supply Voltage, V _{IN}		V _{IN}	6	٧		
Control Voltage, EN	ontrol Voltage, EN		ontrol Voltage, EN		6	٧
Output Voltage, V _{OUT}		Vout	6	V		
Junction Temperature		TJ	125	°C		
Lead Temperature(Solde	ring) 5 Sec.	T _{LEAD}	260	°C		
Storage Temperature Range		T _{STG}	-65 to +150	°C		
Power Dissipation PD @ TA=25°C	PSOP-8(Exposed Pad)	P _D	2770	mW		
Thermal Resistance (Note 2)	PSOP-8	ΘЈΑ	36	°C/W		
Thermal Resistance	PSOP-8	Θ _{JC}	5.5	°C / W		
ESD Rating (Human Bod	y Model) (Note 3)	V _{ESD}	2	kV		

RECOMMENDED OPERATING CONDITIONS (Note 4)

Parameter	Symbol	Operation Conditions	Unit
Supply Voltage, V _{IN}	V _{IN}	1.8 to 5.5	V
Output Voltage, V _{OUT}	V _{OUT}	0.8 to 5.5	V
Operating Junction Temperature	TJ	-40 to +125	°C
Operating Ambient Temperature Range	TA	-40 to +85	°C

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

- Note 2: 2 square inch of FR-4, double sided, 1 oz. minimum copper weight.
- Note 3: Devices are ESD sensitive. Handling precaution recommended.
- Note 4: The device is not guaranteed to function outside its operating conditions.

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ELECTRICAL CHARACTERISTICS

Unless specified: $V_{EN} = V_{IN}$, $V_{IN} = 1.8V$ to 5.5V and $I_{LOAD} = 10\mu A$ to 2A, $T_A = 25^{\circ}C$.

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
V _{IN}						
Supply Voltage Range	V _{IN}		1.8		5.5	٧
Quiocoont Current	IQ	$V_{IN} = 3.3V$, $V_{EN} = V_{IN}$		0.4	1.45	mA
Quiescent Current		V _{IN} = 5.5V, V _{EN} = 0V		5	10	μΑ
V _{OUT}						
	V _{REF}	V _{IN} =3.3V, V _{ADJ} =V _{OUT} ,	0.788	0.8	0.812	V
Reference Voltage (Note 5)		I _{LOAD} =10mA				
Adjust Pin Current (Note 7)	I _{ADJ}	V _{ADJ} =V _{REF}		80	200	nA
Line Regulation (Note 5)	REG _(LINE)	$V_{IN} = 1.8V \text{ to } 5.5V, V_{ADJ} = V_{OUT},$		0.2	1.0	%/V
Line Regulation (Note 5)		I _{LOAD} =10mA				
Load Regulation (Note 5)	REG _(LOAD)	$V_{IN} = 3.3V, V_{OUT} = 2.5V,$		0.1	1.0	%
Load Regulation (Note 5)		10mA≤I _{LOAD} ≤2A				
		I _{LOAD} =1A, V _{OUT} = 2.5V		200	300	mV
Dropout Voltage (Note 5, 6)	V_D	I _{LOAD} =2A, V _{OUT} = 2.5V		250	350	mV
		I _{LOAD} =3A, V _{OUT} = 2.5V		350	450	mV
Current Limit (Note 7)	I _{CL}			3.6		Α
EN						
Enable Pin Current	I _{EN}	$V_{EN} = 0V, V_{IN} = 3.3V$		1.5	10	μΑ
Enable Pin Threshold	V_{IH}	V _{IN} = 3.3V	1.6			٧
Liable Fill Tilleshold	V_{IL}	V _{IN} = 3.3V			0.4	V
Oven Temperature Protection						
High Trip Level	T _{HI}			160		°C
Hysteresis	V _{HYST}			20		°C

Note 5: Low duty cycle pulse testing with Kelvin connections required.

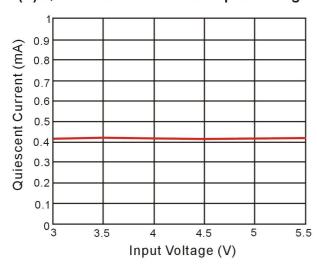
Note 6: Defined as the input to output differential at which the output voltage drops to 2%.

Note 7: Guaranteed by design.

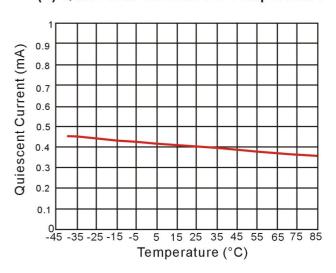


TYPICAL OPERATING CHARACTERISTICS

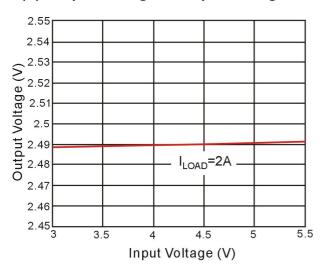
(1) Quiescent Current vs. Input Voltage



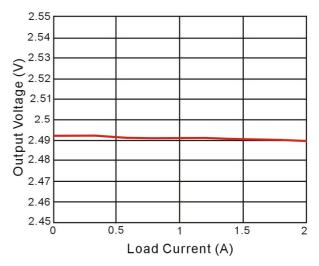
(2) Quiescent Current vs. Temperature



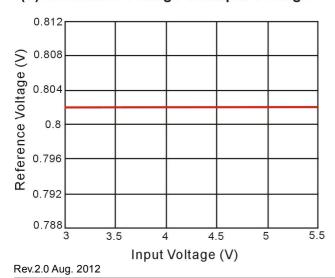
(3) Output Voltage vs. Input Voltage



(4) Output Voltage vs. Load Current



(5) Reference Voltage vs. Input Voltage



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APPLICATION INFORMATION

Introduction

The AT818 is intended for applications where high current capability and very low dropout voltage are required. It provides a very simple, low cost solution that uses very little PCB real estate. Additional features include an enable pin to allow for a very low power consumption standby mode, and a fully adjustable output.

Component Selection

Input Capacitor: A minimum of $10\mu\text{F}$ ceramic capacitor is recommended to be placed directly next to the V_{IN} pin. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, bulk capacitance of about $100\mu\text{F}$ may be added closely to the input supply pin of the AT818 to ensure that V_{IN} does not sag, improves load transient response.

Output Capacitor: A minimum bulk capacitance of 10μF, along with a 0.1μF ceramic decoupling capacitor is recommended. Increasing the bulk capacitance will improve the overall transient response. The use of multiple lower value ceramic capacitors in parallel to achieve the desired bulk capacitance will not cause stability issues. Although designed for use with ceramic output capacitors, and thus will also work comfortably with tantalum output capacitors.

External Voltage Selection Resistors: The use of 1% resistors, and consider for system stability and power losing, we recommend to design high dividing resistance (R1<300K Ω) to strengthen the benefits which AT818 has inherent.

Noise Immunity: In very electrically noisy environments, it is recommended that $0.1\mu F$ ceramic capacitors be placed from V_{IN} to GND and V_{OUT} to GND as close to the device pins as possible.

Parallel a small cap (ex:100pF) would be recommended to improve the transient response.

Thermal Considerations

The power dissipation in the AT818 is approximately equal to the product of the output current and the input to output voltage differential:

$$P_D \approx (V_{IN} - V_{OUT}) \times I_{LOAD}$$

The absolute worst-case dissipation is given by:

$$P_{D(MAX)}=(V_{IN(MAX)}-V_{OUT(MIN)})xI_{LOAD(MAX)} + V_{IN(MAX)}xI_{G(MAX)}$$

For a typical scenario, V_{IN} =3.3V ± 5%, V_{OUT} =2.5V and I_{LOAD} =1.5A, therefore:

$$\begin{split} &V_{IN(MAX)}\text{=}3.465\text{V}, &V_{OUT(MIN)}\text{=}2.45\text{V} \text{ and} \\ &I_{G(MAX)}\text{=}1.45\text{mA}, &\text{Thus } P_{D(MAX)}\text{=}1.53\text{W}. \end{split}$$

Using this formula, and assuming $T_{A(MAX)}$ =85°C, we can calculate the maximum thermal impedance allowable to maintain $T_J \le 125$ °C

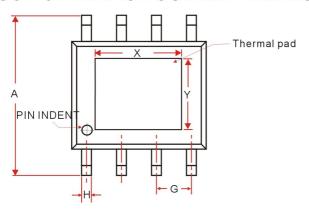
$$R_{TH(J\text{-}A)(MAX)} = \frac{\left(T_{J(MAX)} - T_{A(MAX)}\right)}{P_{D(MAX)}} = \frac{(125 - 85)}{1.53} = 26.1^{\circ}C/W$$

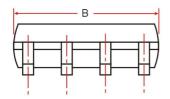
The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad.

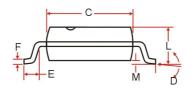


PACKAGE OUTLINE DIMENSIONS

PSOP-8 PACKAGE OUTLINE DIMENSIONS

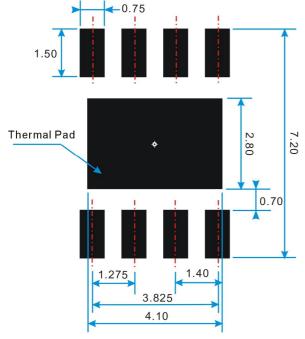






	DIMENSIONS		
REF.	Millimeters		
	Min.	Max.	
Α	5.79	6.20	
В	4.80	5.00	
С	3.80	4.00	
D	0°	8°	
E	0.40	1.27	
F	0.15	0.26	
М	0	0.25	
Н	0.31	0.51	
L	1.30	1.75	
G	1.27 TYP.		
Х	3.30 TYP.		
Υ	2.50 TYP.		

PSOP-8 PACKAGE FOOTPRINT (mm)



Note:

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