PMIC for TFT-LCD TV Panels

General Description

The RT6929 offers a compact power supply solution to provide all voltages required by a TFT-LCD panel. With its high current capabilities, the device is ideal for large screen monitors panels and LCD TV applications with 12V supply voltage. RT6929 is available in a WQFN-48L 6x6 package.

Ordering Information

RT6929 □□

Package Type
QW : WQFN-48L 6x6 (W-Type)
(Exposed Pad-Option 1)

Lead Plating System
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▸ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▸ Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT6929GQW : Product Number
YMDNN : Date Code

Features

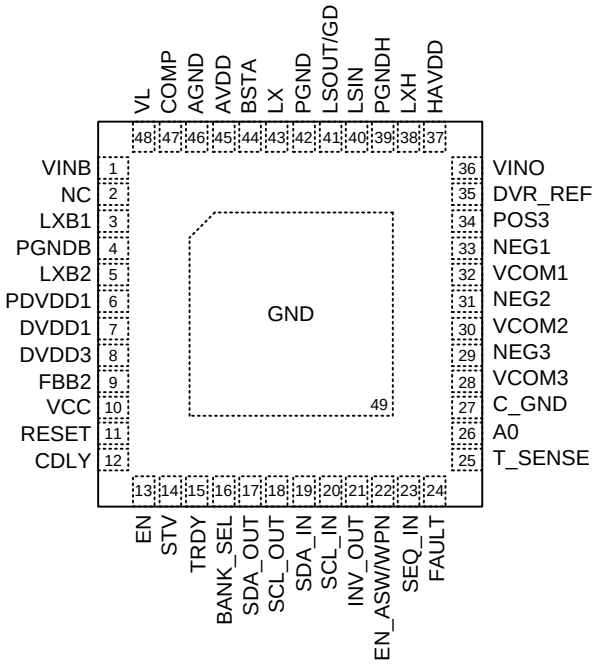
- **9.5V to 14.7V Input Supply Voltage**
- **1.5A to 5A Boost Regulator for AVDD with 13.5V to 19.4V Programmable Output and OCP**
- **1.5A/3.5A Sync. Buck Regulator for DVDD1**
- **1.5A/3.5A Sync. Buck Regulator for DVDD2**
- **0.5A Linear Regulator for DVDD3**
- **1.2A Sync. Buck Regulator or OP type for HAVDD with 6.75V to 9.7V Programmable Output**
- **3-CH VCOM**
- **2-CH Analog Switch**
- **2.7MHz / 2.25MHz / 1.8MHz / 1.5MHz / 1.35MHz / 1.2MHz / 900kHz / 750kHz / 600kHz / 450kHz Selectable Switching Frequency for DVDD1 and DVDD2**
- **900kHz / 750kHz / 600kHz / 450kHz Selectable Switching Frequency for AVDD and HAVDD**
- **7-Bit Programmable VCOM1 Calibrator with EEPROM**
- **7-Bit Programmable AVDD Trimming with EEPROM**
- **Programmable Sequencing**
- **Over-Temperature Protection**
- **I2C-Compatible Interface for Register Control**

Applications

- TFT-LCD TV Panel

Pin Configurations

(TOP VIEW)



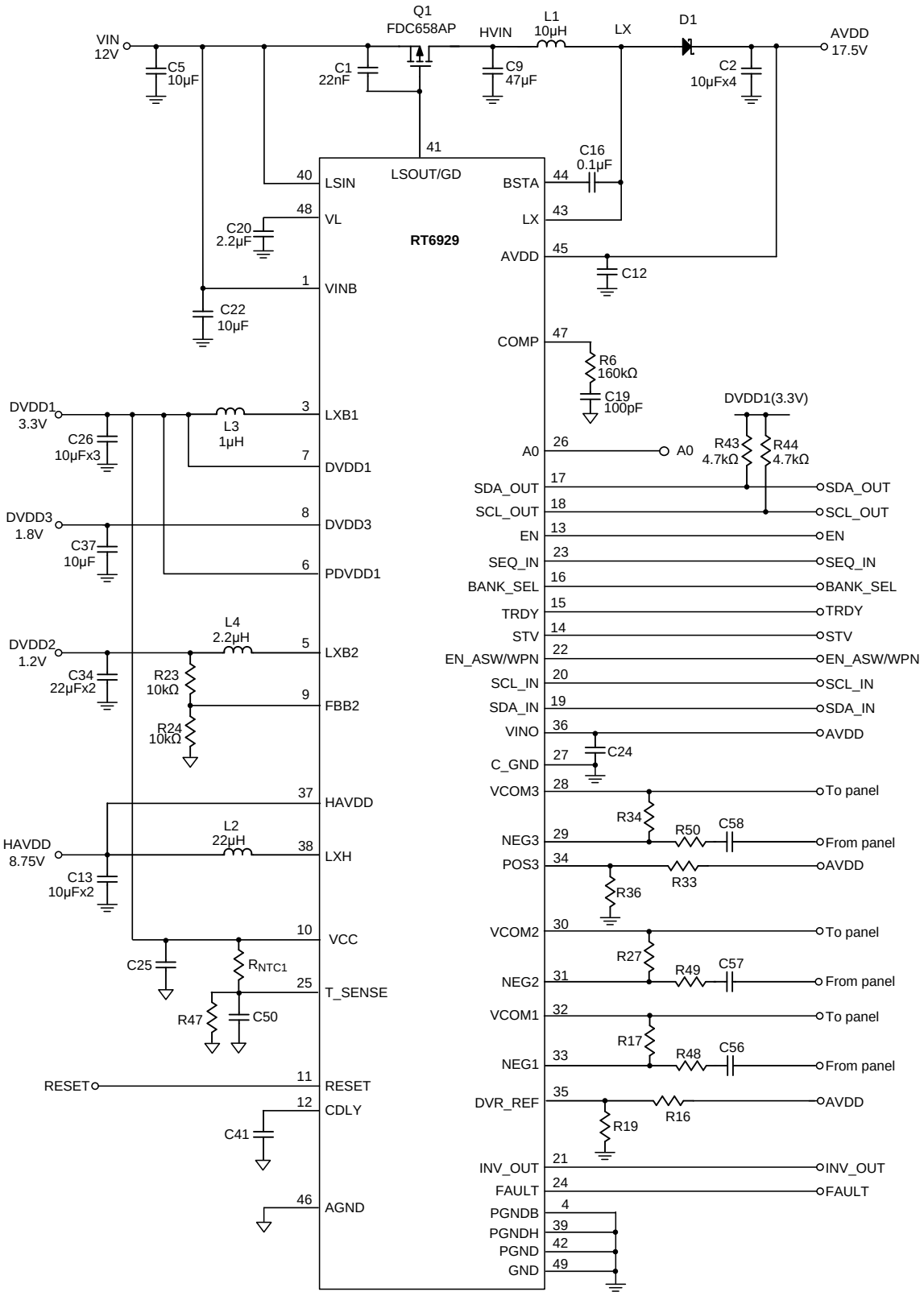
WQFN-48L 6x6

Functional Pin Description

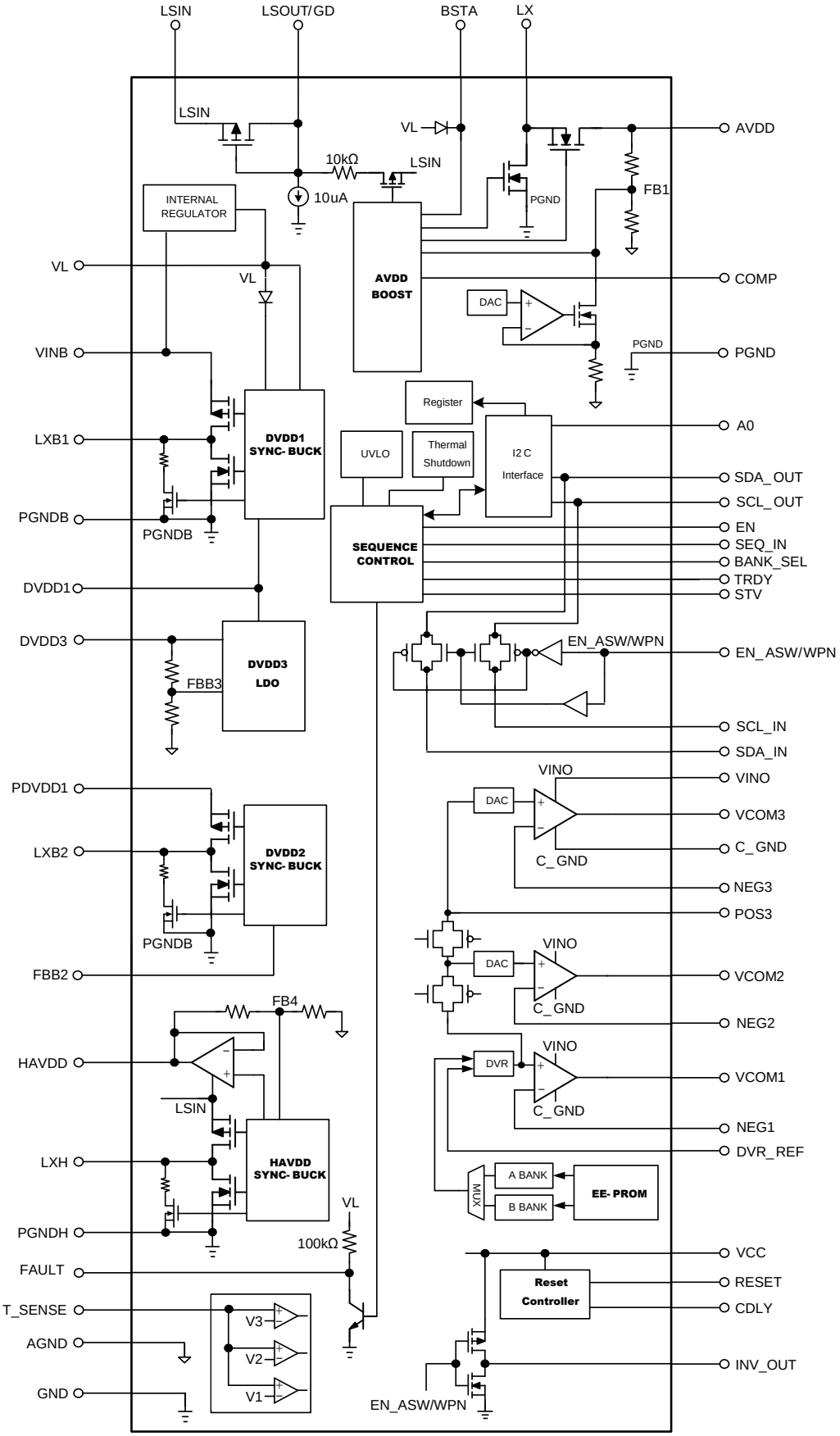
Pin No.	Pin Name	Pin Function
1	VINB	Supply Input Pin for Buck Converter DVDD1 (3.3V).
2	NC	No Internal Connection.
3	LXB1	Switching Node of Buck Converter DVDD1 (3.3V).
4	PGNDB	Power Ground of 3.3VDD, 1.2VDD Buck Converter.
5	LXB2	Switching Node of 1.2VDD Buck Converter.
6	PDVDD1	Power Input of 1.2VDD Buck Converter.
7	DVDD1	Power for 1.8VDD LDO & Feedback of Buck Converter DVDD1 (3.3V).
8	DVDD3	Output of 1.8VDD LDO.
9	FBB2	Feedback of 1.2VDD Buck Converter.
10	VCC	Power for RESET, Inverter.
11	RESET	RESET Signal Output from the integrated DVDD1 (3.3V) Voltage Detector. Active Low.
12	CDLY	RESET Signal Delay Adjustment Point. The value of the capacitance on this Pin Sets the Time Delay for the RESET Output.
13	EN	Enable Signal Input of 3.3VDD, 1.2VDD Buck Converter, 1.8VDD LDO.
14	STV	SCAN Driver Start Signal Input Pin.
15	TRDY	Enable Signal Input from T-CON.
16	BANK_SEL	Bank Select Input for AVDD, HAVDD, DVR and AVDD trimming of 2D/3D; Bank_Sel = 0 => Output Bank 1 = 2D Bank_Sel = 1 => Output Bank 2 = 3D

Pin No.	Pin Name	Pin Function
17	SDA_OUT	Analog Switch Output. (Connect with T-CON I2C interface)
18	SCL_OUT	Analog Switch Output. (Connect with T-CON I2C interface)
19	SDA_IN	I^2C Compatible Serial-Data Input. Analog Switch Input. (Connect with Connector only)
20	SCL_IN	I^2C Compatible Serial-Clock Input. Analog Switch Input. (Connect with Connector only)
21	INV_OUT	Inverting Output from Integrated Inverter. (INV_IN function Pin is EN_ASW/WPN Pin)
22	EN_ASW/WPN	Enable/Disable for the Integrated Analog Switch. Active Low is AVDD Trimming and DVR Writing Protection. 0 = Prevent I2C Data Writes to Internal AVDD Trimming & DVR EEPROM but allow register writing. 1 = Allow I2C Data Writes to Internal AVDD Trimming & DRV EEPROM and Register.
23	SEQ_IN	Enable/Disable for AVDD and HAVDD.
24	FAULT	FAULT Signal (DATA EN, SCP, TSD, UVLO) Output & Enable Signal Input.
25	T_SENSE	Temperature Sense Pin.
26	A0	Slave Address Assignment.
27	C_GND	Ground of Amplifier.
28	VCOM3	Output of VCOM Amplifier 3.
29	NEG3	Negative Input of VCOM Amplifier 3.
30	VCOM2	Output of VCOM Amplifier 2.
31	NEG2	Negative Input of VCOM Amplifier 2.
32	VCOM1	Output of VCOM Amplifier 1.
33	NEG1	Negative Input of VCOM Amplifier 1.
34	POS3	Positive Input of VCOM Amplifier 3.
35	DVR_REF	DVR Reference Input.
36	VINO	Power Input of VCOM Amplifier.
37	HAVDD	HAVDD Buck Feedback Input & Amplifier Output.
38	LXH	Switching Node of HAVDD Buck Converter.
39	PGNDH	Power Ground of HAVDD Buck Converter.
40	LSIN	Load Switch Input & Power Input of HAVDD Buck Converter.
41	LSOUT/GD	Load Switch Output or Gate Drive Pin for External P-MOSFET.
42	PGND	Power Ground of AVDD Boost Converter.
43	LX	Switching Node of AVDD Boost Converter.
44	BSTA	Bootstrap Capacitor Connection of AVDD Boost Converter.
45	AVDD	AVDD Boost OUTPUT & Feedback Input.
46	AGND	Analog Ground.
47	COMP	Compensation Pin for AVDD Boost Control Loop.
48	VL	Internal Linear Regulator Output. Connect this pin with a decoupling capacitor.
49 (Exposed Pad)	GND	Ground. The Exposed Pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Typical Application Circuit



Function Block Diagram



AVDD Boost Application Circuits

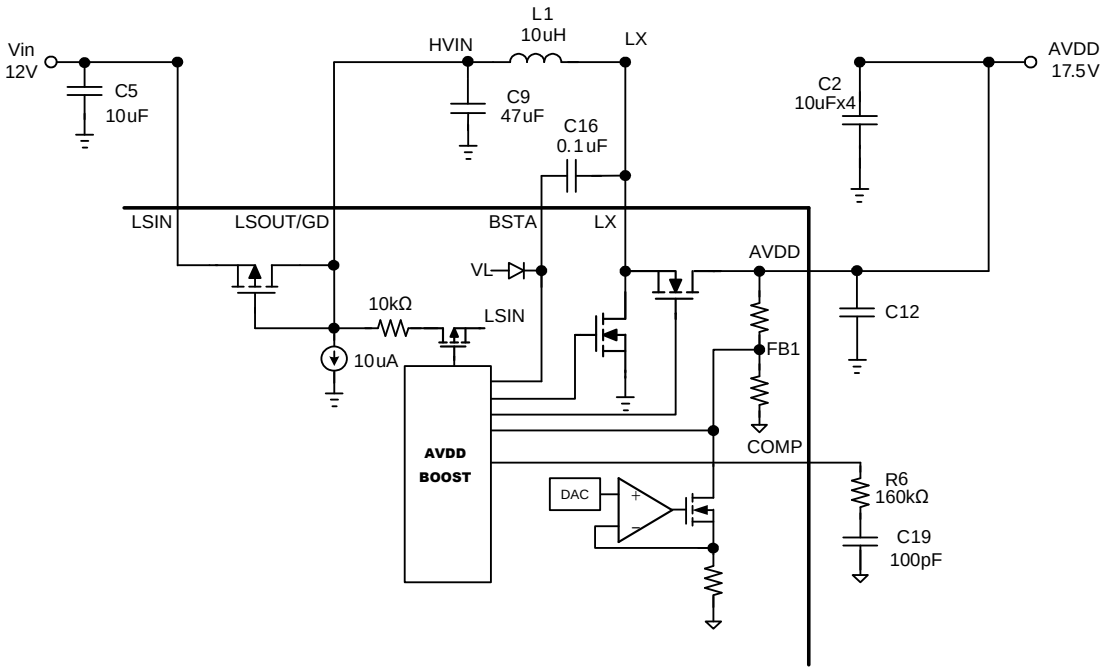


Figure 1. AVDD Control I: Register 14h[2:1] = 00, Sync-Boost Structure used Internal GD MOS

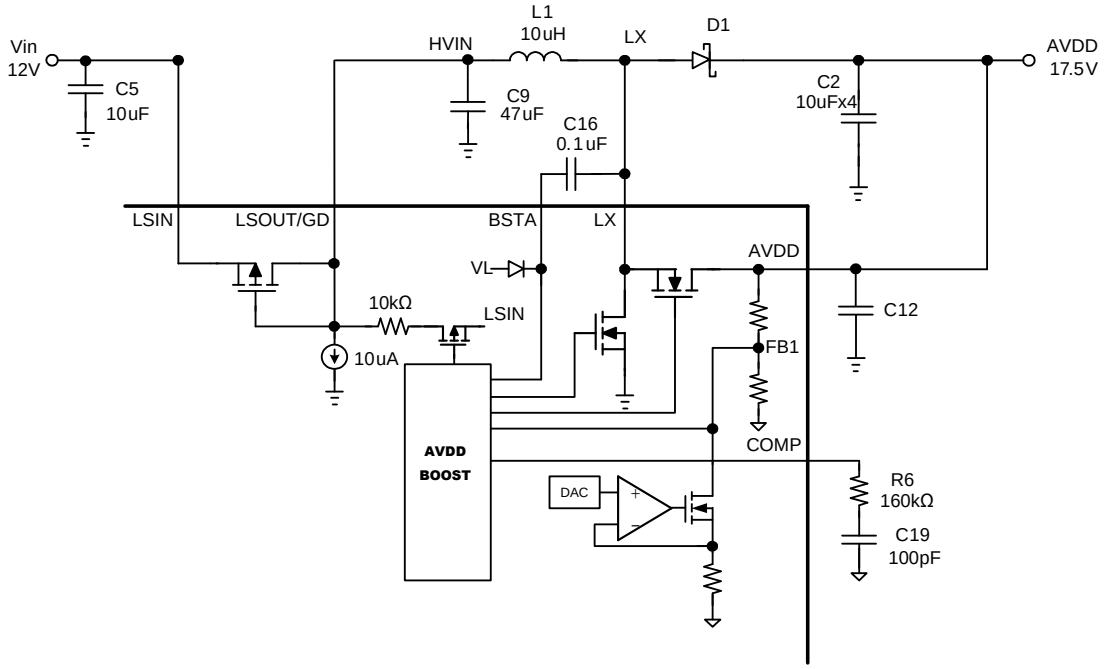


Figure 2. AVDD Control II : Register 14h[2:1] = 01, Asyn-Boost Structure used Internal GD MOS.

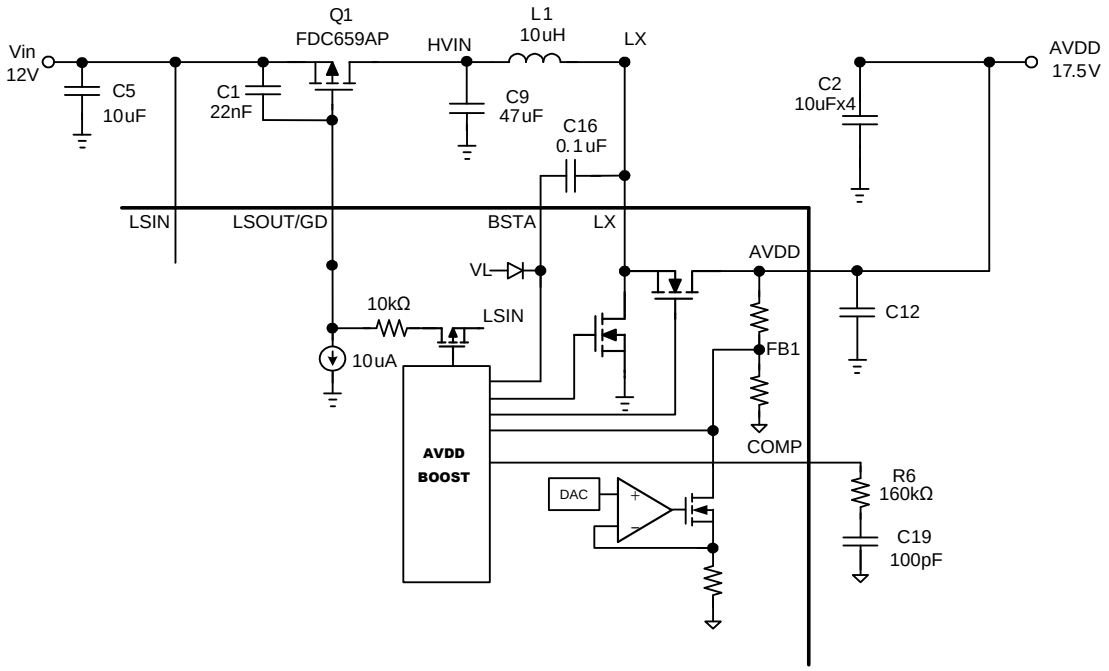


Figure 3. AVDD Control III : Register 14h[2:1] = 10, Sync-Boost Structure used External GD MOS.

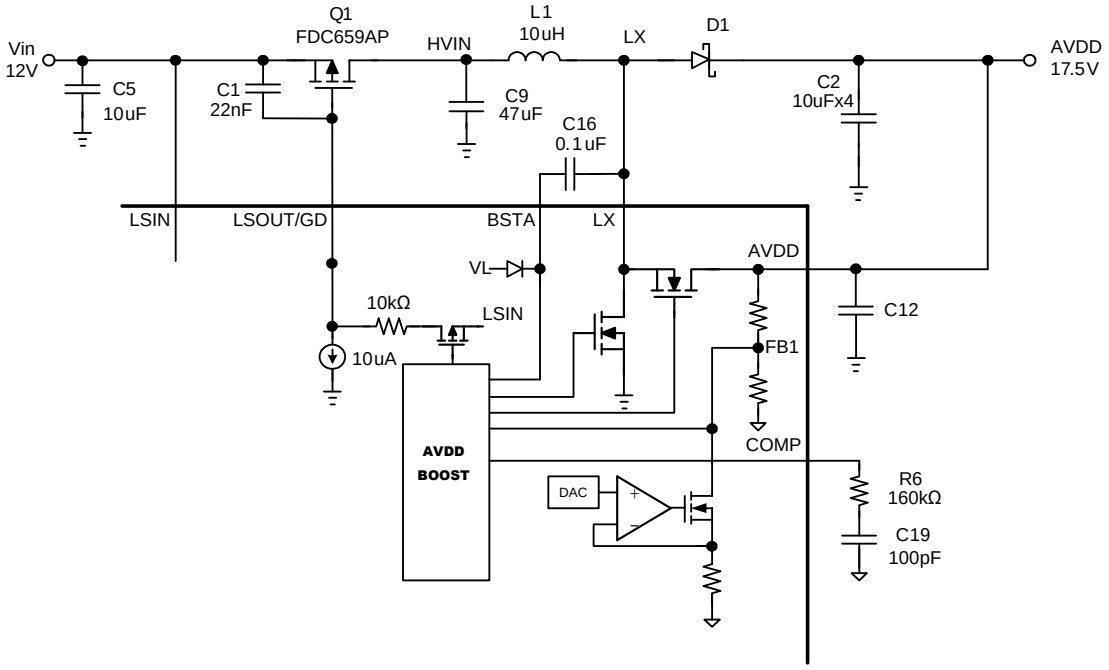


Figure 4. AVDD Control IV : Register 13h[2:1] = 11, Asyn-Boost Structure used External GD MOS.

DVDD1 HV Buck Application Circuits

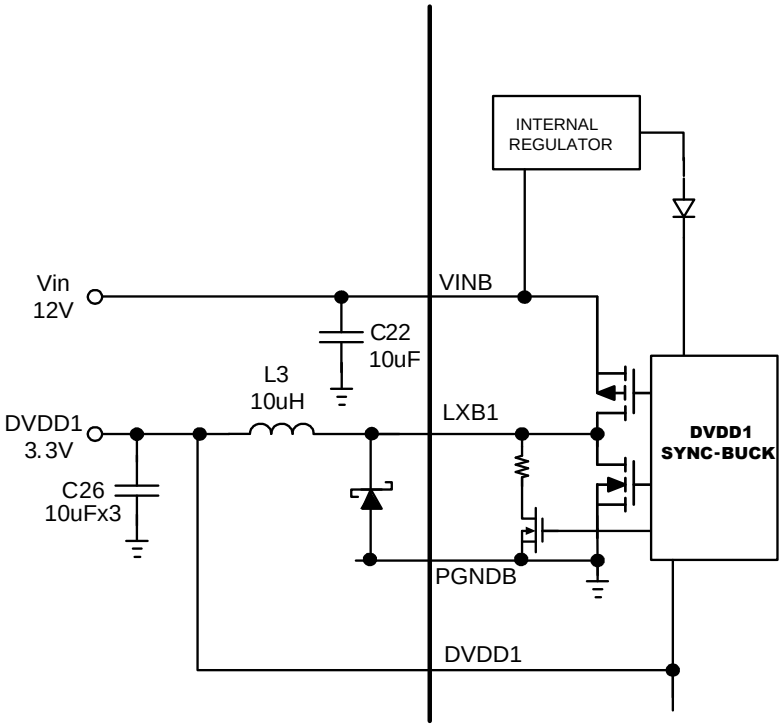


Figure 5. DVDD1 Control : Register 11h[7:6] = 00, initial frequency; Regeister 14h[4] = 0/1, Sync-Buck/Asyn-Buck;
OCP = 3.5A for 10uH coil inductor when Register 13h[1] = 0.

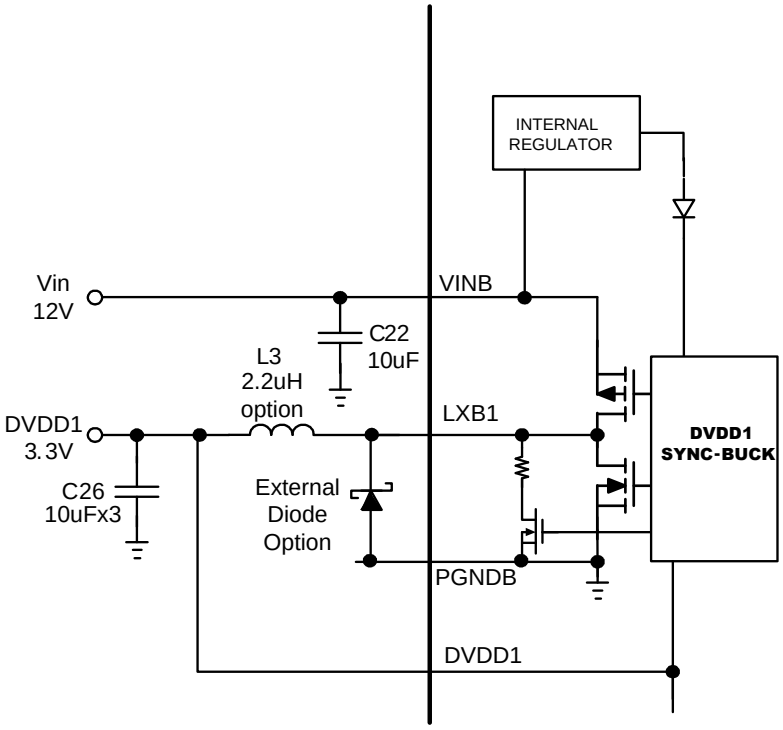


Figure 6. DVDD1 Control: Register 11h[7:6] = 01~11, initial frequency*2,*3;
Regeister 14h[4] = 0/1, Sync-Buck/Asyn-Buck;
OCP = 1.5A for 2.2μH chip inductor when Register 13h[1] = 1.

DVDD2 LV Buck Application Circuits with FB Detect Function

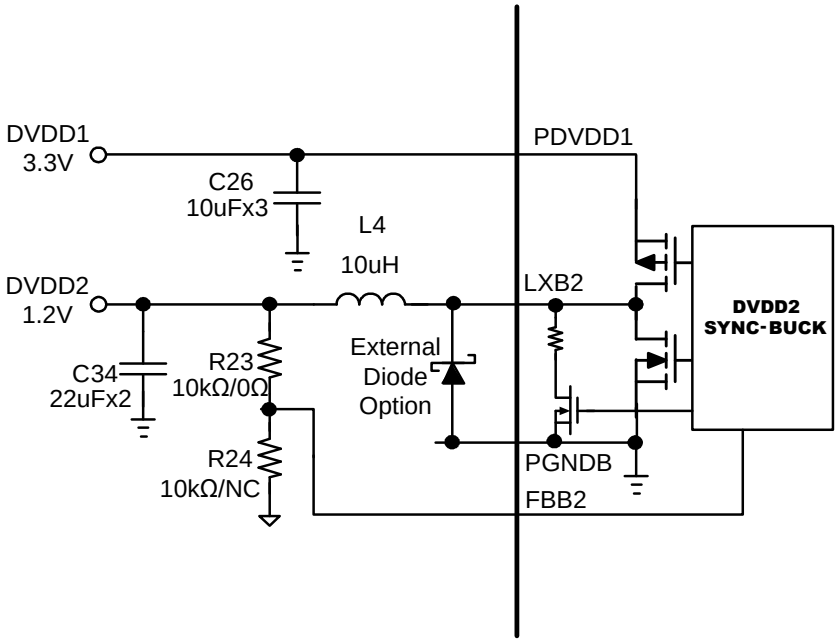


Figure 7. DVDD2 Control : Register 11h[5:4] = 00, initial frequency; Regeister 14h[3] = 0/1, Sync-Buck/Asyn-Buck;
OCP = 3.5A for 10μH coil inductor when Register 13h[0] = 0.

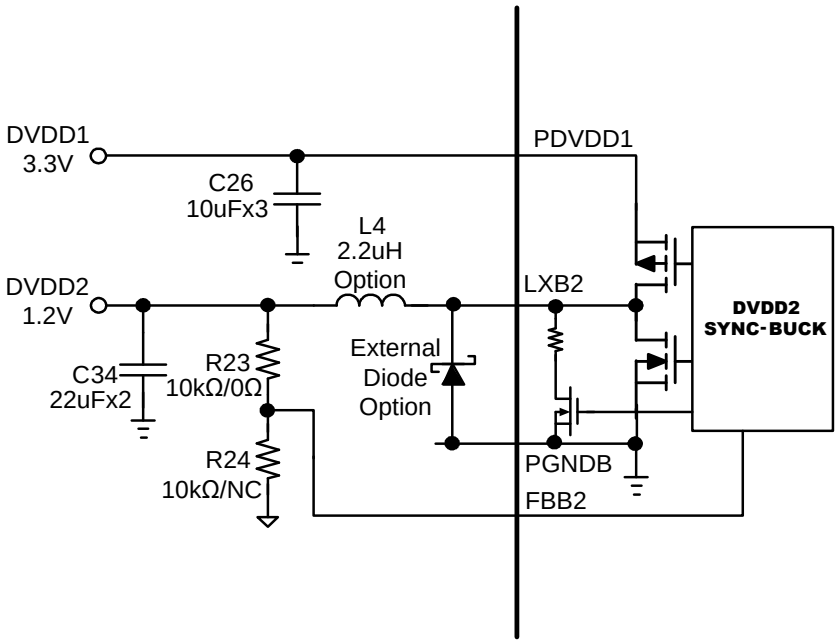


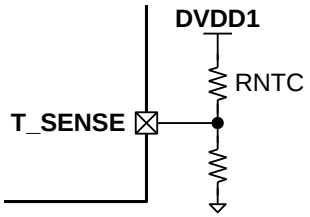
Figure 8. DVDD2 Control: Register 11h[5:4] = 01~11, initial frequency*2,*3;
Regeister 14h[3] = 0/1, Sync-Buck/Asyn-Buck;
OCP = 1.5A for 2.2μH chip inductor when Register 13h[0] = 1.

DVDD2 & DVDD3 Swap Function

If IC is power on and T_SENSE connects to temperature compensated resistor:

DVDD2 initial voltage=1.2V

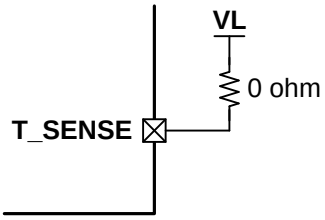
DVDD3 initial voltage=1.8V



If IC is power on and T_SENSE connects to VL pin

DVDD2 initial voltage=1.8V

D VDD3 initial voltage=0.96V



Digital Code (8-Bit)	Decimal	Hex.	Output Voltage				Reference Voltage
			FB Ratio : X = 1.0	FB Ratio : X = 1.5	FB Ratio : X = 2.0	FB Ratio : X	
0010 0111	39	27	0.80	1.000	1.20	0.40*(1+X)	0.40
0010 1000	40	28	0.82	1.025	1.23	0.41*(1+X)	0.41
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0010 1101	45	2D	0.92	1.150	1.38	0.46*(1+X)	0.46
0010 1110	46	2E	0.94	1.175	1.41	0.47*(1+X)	0.47
0010 1111	47	2F	0.96	1.200	1.44	0.48*(1+X)	0.48
0011 0000	48	30	0.98	1.225	1.47	0.49*(1+X)	0.49
0011 0001	49	31	1.00	1.250	1.50	0.50*(1+X)	0.50
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0011 1001	57	39	1.16	1.450	1.74	0.58*(1+X)	0.58
0011 1010	58	3A	1.18	1.475	1.77	0.59*(1+X)	0.59
0011 1011	59	3B	1.20	1.500	1.8	0.60*(1+X)	0.60
0011 1100	60	3C	1.22	1.525	1.83	0.61*(1+X)	0.61
0011 1101	61	3D	1.24	1.550	1.86	0.62*(1+X)	0.62
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0101 0111	87	57	1.76	2.200	2.64	0.88*(1+X)	0.88
0101 1000	88	58	1.78	2.225	2.67	0.89*(1+X)	0.89
0101 1001	89	59	1.80	2.250	2.70	0.90*(1+X)	0.90
0101 1010	90	5A	1.82	2.275	2.73	0.91*(1+X)	0.91
0101 1011	91	5B	1.84	2.300	2.76	0.92*(1+X)	0.92
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1000 0000	128	80	2.58	3.225	3.87	1.29*(1+X)	1.29
1000 0001	129	81	2.60	3.250	3.90	1.30*(1+X)	1.30

HAVDD HV Buck/OP Application Circuits

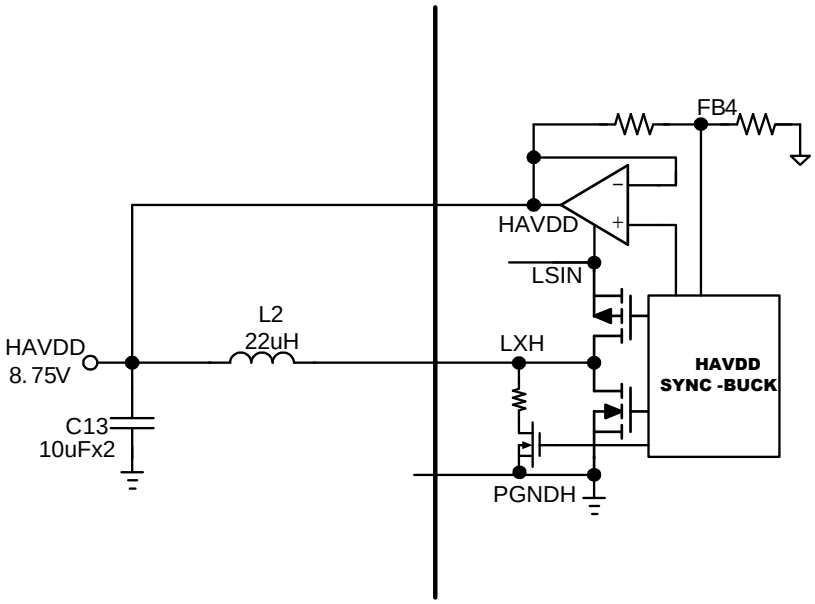


Figure 9. The HAVDD Control: Register 0Fh[0] = 0, DC/DC Sync- Buck Structure.

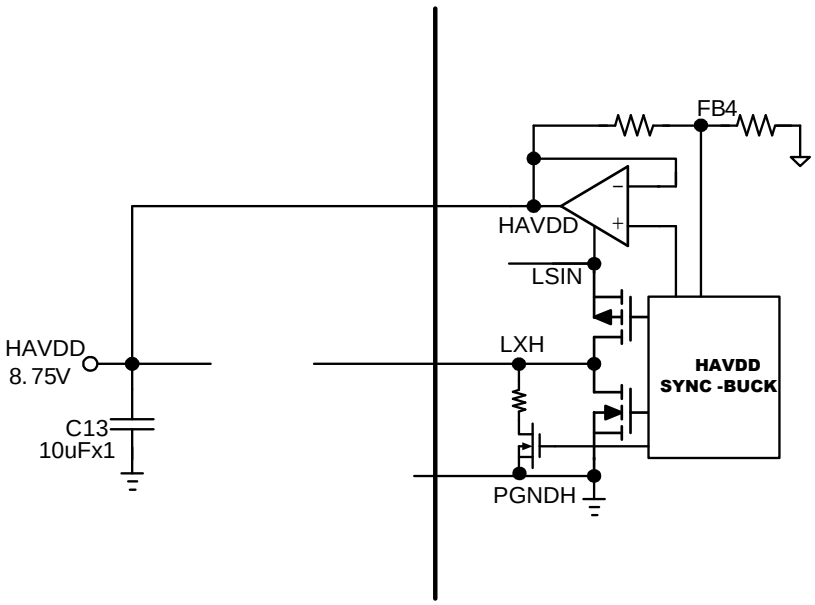


Figure 10. The HAVDD Control : Register 0Fh[0] = 1, OP Structure.

DVR and AVDD Trimming

DVR device address is 1001111 + R/W bit only when A0 = 1.

AVDD trimming address is decided by A0:

When A0 = 0, AVDD trimming address is 0100101 + R/W bit.

When A0 = 1, AVDD trimming address is 0110101 + R/W bit.

Write Command

7-bits value is for DVR and AVDD trimming data. The 7-bits DVR and AVDD trimming value are placed in the upper 7-bits of the byte. When receive the DVR or AVDD trimming write command and EN_ASW/WPN signal is high, IC will write data to both Memory and Register at LSB bit (P)=0 and write data to Register at LSB bit (P) = 1..

The Bank_Sel signal is low and data write to Bank1. The Bank_Sel signal is high and data write to Bank2.

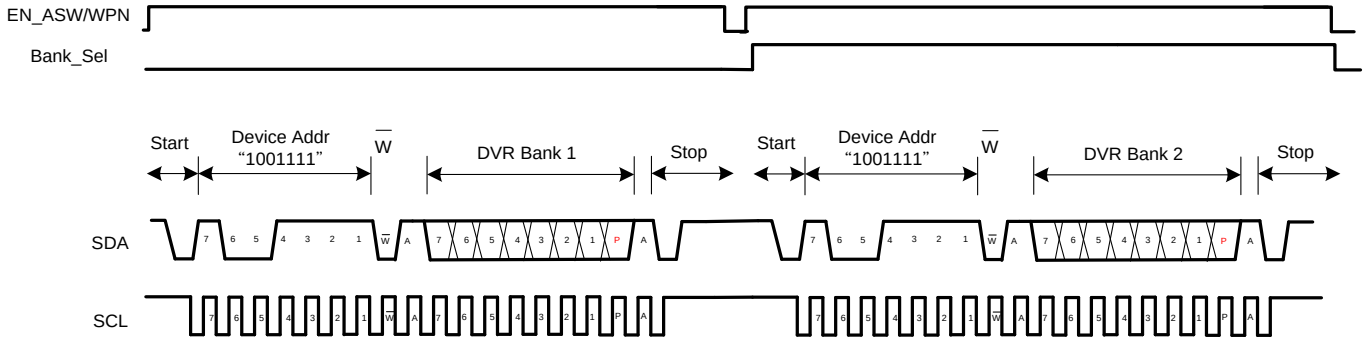


Figure 11. DVR and AVDD trimming write command

Read Command

7-bits value is for DVR and AVDD trimming data. The 7-bits DVR and AVDD trimming value are placed in the upper 7-bits of the byte. The LSB bit (X) must AND with 0 to prevent returning an incorrect value.

The Bank_Sel signal is low, I2C will transfer DVR and AVDD trimming Bank1 data. The Bank_Sel signal is high, I2C will transfer DVR and AVDD trimming Bank2 data.

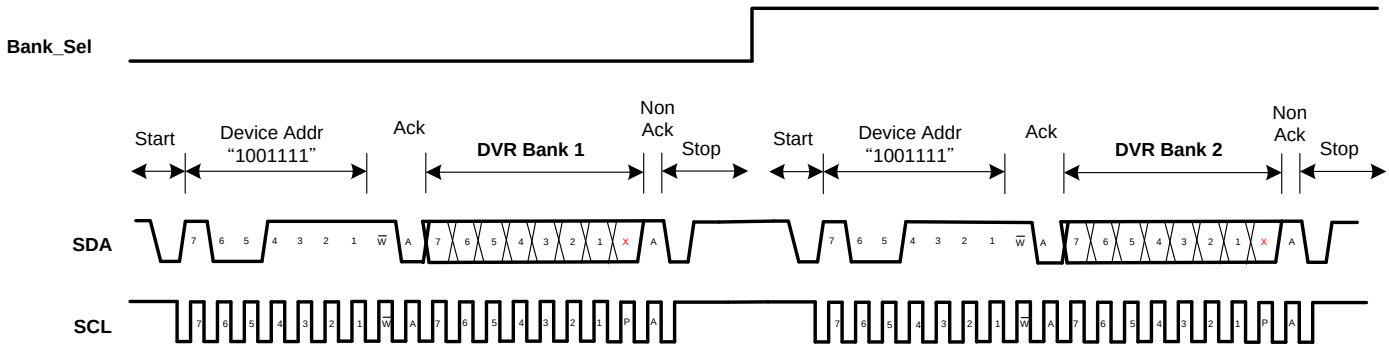


Figure 12. DVR and AVDD Trimming Read Command

DVR Block Diagram

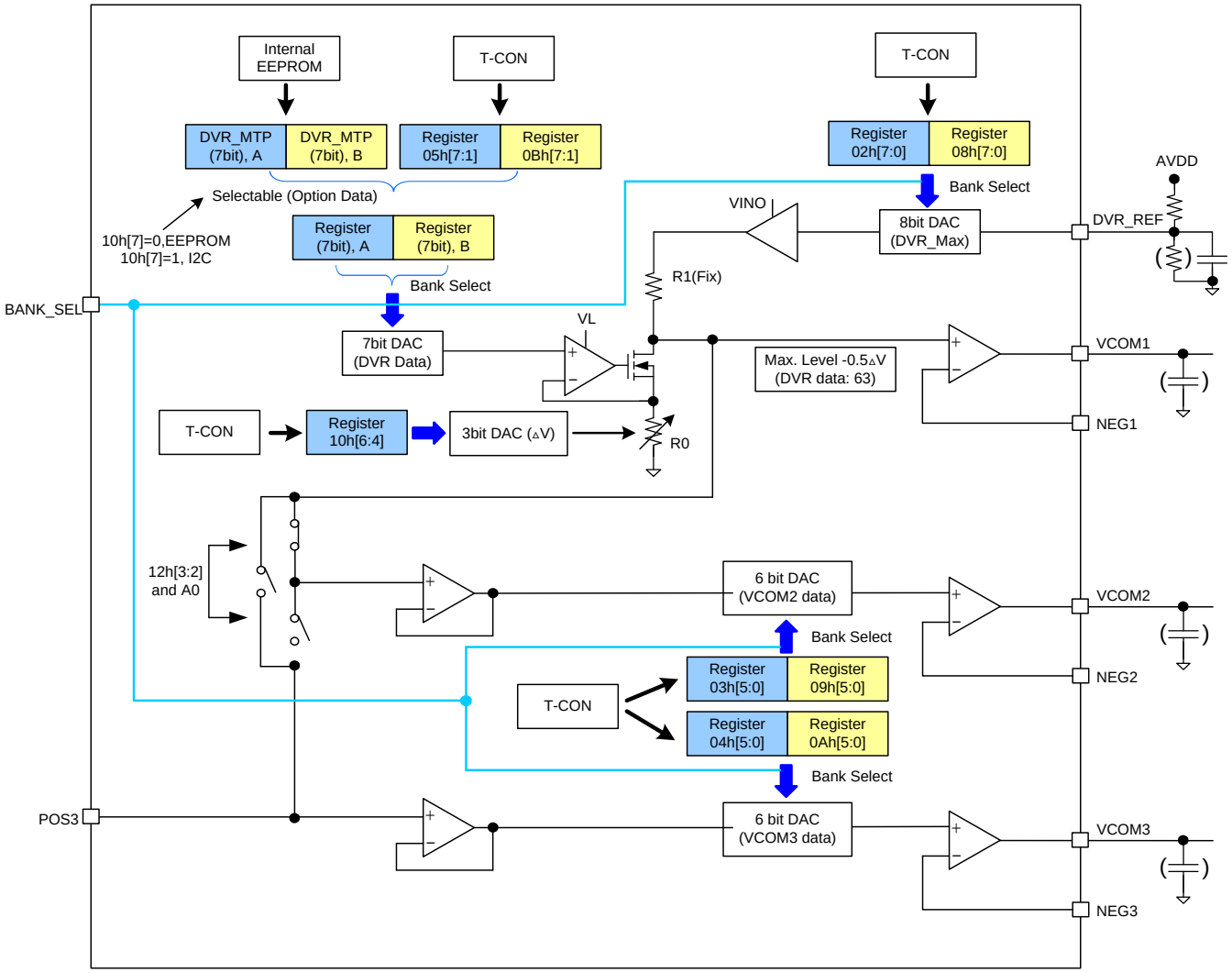


Figure 13. DVR Block Diagram

If internal reference voltage is floating, it will add pull low resistance.

Table 1. VCOM Reference Select: 12h[3:2] with A0.

A0 = 1, DVR ON			A0 = 0, DVR OFF		
[00]	VCOM1	DVR	[00]	VCOM1	Pull Low
	VCOM2	Pull Low		VCOM2	Pull Low
	VCOM3	POS3		VCOM3	POS3
[01]	VCOM1	DVR	[01]	VCOM1	Pull Low
	VCOM2	DVR		VCOM2	Pull Low
	VCOM3	POS3		VCOM3	POS3
[10]	VCOM1	DVR	[10]	VCOM1	Pull Low
	VCOM2	POS3		VCOM2	POS3
	VCOM3	POS3		VCOM3	POS3
[11]	VCOM1	DVR	[11]	VCOM1	POS3
	VCOM2	DVR		VCOM2	POS3
	VCOM3	DVR		VCOM3	POS3

LDO, Inverter, Reset and ASW Block Diagram

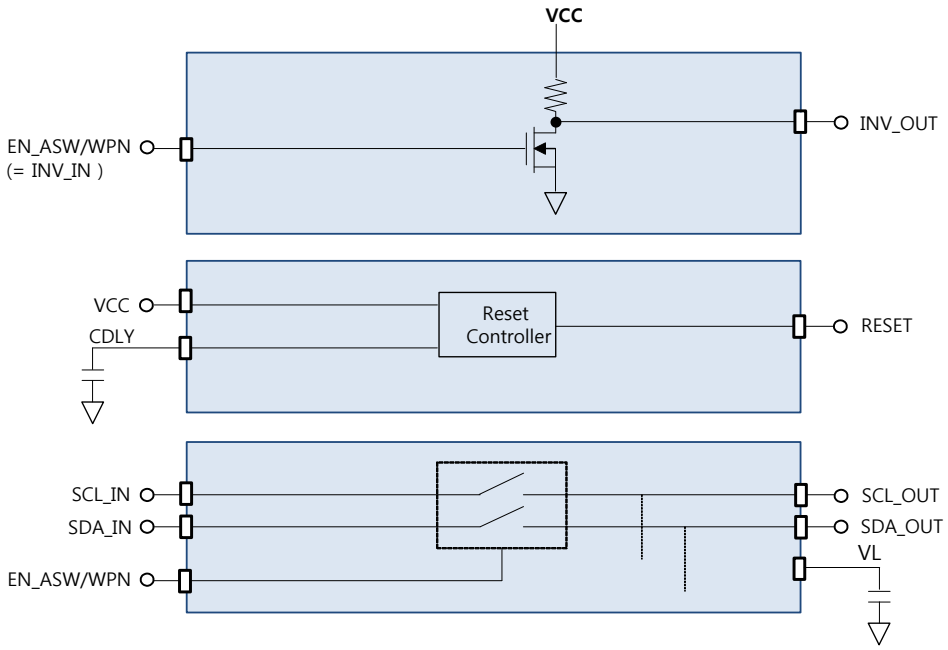


Figure 14. LDO, Inverter, RESET and EN_ASW/WPN Block Diagram

I2C Interface Block Diagram

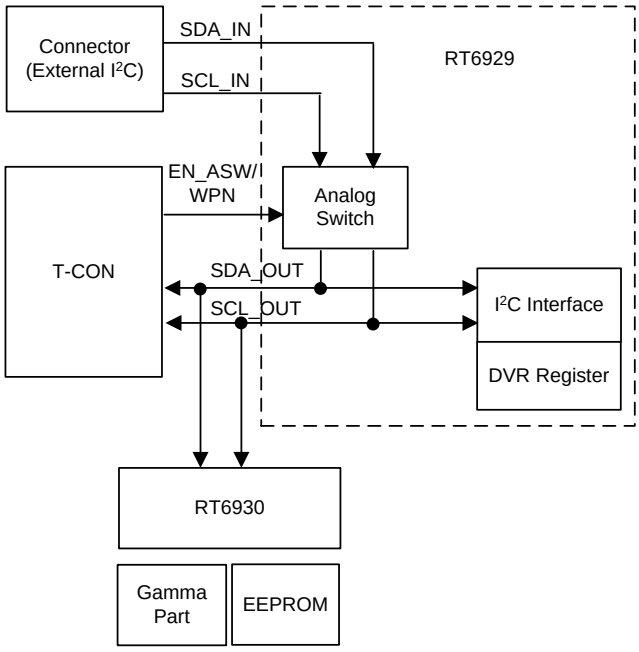


Figure 15. I2C Interface Block Diagram

AVDD Trimming Function Block Diagram

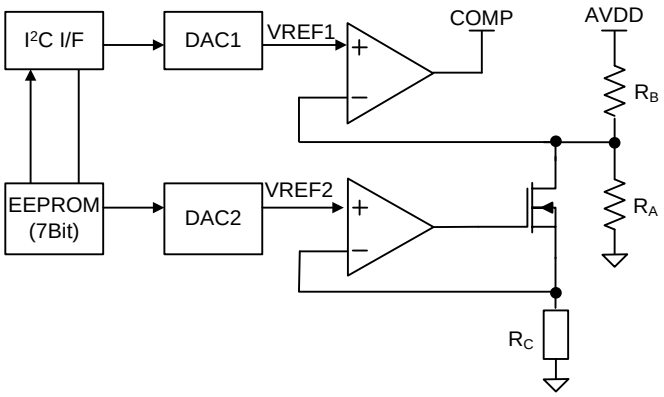


Figure 16. AVDD Trimming Function Block Diagram

$$AVDD\ (Code)=\left(\frac{R_A+R_B}{R_A}\right)\times VREF1+\left(\frac{R_B}{R_C}\right)\times VREF2\ \ (Default\ Setting)$$

Where VREF2=[VREF1×(1+Code)/128]

$$AVDD\ (Code)=\underbrace{\left(\frac{R_A+R_B}{R_A}+\frac{R_B}{R_C}\times\frac{64}{128}\right)\times VREF1}_{Default\ Value\ (AVDD\ Setting)}+\underbrace{\left(\frac{R_B}{R_C}\times\frac{Code-64}{128}\right)\times VREF1}_{Variable\ Value}$$

The 1bit variable value should become 0.1% Resolution as follows :

$$\underbrace{\left(\frac{R_B}{R_C}\times\frac{1}{128}\right)\times VREF1}_{Variable\ Value}=\frac{1}{1000}\times\underbrace{\left(\frac{R_A+R_B}{R_A}+\frac{R_B}{R_C}\times\frac{64}{128}\right)\times VREF1}_{Default\ Value\ (AVDD\ Setting)}$$

Thus, RC becomes as follow equations :

$$R_C=R_B\times\left(\frac{R_A}{R_A+R_B}\right)\times\frac{1000-64}{128}$$

Timing Sequence

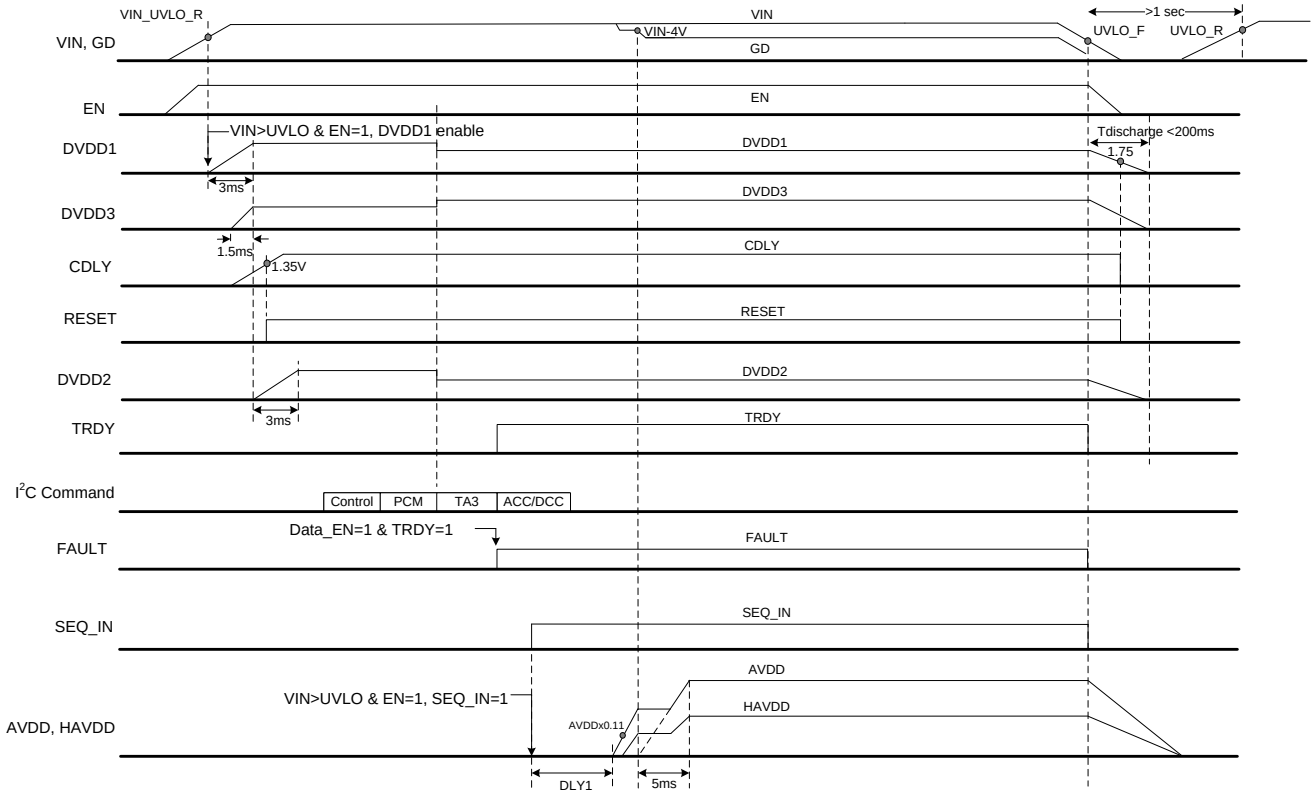


Figure 17. Normal Power On Sequence

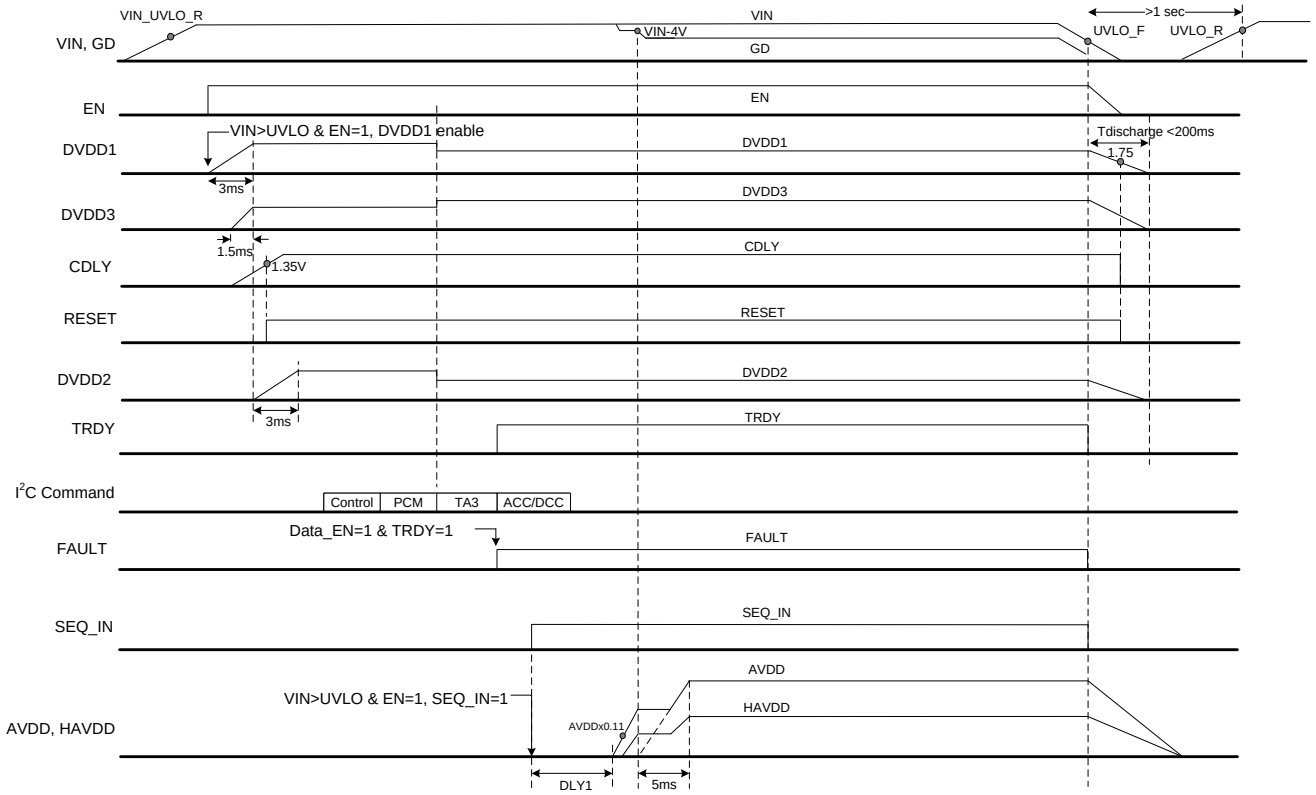


Figure 18. Normal Power On Sequence-EN Control

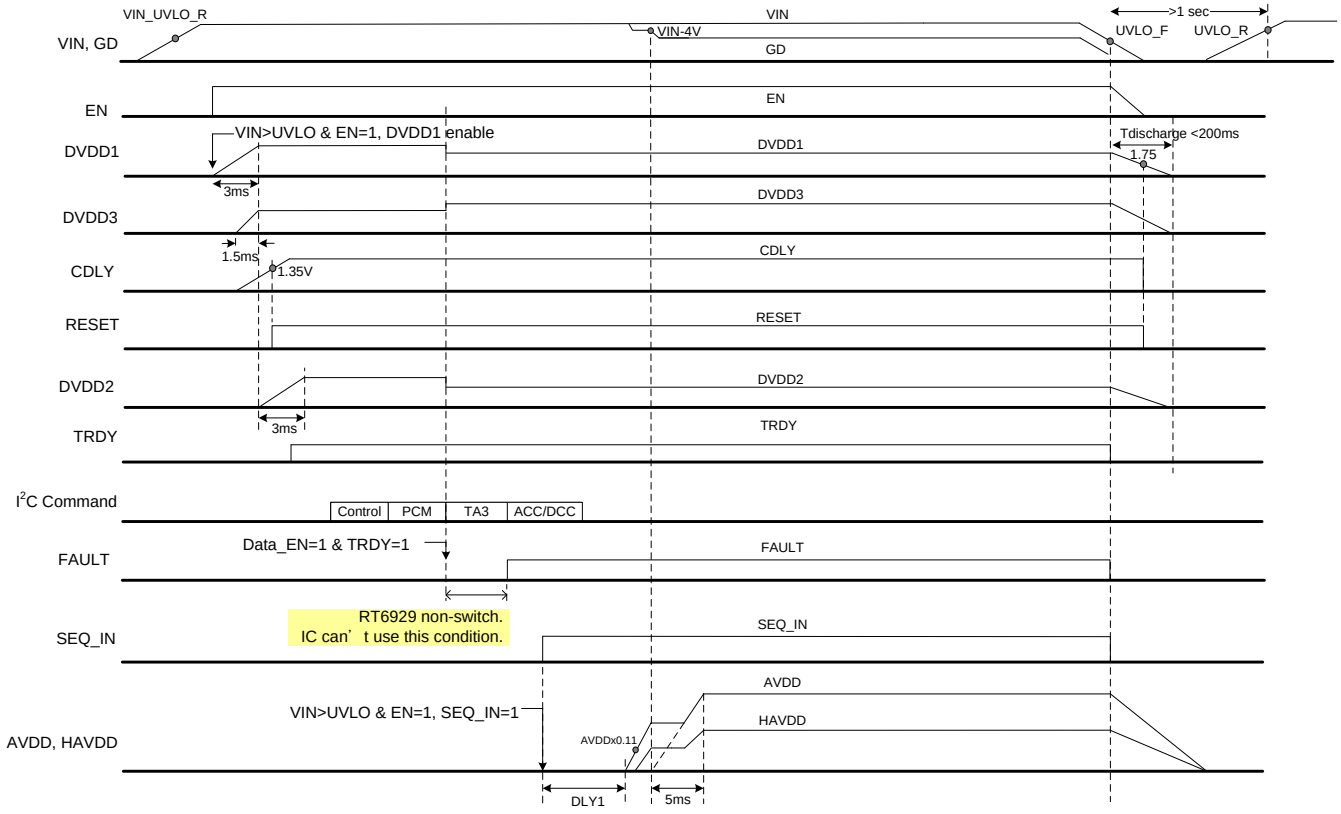


Figure 19. Normal Power On Sequence-TRDY Control

Table 2. IC Shutdown Function

Address	Name	Shutdown Operation	
		Channel Shutdown	IC Shutdown
00h	AVDD_BANK1	AVDD_ BANK1 = 00h	AVDD_ BANK1 > C1h AVDD_ BANK1< 86h
01h	HAVDD_ BANK1	HAVDD_ BANK1 = 00h	HAVDD_ BANK1 > C1h HAVDD_ BANK1 < 86h
06h	AVDD_ BANK2	AVDD_ BANK2 = 00h	AVDD_ BANK2 > C1h AVDD_ BANK2 < 86h
07h	HAVDD_ BANK2	HAVDD_ BANK2 = 00h	HAVDD_ BANK2 > C1h HAVDD_ BANK2 < 86h
0Ch	DVDD1	X	DVDD1 > 4Fh DVDD1 < 33h
0Dh	DVDD2	X	DVDD2 > 81h DVDD2 < 27h
0Eh	DVDD3	X	DVDD3 > 81h DVDD3 < 27h
			AVDD - HAVDD > 10.5V
			AVDD is off, GD will off.

Fault and Monitoring

The monitoring and update should be synchronized by STV. The update point is next frame of setting frame that is controlled by 2bit as shown in Table 3. The update data is the average of monitoring data during the setting frame and should be transferred in max 0.5ms.

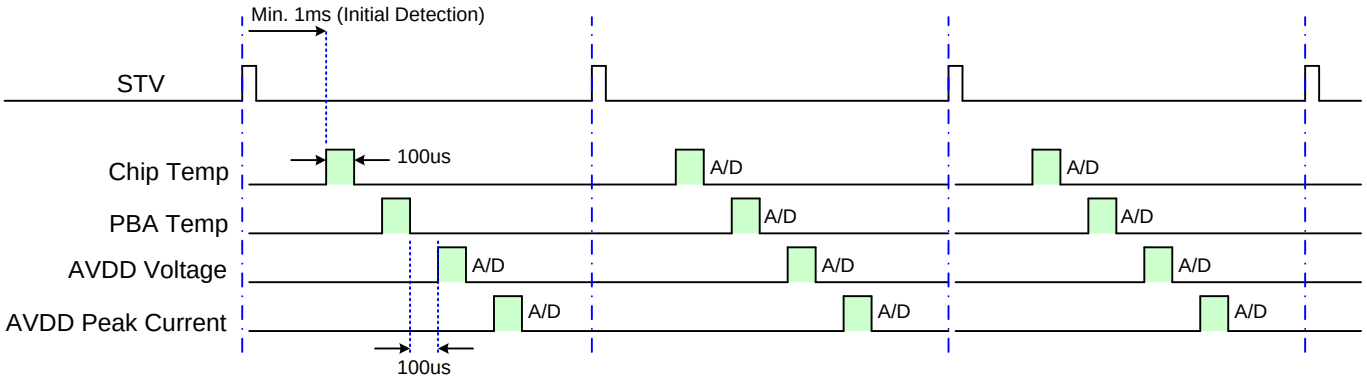


Figure 20. Data Monitoring Sequence

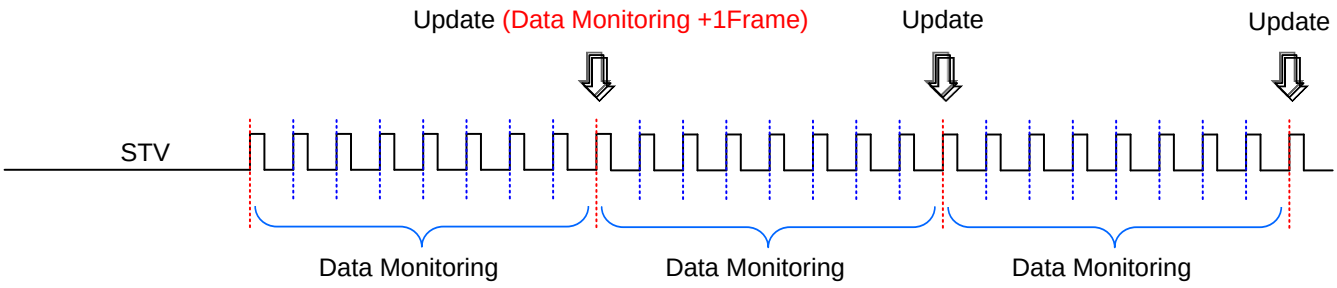


Figure 21. Data Monitoring and Update Period

Table 3. Update Period setting

Data of Register12h [1:0]	00	01	10	11
Frame	8 Frame	32 Frame	128 Frame	512 Frame

Absolute Maximum Ratings (Note 1)

- VINB, LXB1, HAVDD, LXH, LSIN, LSOUT to PGND ---------- –0.3 to 22V
- LXB2 to PGND ---------- –0.3 to 6V
- VCC, PDVDD1, DVDD1, DVDD3, FBB2, RESET, CDLY, TRDY, STV to AGND ---------- –0.3 to 6V
- EN, BANK_SEL, SDA_IN, SCL_IN, SDA_OUT, SCL_OUT, INV_OUT to AGND ---------- –0.3 to 6V
- EN_ASW/WPN, SEQ_IN, FAULT, T_SENSE, A0, COMP, VL to AGND ---------- –0.3 to 6V
- VCOM3, NEG3, VCOM2, NEG2, VCOM1, NEG1, POS3, DVR_REF, VINO to C_GND ---------- –0.3 to 26V
- LX, BSTA, AVDD to PGND ---------- –0.3 to 26V
- GD to LSIN ---------- –0.3 to –6V
- Power Dissipation, P_D @ T_A = 25°C
- WQFN-48L 6x6 ---------- 3.73W
- Package Thermal Resistance (Note 2)
- WQFN-48L 6x6, θ_{JA} ---------- 26.8°C/W
- WQFN-48L 6x6, θ_{JC} ---------- 1.3°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
- HBM (Human Body Model) ---------- 2kV
- MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} =12V, DVDD1 = 3.3V, DVDD2 = 1.2V, DVDD3 = 1.8V, AVDD = 17.5V, HAVDD = 8.75V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
General						
Supply Voltage	V_{IN}		9.5	--	14.7	V
VINB Under-Voltage Lockout Threshold	V_{UVLO}	VINB falling	7.7	8.15	8.6	V
		VINB rising	8.5	8.8	9.1	
VINB UVLO Hysteresis	V_{HYUVLO}		500	650	800	mV
AVDD Input Voltage Range	V_{s_AVDD}		VIN x 1.14	--	19.4	V
PDVDD1 Input Voltage Range	V_{s_PDVDD1}		2.6	--	4	V
VINB Quiescent Current	I_{QVINB}	No Switching	--	4	--	mA
Quiescent Current into PDVDD1	$I_{QPDVDD1}$	No Switching	--	1	--	μA
Quiescent Current into VINO	I_{QVINO}	No Switching	--	9	--	mA
VL Output Voltage	V_L		4.5	5	5.5	V
VL Start Threshold Voltage	V_{L_START}		3.8	4.1	4.4	V
VL Stop Threshold Voltage	V_{L_STOP}		3.2	3.5	3.8	V
VL UVLO Hysteresis	V_{HY_VL}		0.45	0.6	0.75	V
Thermal Shutdown	T_{SD}	Junction Temp. rising	150	165	180	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C
EEPROM Write Guarantee			1000	--	--	count
Internal Oscillator						
Oscillator Frequency11	f_{OSC11}	Initial Frequency “00”	360	450	540	kHz
Oscillator Frequency12	f_{OSC12}	Initial Frequency “01”	480	600	720	kHz
Oscillator Frequency13	f_{OSC13}	Initial Frequency “10”	600	750	900	kHz
Oscillator Frequency14	f_{OSC14}	Initial Frequency “11”	720	900	1080	kHz
Oscillator Frequency21 (DVDD1,2)	f_{OSC21}	Initial Frequency “00” ×2	720	900	1080	kHz
Oscillator Frequency22 (DVDD1,2)	f_{OSC22}	Initial Frequency “01” ×2	960	1200	1440	kHz
Oscillator Frequency23 (DVDD1,2)	f_{OSC23}	Initial Frequency “10” ×2	1200	1500	1800	kHz
Oscillator Frequency24 (DVDD1,2)	f_{OSC24}	Initial Frequency “11” ×2	1440	1800	2160	kHz
Oscillator Frequency31 (DVDD1,2)	f_{OSC31}	Initial Frequency “00” ×3	1080	1350	1620	kHz
Oscillator Frequency32 (DVDD1,2)	f_{OSC32}	Initial Frequency “01” ×3	1440	1800	2160	kHz
Oscillator Frequency33 (DVDD1,2)	f_{OSC33}	Initial Frequency “10” ×3	1800	2250	2700	kHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator Frequency34 (DVDD1,2)	f_{OSC34}	Initial Frequency “11” ×3	2160	2700	3240	kHz
Boost Converter(AVDD)						
Output Voltage Range	AVDD		VIN x 1.14	--	19.4	V
Maximum Duty Cycle	D_{MAX_AVDD}		81	95	99	%
AVDD Voltage (Default)	V_{AVDD}	No load, ±1.0% Error	17.325	17.5	17.675	V
AVDD Input Bias Current	I_{BIAS_AVDD}		--	380	--	μA
AVDD Fault Trip Level Falling	V_{AVDD_OLP}	AVDD falling	AVDD x 0.816	AVDD x 0.85	AVDD x 0.884	V
LX ON-Resistance 1	$R_{DS(ON)1}$	LX-PGHD, I_{LX} = 800mA	100	150	200	mΩ
LX ON-Resistance 2	$R_{DS(ON)2}$	AVDD-LX, I_{LX} = 800mA	100	150	200	mΩ
Load Switch ON-Resistance	R_{LSW}	I_{LSW} = 800mA	90	120	150	mΩ
LX Current Limit	I_{LIM}	DATA = “3”, *see OCP table	3	3.75	4.5	A
	I_{LIM}	DATA = “5”, *see OCP table	4	5	6	A
LSW Leakage Current	I_{LSW}	LS_IN-LS_OUT = 20V	--	--	5	μA
Load Switch Soft Start Period	t_{SS_LS}	Internal mode	2.4	3	3.6	ms
Load Regulation	LRAVDD	0 < I_{LOAD} < 2A	–1	--	1	%
Line Regulation	dV_{AVDD_R}	V_{IN} = 9.5 to 14.7V (I_{LOAD} = 0.3A)	–1	--	1	%
Over-Voltage Protection	V_{OVP}	AVDD rising	20	21	22	V
Over-Voltage Protection Hysteresis	V_{HYAVDD_OVP}		0.6	1.1	1.6	V
GD Voltage	V_{GD}	VIN – VGD	5	6	7	V
GD Sink Current	I_{GD}		8	10	12	μA
GD Pull-up Resistance	R_{GD}		5.5	11	16.5	kΩ
Output Resolution	Res		--	0.1	--	V
Integral Non-Linearity	I_{NL}		–1	--	1	LSB
Differential Non-Linearity	D_{NL}		–1	--	1	LSB
AVDD Calibrator Resolution	Cal_Res	7bit resolution	--	AVDD x 0.1%	--	-
AVDD to PGND Discharging Resistance	R_{AVDD_DCHG}		0.7	1.4	2.1	kΩ
Soft Start Period	t_{SS_AVDD}		4	5	6	ms
Synchronous BUCK Converter (HAVDD)						
Output Voltage Range	HAVDD		6.75	--	9.7	V
HAVDD Voltage	V_{HADD}	No load, ±1.0% Error	8.663	8.75	8.837	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
HAVDD Fault Trip Level Falling	$V_{HAVDD\ falling}$		HAVDD x 0.816	HAVDD x 0.85	HAVDD x 0.884	V
LXH ON-Resistance H/L	R_{DSONH}	I_{LXH} = 200mA, Min/Max	--	1	--	Ω
LXH Current Limit	$I_{LIM\_UGATE\_LXH}$		1.2	--	--	A
	$I_{LIM\_LGATE\_LXH}$		--	--	–1.2	
LXH Leakage Current	I_{LKH_H}	L_{XH} = 0V	--	--	5	μA
	I_{LKH_L}	L_{XH} = 12V	--	--	5	μA
Load Regulation	LRHAVDDsk	HAVDD = 8.75V, –0.5A < I_{OUT} < 0A	–1	--	1	%
	LRHAVDDsr	HAVDD = 8.75V, 0A < I_{OUT} < 0.5A	–1	--	1	%
Line Regulation		V_{IN} = 9.5 to 14.7V (I_{LOAD} = 0.1A)	–1	--	1	%
Output Resolution	Res		--	0.05	--	V
Over-Voltage Protection 1	V_{OVPH1}		9.9	--	10.5	V
Over-Voltage Protection 2	V_{OVPH2}		AVDD – 10.5	--	AVDD – 9.9	V
Integral Non-Linearity	I_{NL}		–1	--	1	LSB
Differential Non-Linearity	DNL		–1	--	1	LSB
HAVDD to PGND Discharging Resistance	R_{HAVDD_DCHG}		3.5	7	14	kΩ
HAVDD Operational Amplifier						
Current LIMIT	$I_{HAVDDsr}$	HAVDD-OPOUT_HAVDD are shorted (Source)	500	650	--	mA
	$I_{HAVDDsk}$	HAVDD-OPOUT_HAVDD are shorted (Sink)	--	–650	–500	mA
Continuous Current	I_{CNT_HAVDD}		--	300	--	mA
VCOM Operational Amplifier						
Supply Current	I_{AVDD}	Buffer configuration, no load, VCOM1-3 active	--	3	--	mA
Output Voltage Swing High (VCOMx)	V_{OH}	I_{COM} = –20mA	VINO – 0.8	VINO – 0.4	VINO – 0.2	V
Output Voltage Swing Low (VCOMx)	V_{OL}	I_{COM} = 20mA	0.2	0.4	0.8	V
Short Current (VCOMx)	I_{SRC_AMP}	Buffer configuration, V_{POS} = VINO/2	500	650	--	mA
	I_{SNK_AMP}	Buffer configuration, V_{POS} = VINO/2	--	-650	-500	mA
Continuous Current	I_{CNT_VCOM}		--	250	--	mA
Load Regulation	LRAMP	–50mA< I_{OUT} < 50mA	–3	--	3	%
Power Supply Rejection Ratio	PSRR	f = 10kHz, Load R_C = 10Ω10nF	75	--	--	dB

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Common Mode Rejection Ratio	CMRR	f = 10kHz, Load R_C = 10Ω 10nF	60	--	--	dB
Zero cross Frequency	UGCF	Load R_C = 10Ω 10nF	5	--	--	MHz
Phase Margin	PM	Load R_C = 10Ω 10nF	45	--	--	Deg.
Open Loop Gain	OLG	Load R_C = 10Ω 10nF	100	--	--	dB
VCOM Slew Rate	SR	Negative Swing	50	--	--	V/μs
VCOM Propagation Delay	TD_AMP	Negative Input	--	--	100	ns
NEGx Input Bias Current	$I_{NEGx,}$	V_{NEGx} = VINO/2	–0.5	0	0.5	μA
POS3 Input Current	I_{POS3}		–0.5	0	0.5	μA
VCOM2,3 Voltage Resolution	$V_{COM2,3VR}$		--	6	--	Bit
Output Error (VCOM1)	OE1		Please refer to DVR Special spec.			mV
Output Error (VCOM2,3)	OE2		Please refer to VCOM Special spec.			mV
Offset Error		DVR data “63”	–20	--	20	mV
Integral Non-Linearity	INL		–1	--	1	LSB
Differential Non-linearity	DNL		–1	--	1	LSB
DVR Calibrator						
VCOM1 Voltage Resolution	VCOM1VR		--	8	--	Bit
DVR_REF Input Current	I_{DVR_REF}		–0.5	0	0.5	μA
DVR_REF Input Range	V_{DVR_REF}		2	0	VINO	V
DVR Voltage Resolution	SETVR		--	7	--	BIT
DVR Integral Non-linearity	V_{SET_INL}		–1	--	1	LSB
DVR Differential Non-linearity	V_{SET_DNL}		–1	--	1	LSB
Maximum Adjustment width	ADW	Setting by 0.5Vstep	0.5	--	4	V
DVR Writing Cycle time	tw		--	10	20	ms
DVR_OUT Setting Time	t_{O_SET}	95% of final value	--	20	--	μs
Sync. Buck Converter (DVDD1)						
Output Voltage Range1	DVDD1		2.6	--	4	V
DVDD1 Output Voltage	DVDD1O	No load, ±2% Error, Default output	3.234	3.3	3.366	V
Maximum Duty Cycle	D_{MAX_DVDD1}		81	90	99	%
Minimum On Time	$t_{ON\_MIN\_DVDD1}$		--	100	--	ns
DVDD1 Fault Trip Level Falling	V_{DVDD1_OLP}	DVDD1 falling	DVDD1 x 0.816	DVDD1 x 0.85	DVDD1 x 0.884	V
DVDD1 Input Bias Current	I_{DVDD1}		--	450	--	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LXB1 ON-Resistance High	R_{ONB1H}	LXB1= 200mA	75	150	300	mΩ
LXB1 ON-Resistance Low	R_{ONB1L}	LXB1= 200mA	75	150	300	mΩ
LXB1 Current Limit1	I_{LIMB11}	Frequency select = *2,*3	1.5	2.2	2.9	A
LXB1 Current Limit2	I_{LIMB12}	Initial Frequency	3.5	5	6.5	A
LXB1 to PGNDB1 Discharging Resistance	R_{LXB1_DCHG}		0.3	0.6	1.2	kΩ
LXB1 Leakage Current	I_{LKB1}		--	--	5	μA
Load Regulation	L_{RVDD1}	DVDD1 = 3.3V, 0A< I_{OUT} < 2A	–1	--	1	%
Line Regulation	d_{VVDD1_R}	V_{IN} = 9 to 14.7V (I_{LOAD} = 0.2A)	–1	--	1	%
Output Resolution	Res		--	0.05	--	V
Over Voltage Protection	OVP		4.75	5	5.25	V
Over Voltage Protection Hysteresis	$V_{HYDVDD1\_OVP}$		--	0.2	--	V
Soft Start Periodz	t_{SS_DVDD1}		2.4	3	3.6	ms
Sync. Buck Converter (DVDD2)						
Output Voltage Range2	V_{DVDD2}		0.8	--	2.6 (PVDD 1 x 0.8)	V
DVDD2 Output Voltage	V_{DVDD2O}	No load, ±2% Error, Default output	1.176	1.24	1.224	V
FBB2 Regulation Voltage1	V_{FBB21}	DVDD2 uses external resistor and T_SENSE connects to temperature compensated resistor.	588	600	612	mV
FBB2 Regulation Voltage2	V_{FBB22}	DVDD2 uses external resistor and T_SENSE connects to VL pin.	882	900	918	mV
Maximum Duty Cyclez	D_{MAX_DVDD2}		81	90	99	%
Minimum On Time	$t_{ON\_MIN\_DVDD2}$		--	120	--	ns
FBB2 Fault Trip Level Falling		V_{FBB2} falling	VFBB2 x 0.816	VFBB2 x 0.85	VFBB2 x 0.884	V
LXB2 ON-Resistance High	R_{ONB2H}	LXB2 = 200mA	50	150	270	mΩ
LXB2 ON-Resistance Low	R_{ONB2L}	LXB2 = 200mA	50	150	270	mΩ
LXB2 Current Limit	I_{LIMB21}	Frequency select = *2,*3	1.5	2.2	2.9	A
LXB2 Current Limit	I_{LIMB22}	Initial Frequency	3.5	5.0	6.5	A
LXB2 to PGNDB2 Discharging Resistance			0.3	0.6	1.2	kΩ
LXB2 Leakage Current	I_{LKB2}		--	--	5	μA
Load Regulation	LRDVDD2	DVDD2 = 1.2V, 0A< I_{OUT} < 2A	–1	--	1	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation	d_{VDVDD2_R}	PDVDD1 = 2.5 to 4.5V (I_{LOAD} = 0.2A)	–1	--	1	%
Output Resolution	Res		--	0.02	--	V
Soft Start Period	t_{SS_DVDD2}		2.4	3	3.6	ms
Linear Regulator (DVDD3)						
Output Voltage Range3	V_{DVDD3}		0.8	--	2.6	V
DVDD3 Voltage	V_{DVDD3}	No load, ±2.0% Error, Default output	1.764	1.8	1.836	V
DVDD3 Fault Trip Level Falling		DVDD3 falling	DVDD3 x 0.816	DVDD3 x 0.85	DVDD3 x 0.884	V
Dropout Voltage	V_{DROP}	DVDD3 = DVDD1-0.2, I_{DD3} = 200mA	--	200	500	mV
Load Regulation	LRDVDD3	DVDD3 = 1.8V, 1mA < I_{LOAD} <250mA	–1	--	1	%
Line Regulation	d_{VDVDD3_R}	DVDD1 = 2.5V to 4.5V, I_{LOAD} = 0.2A	–1	--	1	%
Output Resolution			--	0.02	--	%
Soft Start Period	t_{SS_DVDD3}		1.2	1.5	1.8	ms
Reset						
CDLY Source Current	I_{DLY}		4.25	5	5.75	μA
CDLY Threshold Voltage (VCDLY rising)	V_{DLY}		1.215	1.35	1.485	V
CDLY Threshold Voltage (HYS)	V_{DLY_HYS}		0.3	0.4	0.5	V
RESET Logic Output High Voltage	V_{RESET_H}		--	VCC	--	V
RESET Logic Output Low Voltage	V_{RESET_L}		--	GND	--	V
Reset Threshold (VCC falling)	V_{RST}		1.6	1.75	1.9	V
Reset Threshold (HYS)	V_{RST_HYS}		0.2	0.3	0.4	V
Analog Switch						
Switch OFF Leakage Current	I_{leak_ASW}		--	--	1	μA
Switch On-Resistance	$R_{DS(ON)}$	I_{LOAD} = 10mA	5	10	15	Ω
Propagation Delay Bus-to-Bus	t_{PHL}, t_{PLH}		--	5	20	ns
Output Enable Time	t_{PZL}, t_{PZH}		--	3	200	ns
Output Disable Time	t_{PLZ}, t_{PHZ}		--	3	200	ns
Inverter						
Output High Voltage	V_{OUT_H}	I_{OUT} = 2mA	VCC – 0.2	VCC – 0.1	VCC – 0.01	V
Output Low Voltage	V_{OUT_L}	I_{OUT} = 2mA	0.01	0.1	0.2	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay	Tdelay		--	--	100	ns
Monitoring Function						
AVDD Voltage Resolution	Res_V		--	4	--	Bit
Voltage Monitoring tolerance	TL_V		-3	--	3	%
LX Current Resolution	RES_I		--	4	--	Bit
Current Monitoring tolerance	TL_I		–20	--	20	%
Die Temperature Resolution	RES_DT		--	4	--	Bit
Die Temperature Monitoring tolerance	TL_DT		–7	--	7	%
PBA Temperature Resolution	RES_PT		--	2	--	Bit
PBA Temperature Monitoring 0°C Sensing Voltage	V_{T0_Sense}		–5%	0.401	5%	V
PBA Temperature Monitoring 25°C Sensing Voltage	V_{T25_Sense}		–5%	1.115	5%	V
PBA Temperature Monitoring 50°C Sensing Voltage	V_{T50_Sense}		–5%	1.999	5%	V
Sequence Control Pins SEQ_IN,FAULT						
Pull Up Resistance (FAULT)	R_{FLT}		100	--	--	kΩ
Pull Down Resistance (SEQ_IN)	R_{SEQ}		100	--	--	kΩ
High-level Input Voltage (SEQ_IN, FAULT)	V_{IH}		2	--	--	V
Low-level Input Voltage (SEQ_IN, FAULT)	V_{IL}		--	--	1	V
Pull low Voltage (FAULT)	V_{ON}	I_{IN} = 3mA	--	--	0.4	V
Fault Trigger Duration	T_{FAULT}		2.5	3	3.5	ms
Logic Signal EN						
High-level Input Voltage	V_{IH_EN}		1.6	--	--	V
Low-level Input Voltage	V_{IL_EN}		--	--	0.75	V
Logic Signals SDA_OUT, SCL_ OUT, EN_ASW/WPN, TRDY, BANK_SEL, EN, A0, SEQ_IN						
High-level Input Voltage	V_{IH}		2	--	--	V
Low-level Input Voltage	V_{IL}		--	--	1	V
A0 Pull-Up Resistance	R_{A0}	VL Pull Up	100	--	--	kΩ
TRDY Pull-down Resistance	R_{TRDY}		100	--	--	kΩ
BANK_SEL Input current	I_{BANK}	V_{BANK_SEL} = 2V	9.3	13.3	17.3	μA
EN Input Current	I_{EN}	I_{EN} = 0V, 100kΩ Pull Up (VL)	–65	-50	–35	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
EN_ASW/WPN Input Current	Iin	EN_ASW/WPN = BANK_SEL = 2V	9.3	13.3	17.3	μA
STV Pull Down Resistance	R_{STV}		100	--	--	kΩ
SDA_IN, SCL_IN Input Current	Iin		–2	0	2	μA
SDA_ACK ON Voltage	V_{ACK}	I_{SDA} = 3mA	--	--	0.4	V
SCL Frequency	F_{CLK}		--	--	1	MHz
SCL High Period	t_{HIGH}		0.3	--	--	μs
SCL Low Period	t_{LOW}		0.4	--	--	μs
SCL Rise Time	t_R		--	--	0.12	μs
SCL Fall Time	t_F		--	--	0.12	μs
Start Condition Hold Time	t_{HD_STA}		0.25	--	--	μs
Start Condition Setup Time	t_{SU_STA}		0.25	--	--	μs
SDA Hold Time	t_{HD_DAT}		50	--	--	ns
SDA Setup Time	t_{SU_DAT}		50	--	--	ns
ACK Delay Time	t_{PD}		--	--	0.35	μs
ACK Hold Time	t_{HD}		--	0.1	--	μs
Stop Condition Setup Time	t_{SU_STO}		0.25	-	--	μs
Bus Free Time	t_{BUF}		0.5	-	--	μs
Bus Capacitance	Cb		--	--	400	pF
Spike Rejection Pulse Width	tl		--	0.05	--	μs

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

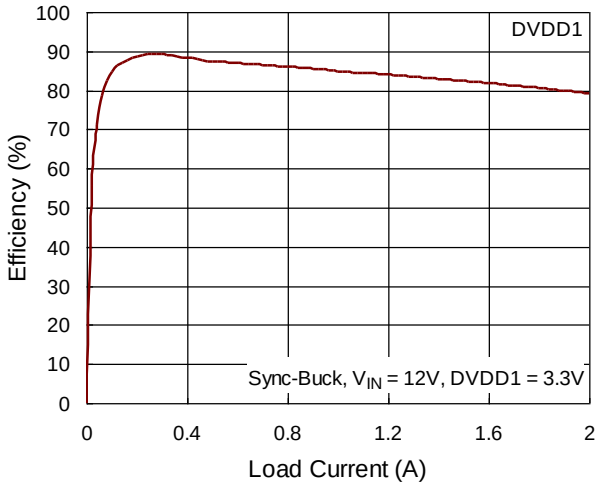
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

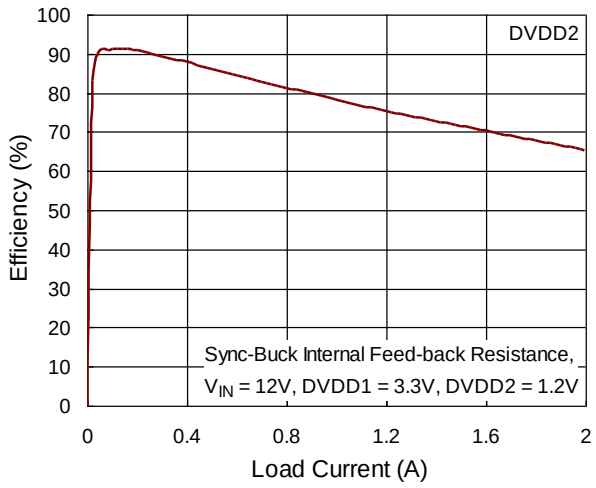
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

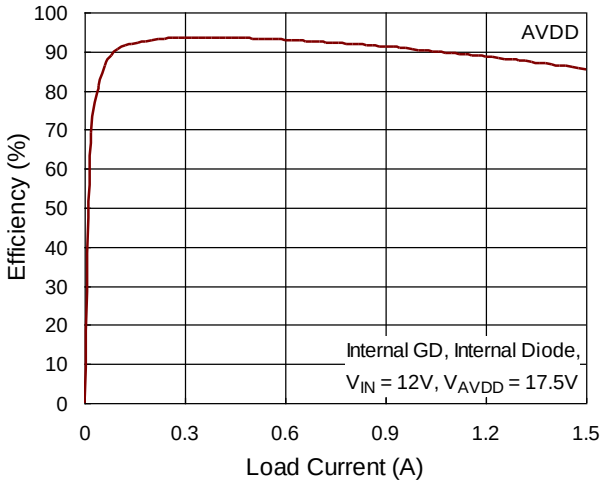
Buck Efficiency vs. Load Current



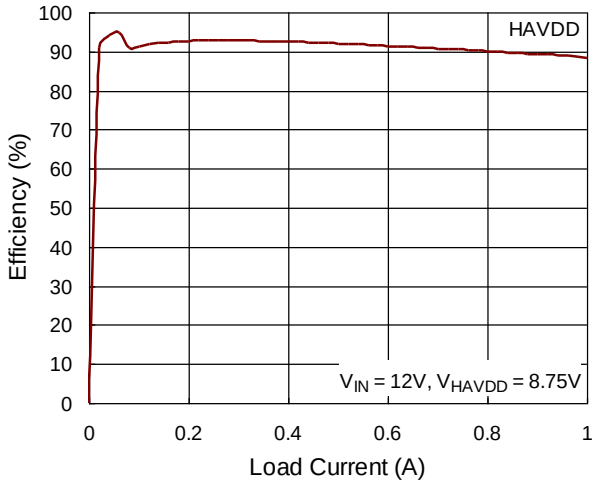
Buck Efficiency vs. Load Current



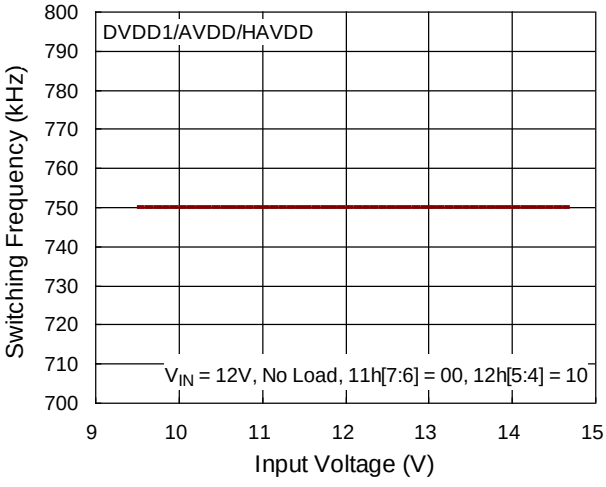
Boost Efficiency vs. Load Current



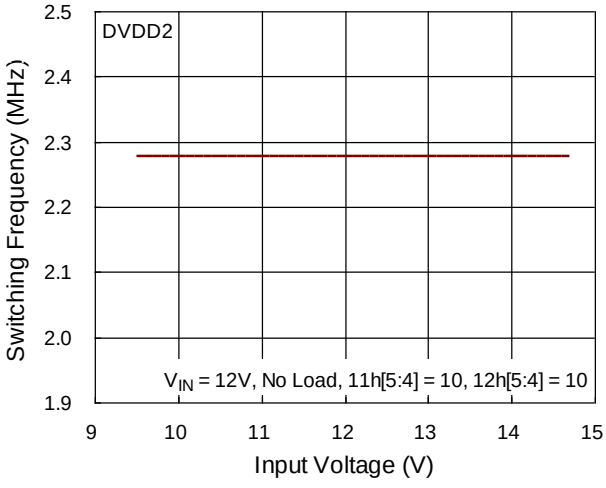
Buck Efficiency vs. Load Current



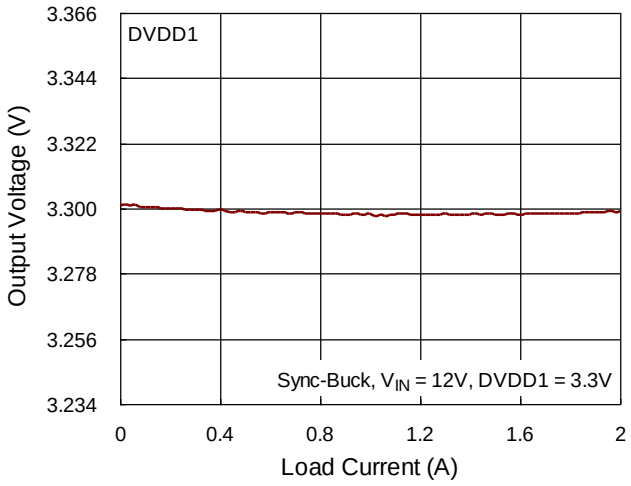
Switching Frequency vs. Input Voltage



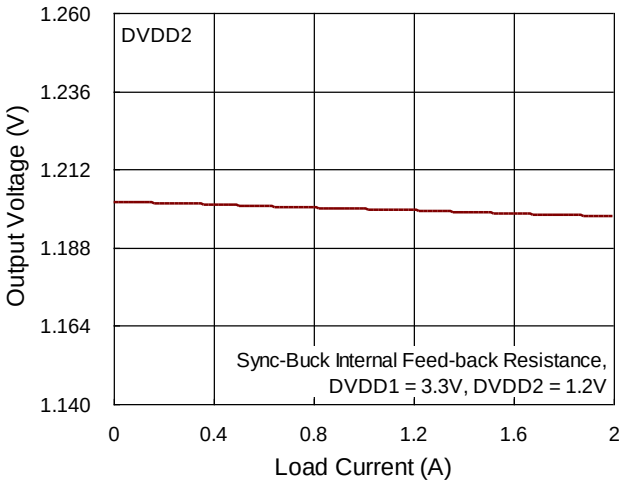
Switching Frequency vs. Input Voltage



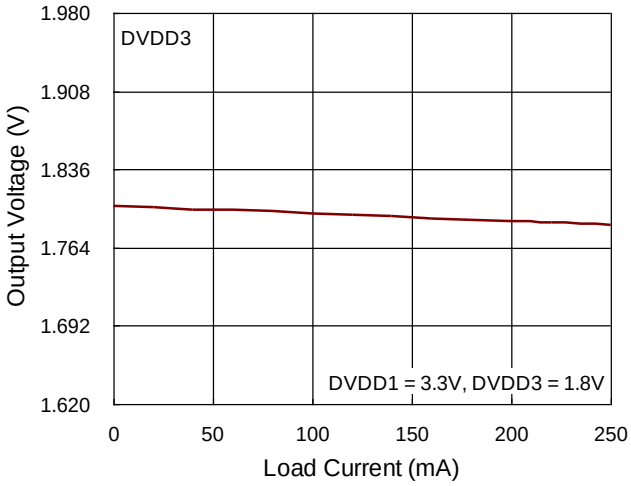
Buck Output Voltage vs. Load Current



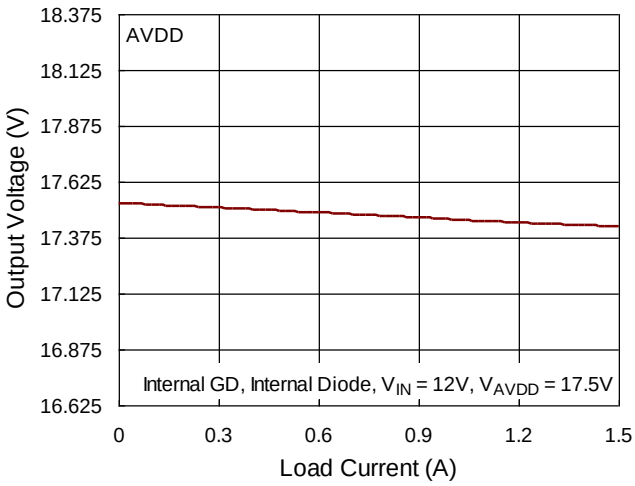
Buck Output Voltage vs. Load Current



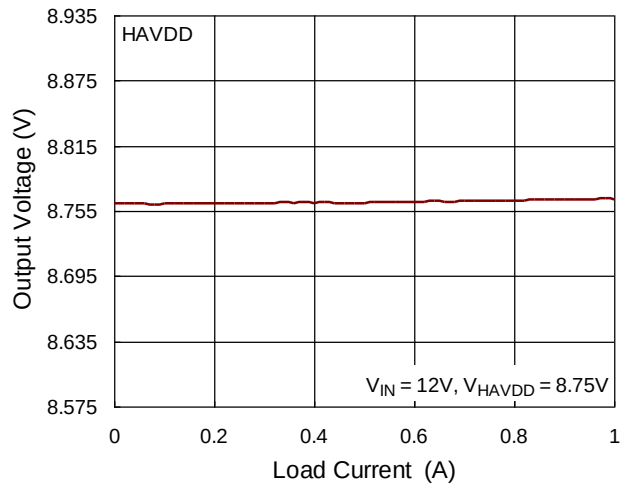
LDO Output Voltage vs. Load Current



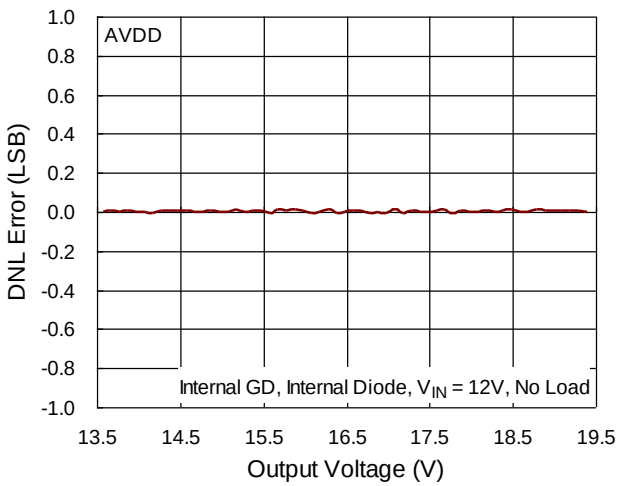
Boost Output Voltage vs. Load Current



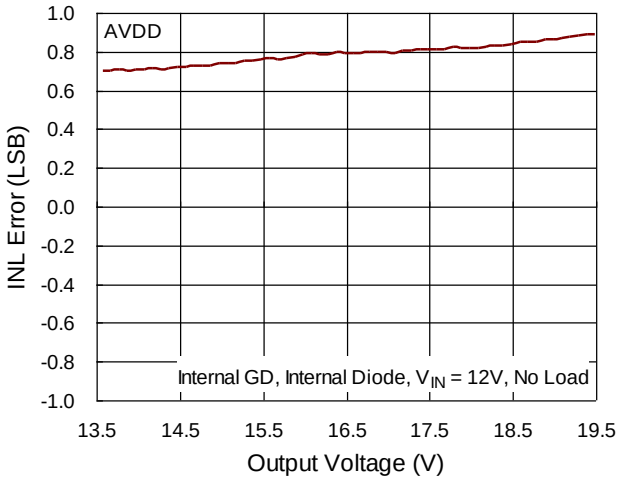
Buck Output Voltage vs. Load Current



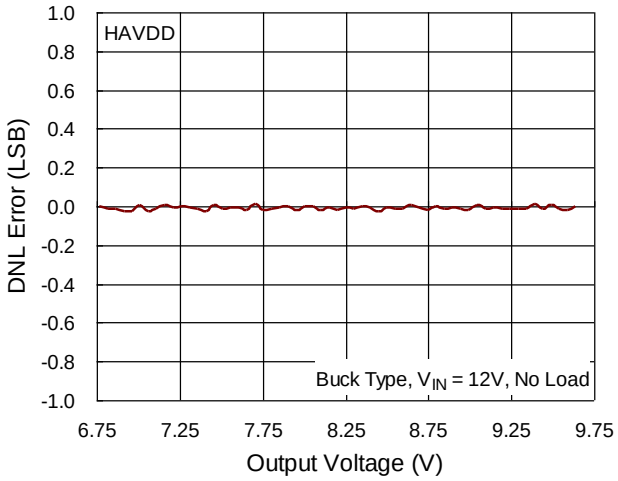
Differential Non-Linearity Error vs. Output Voltage



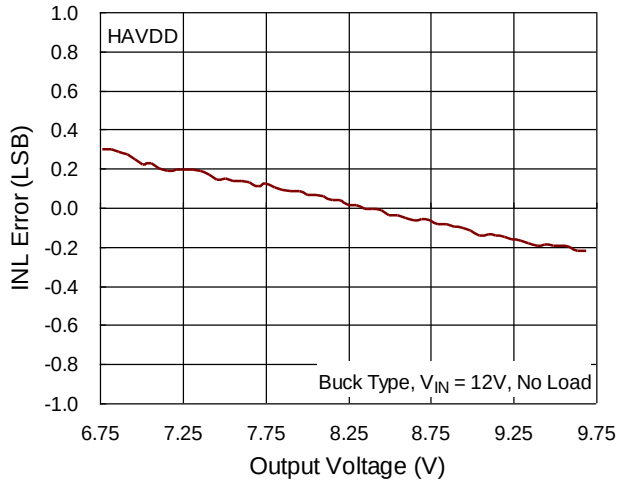
Integral Non-Linearity Error vs. Output Voltage



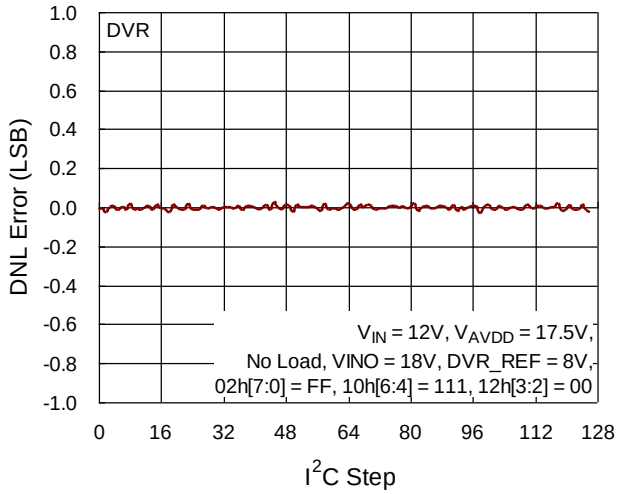
Differential Non-Linearity Error vs. Output Voltage



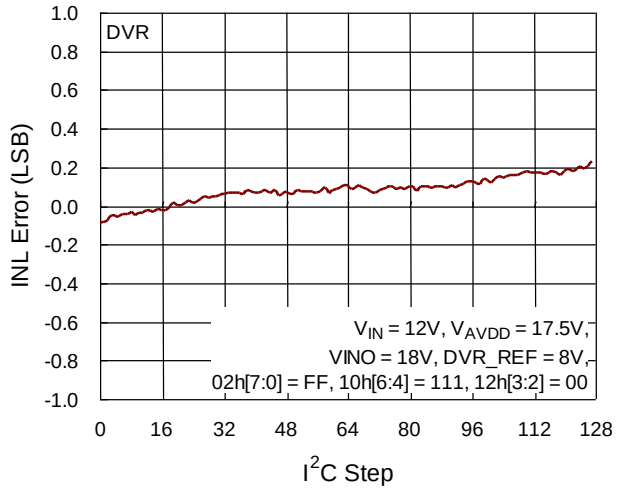
Integral Non-Linearity Error vs. Output Voltage



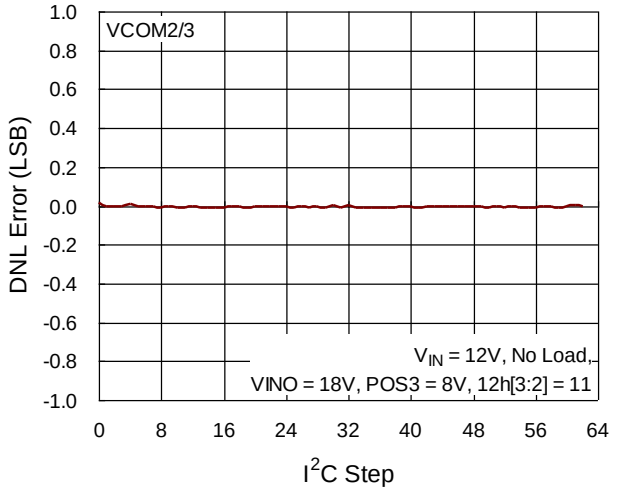
Differential Non-Linearity Error vs. I^2C Step



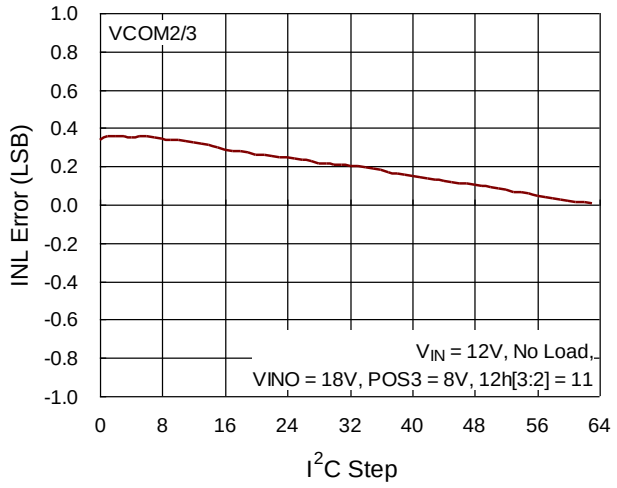
Integral Non-Linearity Error vs. I^2C Step



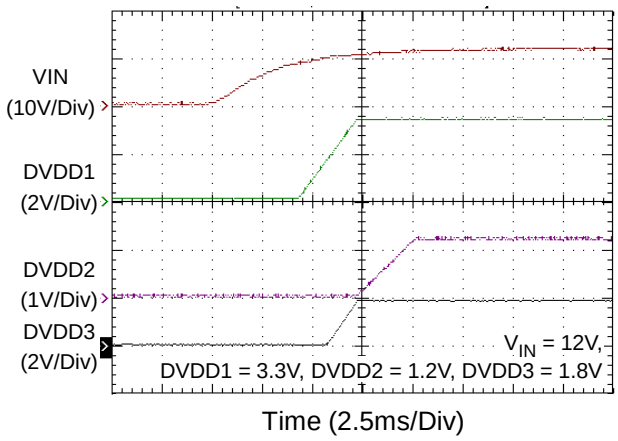
Differential Non-Linearity Error vs. I^2C Step



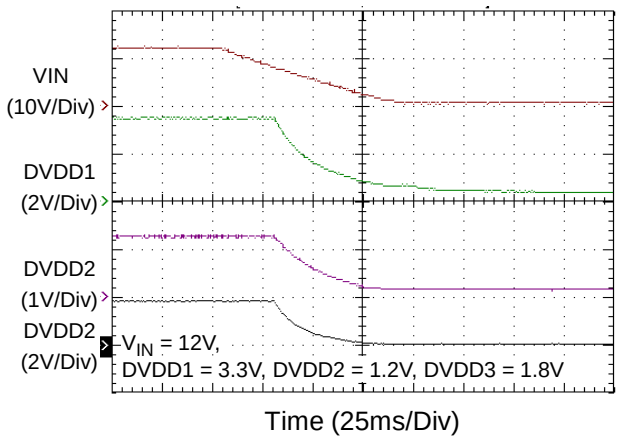
Integral Non-Linearity Error vs. I²C Step



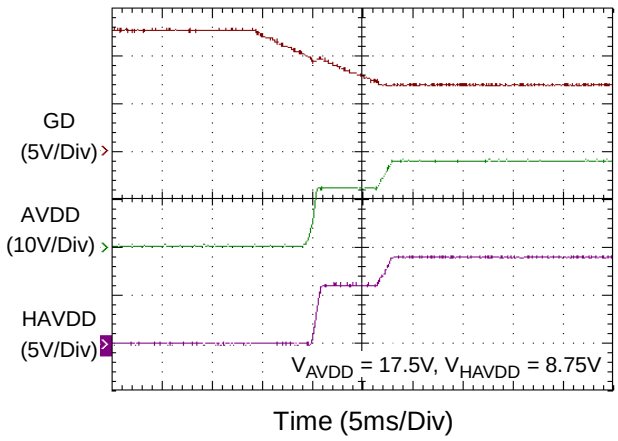
Power-On Sequence I



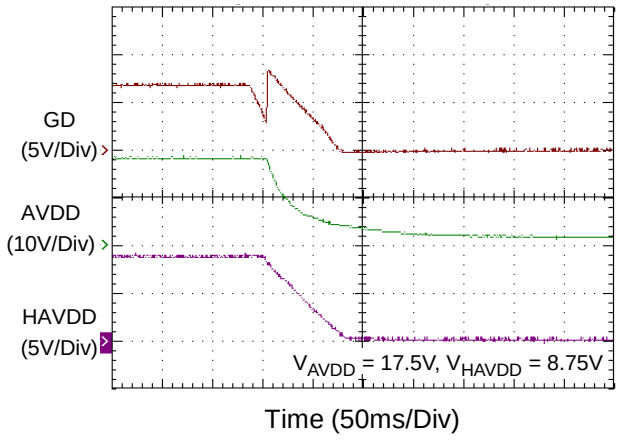
Power-Off Sequence I



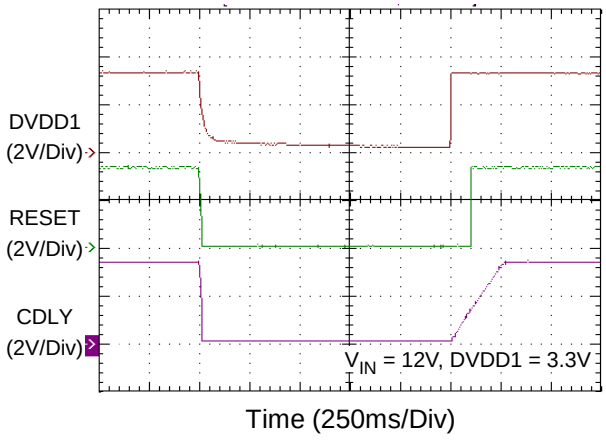
Power-On Sequence II



Power-Off Sequence II

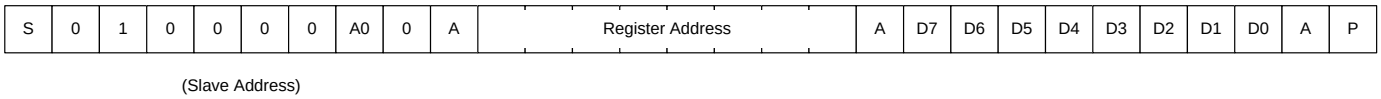


RESET Function

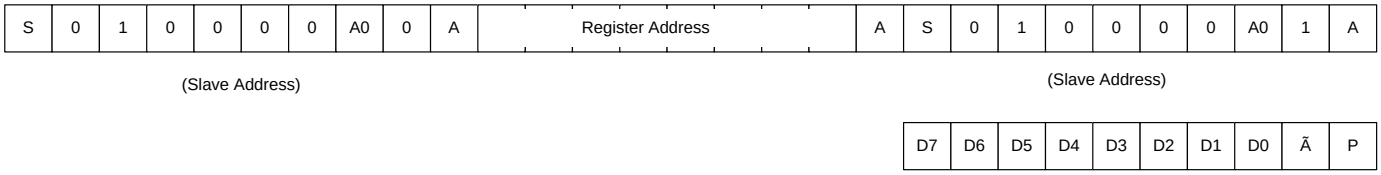


I2C Command

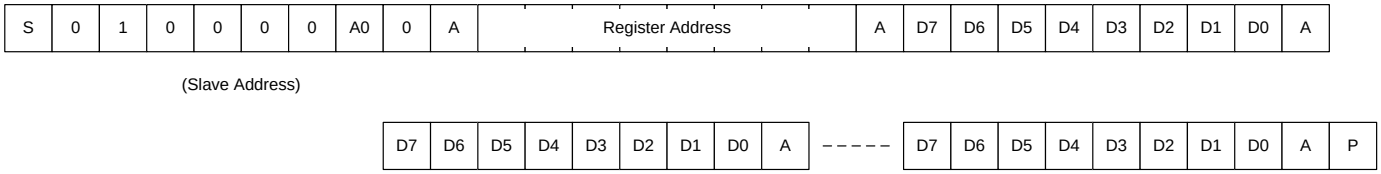
Single I2C Register Write Protocol



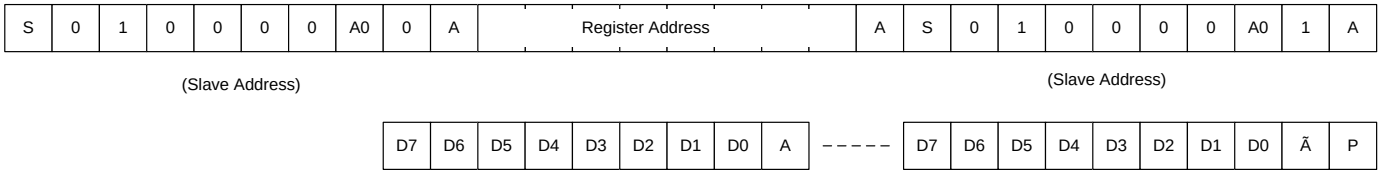
Single I2C Register Read Protocol



Multiple I2C Register Write Protocol



Multiple I2C Register Read Protocol



RT6929 I2C register data address is 0x40h(A0=0) or 0x42h(A0 = 1).

RT6929 Fault address is 0x50h(A0 = 0) or 0x52h(A0 = 1).

RT6929 DVR I2C register/EEPROM address is 0x9Eh only when A0 = 1.

RT6929 AVDD Trimming I2C register/EEPROM address is 0x4Ah(A0 = 0) or 0x6Ah(A0 = 1).

Register Map

Slave Address: 40h(A0 = 0) or 42h(A0 = 1)

Reg Add.	Bits	Register	Description	Resolution
0x00	8	(1) AVDD	A-bank Analog Voltage Setting	0.1V(13.5V～19.4V) (86h～C1h)
0x01	8	(1) HAVDD		0.05V(6.75V～9.7V) (86h～C1h)
0x02	8	(1) DVR (Max), VCOM1		DVR_REF/256 (DVR_REF/256 ~ DVR_REF)
0x03	6	(1) VCOM2 [5:0]		POS2/64 (POS2/64 ~ POS2)
0x04	6	(1) VCOM3 [5:0]		POS3/64 (POS3/64 ~ POS3)
0x05	7	(1) DVR Tuning Data [7:1]		[DVR Code
0x06	8	(1) AVDD	B-bank Analog Voltage Setting	0.1V(13.5V～19.4V) (86h～C1h)
0x07	8	(1) HAVDD		0.05V(6.75V～9.7V) (86h～C1h)
0x08	8	(1) DVR (Max), VCOM1		DVR_REF/256 (DVR_REF/256 ~ DVR_REF)
0x09	6	(1) VCOM2 [5:0]		POS2/64 (POS2/64 ~ POS2)
0x0A	6	(1) VCOM3 [5:0]		POS3/64 (POS3/64 ~ POS3)
0x0B	7	(1) DVR Tuning Data [7:1]		DVR Code
0x0C	8	(1) DVDD1 (FB Internal)	Logic Voltage Setting	0.05V (2.6V ~ 4.0V) (33h～4Fh)
0x0D	8	(1) DVDD2 (FB Internal, External)		0.02V (0.8V ~ 2.6V) (27h～81h)
0x0E	8	(1) DVDD3 (FB Internal)		0.02V (0.8V ~ 2.6V) (27h～81h)
0x0F	8	(1) Transient Time : AVDD, HAVDD [7:4]		0: disable, 1.0ms ～ 15s)
		(2) Transient Option : DVR [1], VCOM2 [2], VCOM3 [3]		[1] [2] [3] 0 : disable, 1 : Enable
		(3) HAVDD Option [0]		0 : DC/DC, 1 : OPAMP
0x10	8	(1) DVR Selectable Option [7]		0 : EEPROM, 1 : I2C
		(2) DVR Variable Range [6:4]		0.5V (0.5V ~ 4V)
		(3) AVDD Delay 1 time [3:0]		20ms (0ms ～ 300ms)
0x11	8	(1) DVDD1 Frequency Select [7:6]	EMI Tuning	00 : Initial Frequency(Default), 01 : X2, 10 : X3, 11 : x3
		(2) DVDD2 Frequency Select [5:4]		00 : Initial Frequency, 01: X2, 10 : X3(default), 11 : x3
		(3) AVDD switching slew-rate [3:2]		00 : 100%(default) 01 : 80% 10 : 65% 11 : 55%
		(4) DVDD2 switching slew-rate [1:0]		00 : 100%(default) 01 : 75% 10 : 50% 11 : 25%

0x12	8	(1) Initial Frequency [5:4]		00 : 450kHz, 01 : 600kHz, 10 : 750kHz (default), 11: 900kHz
		(2) VCOM Reference Select [3:2]		00 : POS2 Floating, 01 : POS1 = POS2, 10 : POS2 = POS3, 11 : POS1 = POS2 = POS3
		(3) Monitoring Frame setting [1:0]		00 : 8Frame, 01:32Frame, 10: 128Frame, 11 : 512 Frame
0x13	8	(1) TSD option [5]		0 : ON, 1 : OFF
		(2) AVDD OCP Select [4:2]		0.5A (1.5A ~ 5.0A)
		(3) DVDD1 OCP Select [1]		0 : 3.5A(default), 1 : 1.5A
		(4) DVDD2 OCP Select [0]		0 : 3.5A(default), 1 : 1.5A
0x14	8	(1) DVDD1 SBD Option [4]		0 : Internal(Default), 1 : External
		(2) DVDD2 SBD Option [3]		0 : Internal(Default), 1 : External
		(3) Load Switch Option [2]		0 : Internal, 1 : External
		(4) AVDD Diode Option [1]		0 : Internal, 1 External
		(5) MAIN PMIC Start-up [0]		0 : Disable, 1 : Enable

Transient Time : 0Fh [7:4]

Step	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Time	Disable	1ms	2.5ms	4ms	5.5ms	7ms	8.5ms	10ms	1s	3s	5s	7s	9s	11s	13s	15s

DVR Variable Range : 10h [6:4]

Step	0	1	2	3	4	5	6	7
△V	0.5	1	1.5	2	2.5	3	3.5	4

AVDD Delay1 Time : 10h [3:0]

Step	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Time(ms)	0	20	40	60	80	100	120	140	160	180	200	220	240	260	280	300

DVDD1 Frequency Select : 11h [7:6]

Step	0	1	2	3
Freq.(KHz)	Initial Freq.(default)	X2	X3	X3

DVDD2 Frequency Select : 11h [5:4]

Step	0	1	2	3
Freq.(KHz)	Initial Freq.	X2	X3 (default)	X3

AVDD Switching Slew-Rate : 11h [3:2]

Step	0	1	2	3
Slew-rate	100%	80%	65%	55%

DVDD2 Switching Slew-Rate : 11h [1:0]

Step	0	1	2	3
Slew-rate	100%	80%	65%	55%

Monitor Frame Setting : 12h [1:0]

Step	0	1	2	3
Frame	8	32	128	512

Initial Frequency : 12h [5:4]

Step	0	1	2	3
Freq.(KHz)	450	600	750 (default)	900

VCOM Reference Select: 12h [3:2]

Step	0	1	2	3
Number	Floating	POS1=POS2	POS2=POS3	POS1=POS2=POS3

AVDD OCP Level Setting: 13h [4:2]

SW Current	0	1	2	3	4	5	6	7
Min [A]	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0

Slave address : 50h(A0 = 0) or 52h(A0 = 1)

Reg. Add.	Bits	Register	Description	Resolution
0x00	8	(1) Die Temperature [5:2] (2) PBA Temperature [1:0]		(1) 5°C (75°C ~ 150°C) (2) 25°C (~0°C, 0~25°C, 25~50°C, 50°C ~)
0x01	8	(1) AVDD Voltage [7:4] (2) AVDD Current [3:0]		(1) 0.5V (13V ~ 20.5V) (2) 0.3A (0.3A ~ 4.8A)
0x02	8	(1) - (2) Logic EN [6] (3) Analog EN [5] (4) I2C [4] (5) Wrong Data [3] (6) Seq. IN [2] (7) DVDD1 OVP [1] (8) DVDD1 OLP [0]		(1) – (2) 0 : Normal 1 : Error (3) 0 : Normal 1 : Error (4) 0 : Normal 1 : Error (5) 0 : Normal 1 : Error (6) 0 : Normal 1 : Error (7) 0 : Normal 1 : Error (8) 0 : Normal 1 : Error
0x03	8	(1) DVDD2 OLP [7] (2) DVDD3 OLP [6] (3) AVDD OVP [5] (4) AVDD OLP [4] (5) HAVDD OVP [3] (6) HAVDD OLP [2] (7) AVDD-HAVDD [1] (8) TSD [0]		(1) 0 : Normal 1 : Error (2) 0 : Normal 1 : Error (3) 0 : Normal 1 : Error (4) 0 : Normal 1 : Error (5) 0 : Normal 1 : Error (6) 0 : Normal 1 : Error (7) 0 : Normal 1 : Error (8) 0 : Normal 1 : Error

Detail Monitoring

Code	Die Temp. (°C)	PBA Temp. (°C)	AVDD Voltage (V)	AVDD Current (A)
0000	70 ~ 75	~ 0	0.0 ~ 13.0	0.0 ~ 0.3
0001	75 ~ 80	0 ~ 25	13.0 ~ 13.5	0.3 ~ 0.6
0010	80 ~ 85	25 ~ 50	13.5 ~ 14.0	0.6 ~ 0.9
0011	85 ~ 90	50 ~	14.0 ~ 14.5	0.9 ~ 1.2
0100	90 ~ 95		14.5 ~ 15.0	1.2 ~ 1.5
0101	95 ~ 100		15.0 ~ 15.5	1.5 ~ 1.8
0110	100 ~ 105		15.5 ~ 16.0	1.8 ~ 2.1
0111	105 ~ 110		16.0 ~ 16.5	2.1 ~ 2.4
1000	110 ~ 115		16.5 ~ 17.0	2.4 ~ 2.7
1001	115 ~ 120		17.0 ~ 17.5	2.7 ~ 3.0
1010	120 ~ 125		17.5 ~ 18.0	3.0 ~ 3.3
1011	125 ~ 130		18.0 ~ 18.5	3.3 ~ 3.6
1100	130 ~ 135		18.5 ~ 19.0	3.6 ~ 3.9
1101	135 ~ 140		19.0 ~ 19.5	3.9 ~ 4.2
1110	140 ~ 145		19.5 ~ 20.0	4.2 ~ 4.5
1111	145 ~ 150		20.0 ~ 20.5	4.5 ~ 4.8

Fault Analysis

Fault Type	Fault Judgment
Logic EN (Masking “Low” during the operation)	When the EN from SET is not detected in 10 seconds(typ.) after releasing VIN UVLO
I2C Error	When the I2C enable signal is not detected in 10 seconds(typ.) after releasing VIN UVLO
Analog EN (Masking “Low” during the operation)	When the TRDY signal from T-con is not detected in 10 seconds(typ.) after completion of I2C communication.
SEQ_IN (Masking “Low” during the operation)	When the SEQ_IN signal from RT6930 is not detected in 10 seconds(typ.) after input of Analog EN signal.
Wrong DATA	When any register data is out of range
OVP	When any output voltage is over the OVP detect level 10 times (When STV signal starts , the OVP function resets the OVP level count)
HAVDD OVP (OP-AMP)	When the HAVDD voltage is over the OVP detect level for 20us (When STV signal starts , the OVP function resets the OVP level count)
OLP	When the IC is latched in shut-down condition due to the SCP
TSD	When the IC falls to TSD condition irrespective of TSD on/off option.
AVDD-HAVDD	When the difference of AVDD and HAVDD becomes higher than 10.5V during the transient period 10 times (When STV signal starts, the subtract function resets the count)

Application Information

The RT6929 is a multi-functional power solution for LCD panel. The RT6929 contains a Boost converter for main power, three synchronous Buck converters and LDO regulator to provide the logic voltage and the source driver for the system, and three VCOM drivers. The AVDD Boost and HAVDD Buck are operation switching frequency of 900kHz / 750kHz / 600kHz / 450kHz which can be controlled by setting I2C Register 12h[5:4]. The DVDD1 Buck converter and DVDD2 Buck converter are operation switching frequency of 2.7MHz / 2.25MHz / 1.8MHz / 1.5MHz / 1.35MHz / 1.2MHz / 900KHz / 750KHz / 600KHz / 450KHz which can be controlled by setting I2C Register 11h[7:6] and Register 11h[5:4].

Under Voltage Lockout

To prevent abnormal operation of the IC in low voltage condition, an under voltage lockout is included which shut down the device at voltages lower than 8.15V (Typ.). All functions will be turned off in this state.

Over-Temperature-Protection

The RT6929 equips an Over Temperature Protection (OTP) to prevent the excessive power dissipation from overheating. The OTP will shut down switching operation while junction temperature exceeds 160°C. Main converter starts switching while junction temperature is cooled by approximately 30°C. Prevent the maximum junction temperature over around 160°C to maintain the continuous operation.

AVDD Boost Converter

The Boost converter is high efficiency PWM architecture. It performs fast transient responses to generate source driver supplies for TFT LCD display. The high operation frequency allows use of smaller components to minimize the thickness of the LCD panel. The output voltage can be achieved by setting the I2C data.

Boost Soft-Start

The main boost converter has an internal soft-start to prevent high inrush current during start-up. The device incorporates a digital soft-start increasing the current limit in digital current limit steps. AVDD soft-start time is 5ms (Typical).

Gate Drive Pin (GD) and Isolation Switch Selection

The external isolation switch disconnects the boost converter once the device is turned off. If the boost converter is enabled and the delay time DLY1 by I2C setting pass by, the gate pin GD is pulled low by an internal 10μA current sink to minimize inrush current until the Gate-Source voltage is clamped at about VLSIN -6 V. An internal 10kΩ pull up resistor to VIN is connected to GD to open the isolation switch if the Gate Drive is disabled. Using a gate drain capacitor of typically 22nF allows to increase the turn on time of the MOSFET for further inrush current minimization. If the boost sense voltage falls below VAVDD x 0.85 for more than 3ms, GD is pulled high and the boost converter shut down. The device does not recover automatically from shut down but under-voltage lockout must be toggled. Using this configuration allows to optimize the solution to specific application requirement and different MOSFETs can be used. A standard P-Channel MOSFET with a current rating close to the maximal used switch current of the boost converter is sufficient.

Boost Output Voltage Setting

The output voltage can be achieved by setting the I2C Register 00h (Bank1) / 06h(Bank2). The AVDD setting is from 13.5V to 19.4V when Register 00h data from 86h to C1h. Refer to Register Map and Output Code Table. The AVDD output voltage can be disabled by setting I2C Register 00h / 06h data 00h. If AVDD setting is over C1h or under 86h, IC will shut down.

Boost Inductor Selection

The inductor value depends on the maximum input current. As a general rule the inductor ripple current is 20% to 40% of maximum input current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equation :

$$I_{IN(MAX)}=\frac{V_{OUT}\times I_{OUT(MAX)}}{\eta\times V_{IN}}$$

$$I_{RIPPLE}=0.4\times I_{IN(MAX)}$$

where η is the efficiency of the Boost converter, $I_{IN(MAX)}$ is the maximum input current and I_{RIPPLE} is the inductor ripple current. The input peak current can be obtained by adding the maximum input current with half of the inductor ripple current as shown in the following equation :

$$L=\frac{\eta\times(V_{IN})^2\times(V_{OUT}-V_{IN})}{0.4\times(V_{OUT})^2\times I_{OUT(MAX)}\times f_{OSC}}$$

where f_{OSC} is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

Boost Diode Selection

Schottky diode is a good choice for an asynchronous Boost converter due to its small forward voltage. However, when selecting Schottky diodes, important parameters such as power dissipation, reverse voltage rating and pulsating peak current should all be taken into consideration. For better performance, it is recommended to choose a suitable diode with reverse voltage rating greater than the maximum output voltage and its average current rating must exceed the average output current.

Boost Input Capacitor Selection

Low ESR ceramic capacitors are recommended for input capacitor applications. Low ESR will effectively reduce the input ripple voltage caused by the switching operation. 10μF x 2 low ESR ceramic capacitors are sufficient for most applications. Nevertheless, this value can be decreased for applications with lower output current requirement. Another consideration is the voltage rating of the input capacitor, which must be greater than the maximum input voltage.

Boost Output Capacitor Selection

Output ripple voltage is an important index for estimating the performance. This portion consists of two parts, one is the product of IIN and ESR of output capacitor, another part is formed by charging and discharging process of output capacitor. As shown in Figure 22, $\triangle V_{OUT1}$ can be evaluated based on the ideal energy equalization. According to the definition of Q, the Q value can be calculated as the following equation :

$$Q=\frac{1}{2}\times\left[\left(I_{IN}+\frac{1}{2}\Delta I_L-I_{OUT}\right)+\left(I_{IN}-\frac{1}{2}\Delta I_L-I_{OUT}\right)\right]\times\frac{V_{IN}}{V_{OUT}}\times\frac{1}{f_{OSC}}$$

$$=C_{OUT}$$

where f_{OSC} is the switching frequency and the $\triangle I_L$ is the inductor ripple current. Move C_{OUT} to the left side to estimate the value of $\triangle V_{OUT1}$ as the following equation :

$$\Delta V_{OUT1}=\frac{D\times I_{OUT}}{\eta\times C_{OUT}\times f_{OSC}}$$

Finally, the output ripple voltage can be determined as the following equation :

$$\Delta V_{OUT}=I_{IN}\times ESR+\frac{D\times I_{OUT}}{\eta\times C_{OUT}\times f_{OSC}}$$

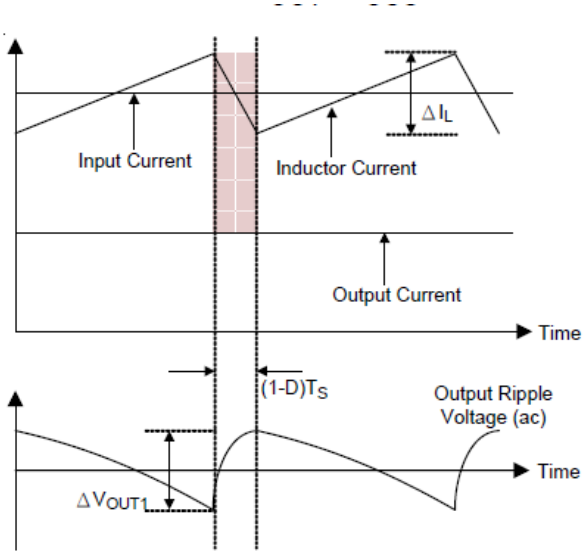


Figure 22. The Output Ripple Voltage without the Contribution of ESR

Boost Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisting of R6 and C19. Choose R6 to set high frequency integrator gain for fast transient response and C19 to set the integrator zero to maintain stability.

Boost Over-Voltage Protection

The main Boost converter has an over voltage protection to protect the main switch pin (LX) in case the COMP pin is shorted to abnormal voltage. In such an event, the output voltage rises and is monitored with the over voltage protection comparator at the AVDD pin. In case AVDD pin is above 21V (typ.), the converter turns the N-MOSFET switch off. As soon as the output voltage falls below the over voltage threshold, the converter resumes operation.

Boost Over-Current Protection

The RT6929 can limit the peak inductor current to achieve over current protection. The IC senses the inductor current of on period that is flowing into LX pin. The minimize value of the current limit is 5A. The internal N-MOSFET will be turned off if the peak inductor current reaches 5A. So that, the output current at current limit boundary is denoted as $I_{OUT(CL)}$ and can be calculated as the following equation :

$$I_{OUT(CL)}=\eta\times\frac{V_{IN}}{V_{OUT}}\times\left(I_{CL}-\frac{1}{2}\times\frac{V_{IN}\times(V_{OUT}-V_{IN})}{V_{OUT}}\times\frac{t_S}{L}\right)$$

Where η is the efficiency of the Boost converter, $I_{OUT(CL)}$ is the value of the current limit and TS is the switching period. The minimize value of current limit can be achieved from 0.5A to 5A by setting the I2C Register 13h [4:2].

Boost Fault Protection

The Boost function has a fault protection feature to protect the IC when the output becomes shorted to GND. This is achieved by using the comparator to monitor the AVDD voltage. If AVDD remains below AVDD x 0.85 for 3ms, the boost converter will be disabled. Once shut down, the Boost converter can only be enabled until the chip is power on again.

Buck Converter

The synchronous Buck converter is high efficiency PWM architecture with fast transient response. The converter drives an internal N-MOSFET which is connected among the VINB pin and LXB1, PDVDD1 pin and LXB2 respectively.

Buck Soft-Start

The two step-down converters have an internal soft-start to reduce the input inrush current. When the Buck converter is enabled, the reference voltage rises slowly from zero to 3.3V and 1.2V respectively. The typical soft-start time is around 3ms.

Buck Output Voltage Setting

The output voltage of DVDD1 can be achieved by setting I2C data.

Due to FB detect function, the output voltage of DVDD2 can be achieved by not only setting I2C data, but also setting as following equation :

$$V_{DVDD2}=V_{FBB2}\times\left(1+\frac{R_{23}}{R_{24}}\right)$$

Where V_{FBB2} are the reference voltage and the typical value is 0.6V. The V_{DVDD1} and V_{DVDD2} must be below $V_{DVDD1} = V_{IN} \times D_{MAX}$ and $V_{DVDD2} = V_{PDVDD1} \times D_{MAX}$

Buck Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L will increase with higher V_{IN} and decrease with higher inductance, as shown in below equation :

$$\Delta I_L = \left(\frac{V_{OUT}}{f \times L}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal. For the ripple current selection, the value of $I_{L(MAX)} = 0.4$ is a reasonable starting point. The largest ripple current occurs at the highest VIN. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left(\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN(NAX)}}\right)$$

Buck Input Capacitor Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, a 22μF low ESR ceramic capacitor is recommended.

Buck Output Capacitor Selection

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, V_{OUT}, is determined by :

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR + \frac{1}{8 \times f \times C_{OUT}}\right)$$

The output ripple will be highest at the maximum input voltage since I_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Suitable candidates such as dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications requiring high ripple current rating and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. Nevertheless, higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator

applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input, VIN, and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input. At best, this ringing can be coupled to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at VIN large enough to damage the part.

Buck Over-Current Protection

The RT6929 can limit the peak current to achieve over current protection. The IC senses the inductor current of on period that is flowing out of the LXB1 and LXB2 pin. The internal N-MOSFET will be turned off if the peak inductor current reaches 5A/2.2A (typ.). The DVDD1 and DVDD2 minimum value of current limit can be achieved from 3.5A/1.5A by setting the I2C Register 13h [1] and 13h [0], respectively.

Buck Fault Protection

To avoid the output is shorted to GND and the switching frequency is reduced from normal operating frequency, the converter uses the comparator to monitor the DVDD1 or FBB2 voltage. The Buck converter switching frequency reduces to 1/2 of the original switching frequency when the DVDD1 or FBB2 is below DVDD1*0.85 or FBB2 *0.85 . The fault function can disable the Buck converter if DVDD1 or FBB2 falls below DVDD1*0.85 or FBB2 *0.85 and keeps 3ms. The Buck converter will turn on until power on again.

HAVDD Buck Output Voltage Setting

The output voltage can be achieved by setting the I2C Register 01h (BANK1)/Register 07h (BANK2). The HAVDD setting is from 6.75V to 9.7V when Register 01h/07h data from 86h to C1h. Refer to Register Map and Output Code Table. The output voltage can be disabled by I2C Register 01h/07h data setting 00h. If HAVDD setting is over C1h or under 86h or (AVDD-HAVDD) >10.5V, IC will shut down.

HAVDD Buck Over-Current Protection

The RT6929 can limit the peak current to achieve over current protection. The IC senses the inductor current that is flowing out or flowing in of the LXH pin. The internal P-MOSFET or N-MOSFET will be turned off if the peak inductor current reaches 1.2A (min.).

HAVDD Buck Short Circuit and Over Voltage Protection and Fault Protection

To avoid the output is shorted to GND and the switching frequency is reduced from normal operating frequency, the converter uses the comparator to monitor the HAVDD voltage. The Buck converter switching frequency reduces to 1/2 of the original switching frequency when the HAVDD is below HAVDD x 0.85V. The fault function can disable the synchronous Buck converter if HAVDD falls below HAVDD x 0.85 or above 10.5V and keeps 3ms. The synchronous Buck converter will turn on until power on again.

HAVDD Operational Amplifier

The RT6929 has OP_HAVDD operational amplifier where the output voltage acts as VOP_HAVDD for the LCD panel. The OP_HAVDD can be achieved by setting the I2C Register 0Fh [0] = 1 and the typical values of short circuit current is 250mA.

LDO Regulator

The low-dropout linear regulator (LDO) can supply up to 600mA current with an input voltage of 1.8V. It uses an internal P-MOSFET as the pass device. It is suitable as the supply voltage for the T-CON ASIC. The output voltage of DVDD3 can be achieved by setting I2C data.

Digital VCOM1

The RT6929 provides the ability to reduce the flicker of an LCD Panel by adjusting the VCOM1 voltage during production test and alignment. A 128-step resolution is provided under digital control. The DVR setting is composed of two max voltage and one variable range voltage as shown in Table 4.

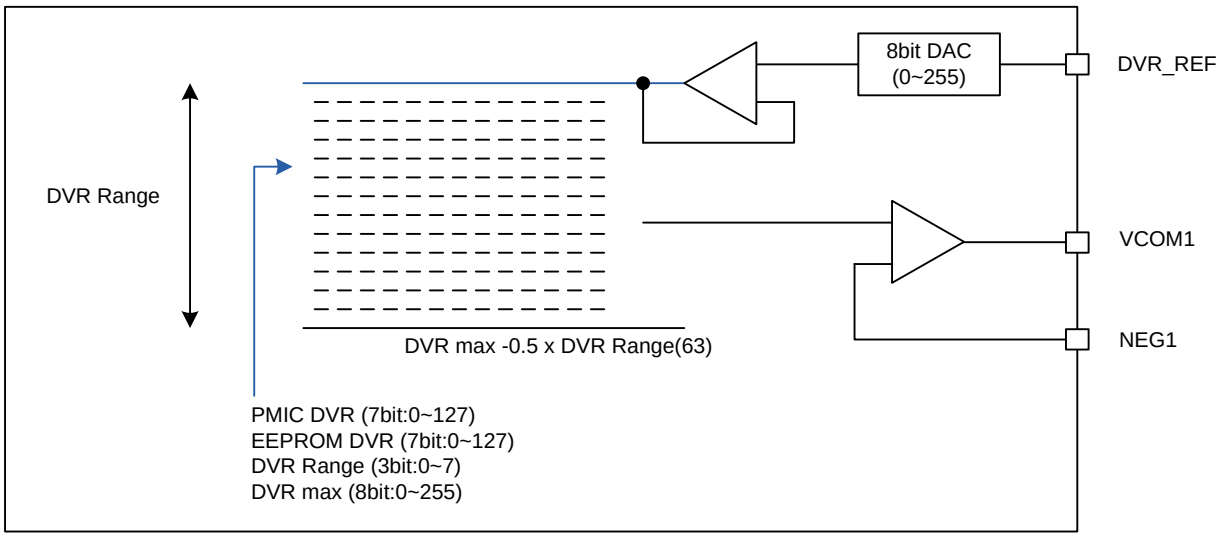


Figure 23. DVR Function Block

Table 4. DVR Setting Function

	items	bits	Resolution
SET	Max Voltage (2D)	8bit	[DVR_REF/256 ~DVR_REF]
	Max Voltage (3D)	3bit	[DVR_REF/256 ~DVR_REF]
	Variable Range Voltage (ΔV)	3bit	0.5V (0.5V~4V)
Data	EEPROM DVR (2D)	7bit	ΔV/128 (ΔV/128 ~ ΔV)
	EEPROM DVR (3D)	7bit	ΔV/128 (ΔV/128 ~ ΔV)
	PMIC DVR (2D)	7bit	ΔV/128 (ΔV/128 ~ ΔV)
	PMIC DVR (3D)	7bit	ΔV/128 (ΔV/128 ~ ΔV)

The VCOM1 voltage setting can be calculated according to the following equation :

BANK_SEL = 0 : BANK 1 Data Writing & Reading (Line DVR Tuning).

$$VCOM1\,Code\ (BANK1) = \left[\frac{DVR\_max\ Code(bank1)+1}{256}\right]\times DVR\_REF - \left[\frac{DVR\_tuning\ Code(bank1)+1}{128}\right]\times DVR\_Range(bank1)$$

BANK_SEL = 1 : BANK 2 Data Writing & Reading (Line DVR Tuning).

$$VCOM1\,Code\ (BANK2) = \left[\frac{DVR\_max\ Code(bank2)+1}{256}\right]\times DVR\_REF - \left[\frac{DVR\_tuning\ Code(bank2)+1}{128}\right]\otimes DVR\_Range(bank2)$$

AVDD Detail Trimming Function

AVDD detail trimming function is detail trimming about AVDD level of BANK1/BANK2. AVDD setting value should be detail trimming 0.1% as show in Table 5. When LSB = 0, data writes to Memory and Register. But LSB = 1, data is only write to Register. A 128-step resolution is provided under digital control and AVDD trimming slave address is 0100101xb when A0 = 0(0110101xb when A0 = 1).

Table5. AVDD Output by Code Setting.

Code Setting	AVDD
127	+6.3%
126	+6.2%
125	+6.1%
. . .	. . .
66	+0.2%
65	+0.1%
64 (default)	AVDD Setting
63	-0.1%
62	-0.2%
. . .	. . .
2	-6.2%
1	-6.3%
0	-6.4%

Analog Switch

The RT6929 has a high speed dual analog switch for SDA and SCL. The device is organized as a dual switch with independent CMOS compatible switch control (EN_ASW/WPN). When EN_ASW/WPN is high, the switch is turn on and SDA_OUT (SCL_OUT) is connected to SDA_IN (SCL_IN). And Allow I2C data writes to internal AVDD Trimming & DVR Register and EEPROM. When EN_ASW/WPN is low, the switch is turn off and a high impedance state exists between the input and output. And prevent I2C data writes to internal AVDD Trimming & DVR Register and EEPROM. The analog switch must have very short propagation delay, typically <5ns (50% to 50%) as show in Figure 24 and Figure 25. The Test circuit is as show in Figure 26.

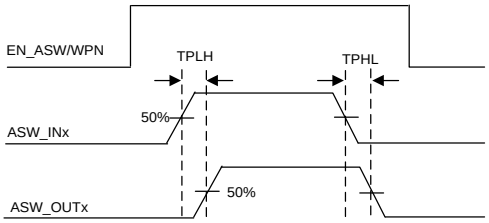


Figure 24. Analog Switch Propagation Delay

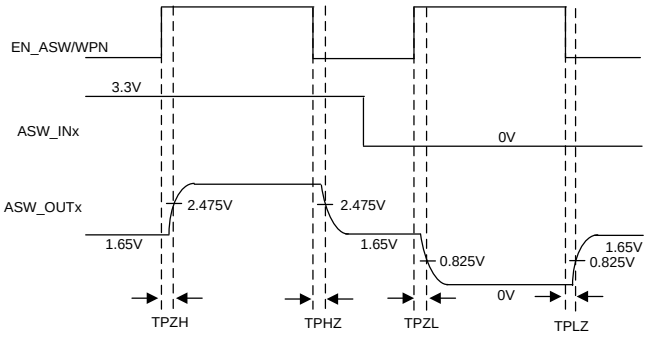


Figure 25. Analog Switch Output Enable/Disable time

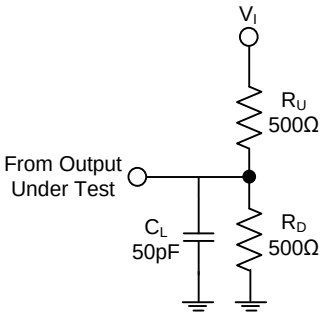


Figure 26. Analog Switch Test Circuit

RESET Function

When VCC falls below a set threshold level (V_{RESET}), the RESET output goes low, signaling the T-CON to terminate digital operation. When VCC recovers, the RESET signal goes high after a delay time. The amount of delay is determined by the external capacitance on the CDLY pin. The function block and waveforms as show in Figure 27 and Figure 28.

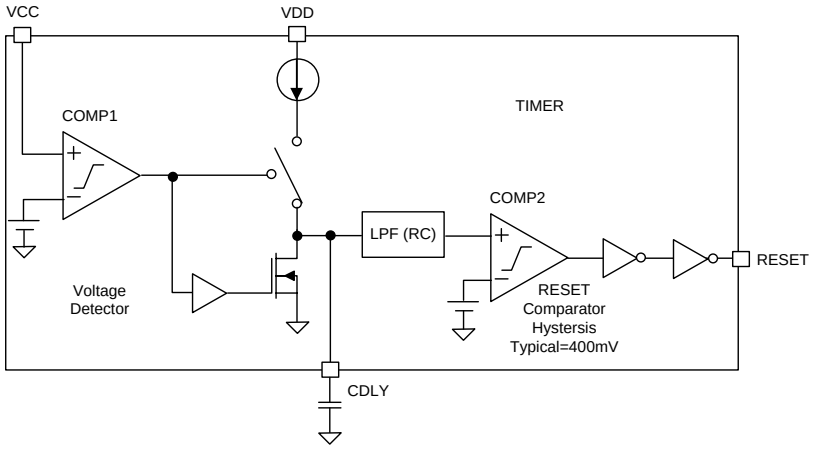


Figure 27. RESET Function Block

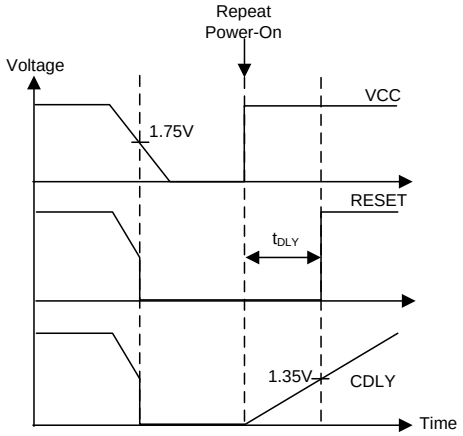


Figure 28. RESET Function Waveforms

t_{DLY} Defined :

t_{DLY} (ms) = C_{DLY} *(1.35V/5μA)

CDLY Voltage Threshold (Falling) = 1.75V(typ) ±10%

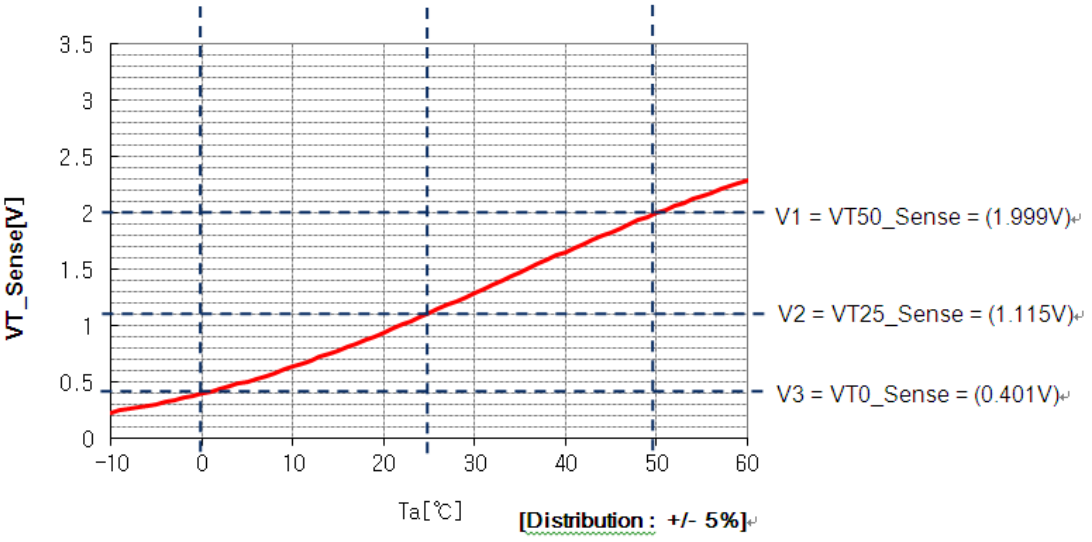
(Hysteresis = 300mV (typ) ±33%)

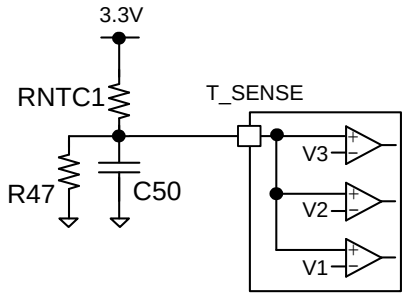
CDLY Voltage DLY Threshold (Rising) = 1.35V(typ) ± 10% (Reset comparator Hysteresis = 400mV(typ) ± 25%)

CDLY Current = 5μA(typ) ±15%

Temperature Detect Function

The RT6929 detects the voltage of NTC and update its data at register for PBA temperature monitoring function.





Data	00	01	10	11
Range	Under 0°C	0~25 °C	25~50 °C	Over 50 °C

IC Fault Function

During normal operating, each Fault Pin becomes High-state. If the one chip becomes the fault-state, the fault pin becomes low-state. Thus, the fault pin of the other chip becomes also low-state and shut-down. If the RT6929 becomes the fault-state, the RT6930 becomes shut down. If the RT6930 becomes the fault-state, the RT6929 becomes shut down except for logic power. If the resister R removes, the fault pin of the other chip becomes high-state and normal operation. As show in Figure 29.

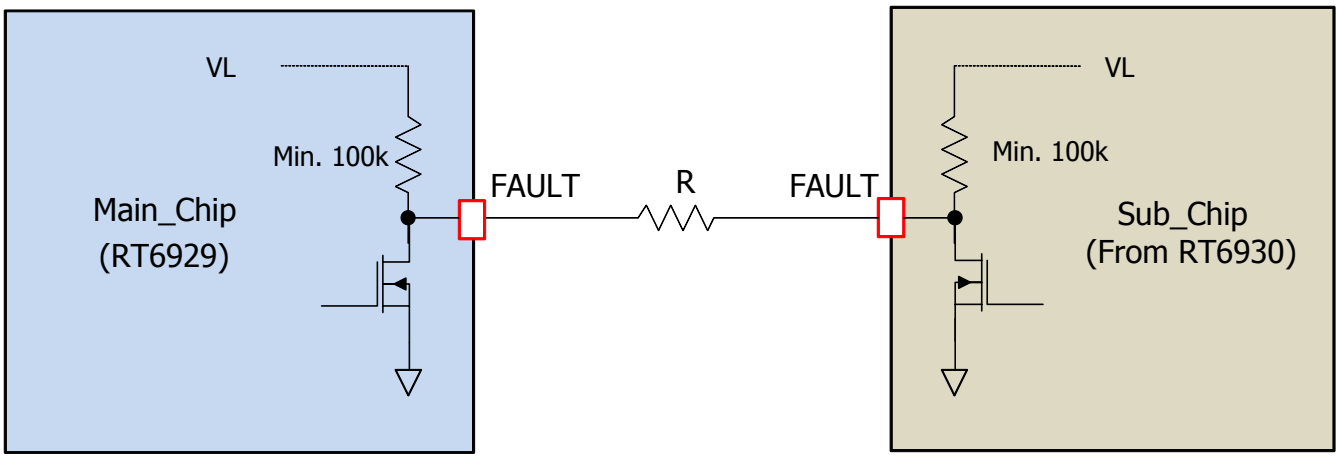


Figure 29. Fault Function Block

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-48L 6x6 package, the thermal resistance, θ_{JA}, is 26.8°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (26.8°C/W) = 3.73W for WQFN-48L 6x6 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 30 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

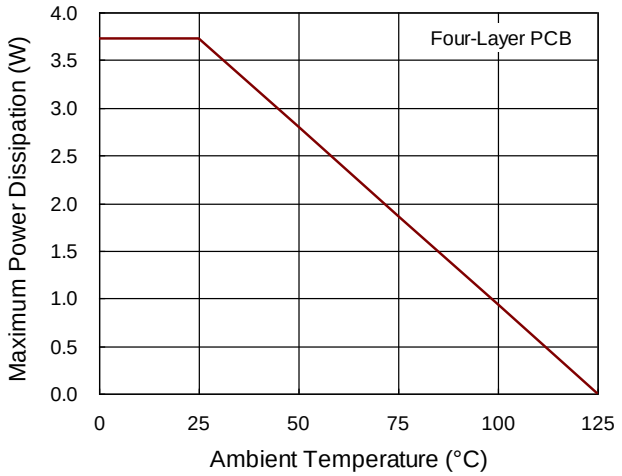


Figure 30. Derating Curve of Maximum Power Dissipation

Layout Consideration

PCB layout is very important for designing power switching converter circuits. For best performance of the RT6929, the following layout guidelines must be followed:

- For good regulation, place the power components as close as possible. The traces should be wider and shorter especially for the high current output loop.
- The feedback voltage divider resistors and output sense voltage pin must be near the feedback pin. The divider's center trace and output sense voltage pin must be short and avoid the trace near any switching nodes.
- The compensation circuit should be kept away from the power loops and be shielded with a ground trace to prevent any noise coupling.
- The sense voltage must be near the sense pin. The sense voltage pin trace must be short and avoid the trace near any switching nodes.
- Minimize the size of the LXB1, LXB2, LX and LXH node and keep it wide and shorter. Keep the LXB1, LXB2, LX and LXH node away from the feedback pin and analog ground.
- The power ground (PGND) consists of input and output capacitor grounds.
- Separate power ground (PGND) and analog ground (AGND). Connect the AGND and the PGND islands at a single end. Make sure that there are no other connections between these separate ground planes. Connect the exposed pad to a strong ground plane for maximum thermal dissipation.

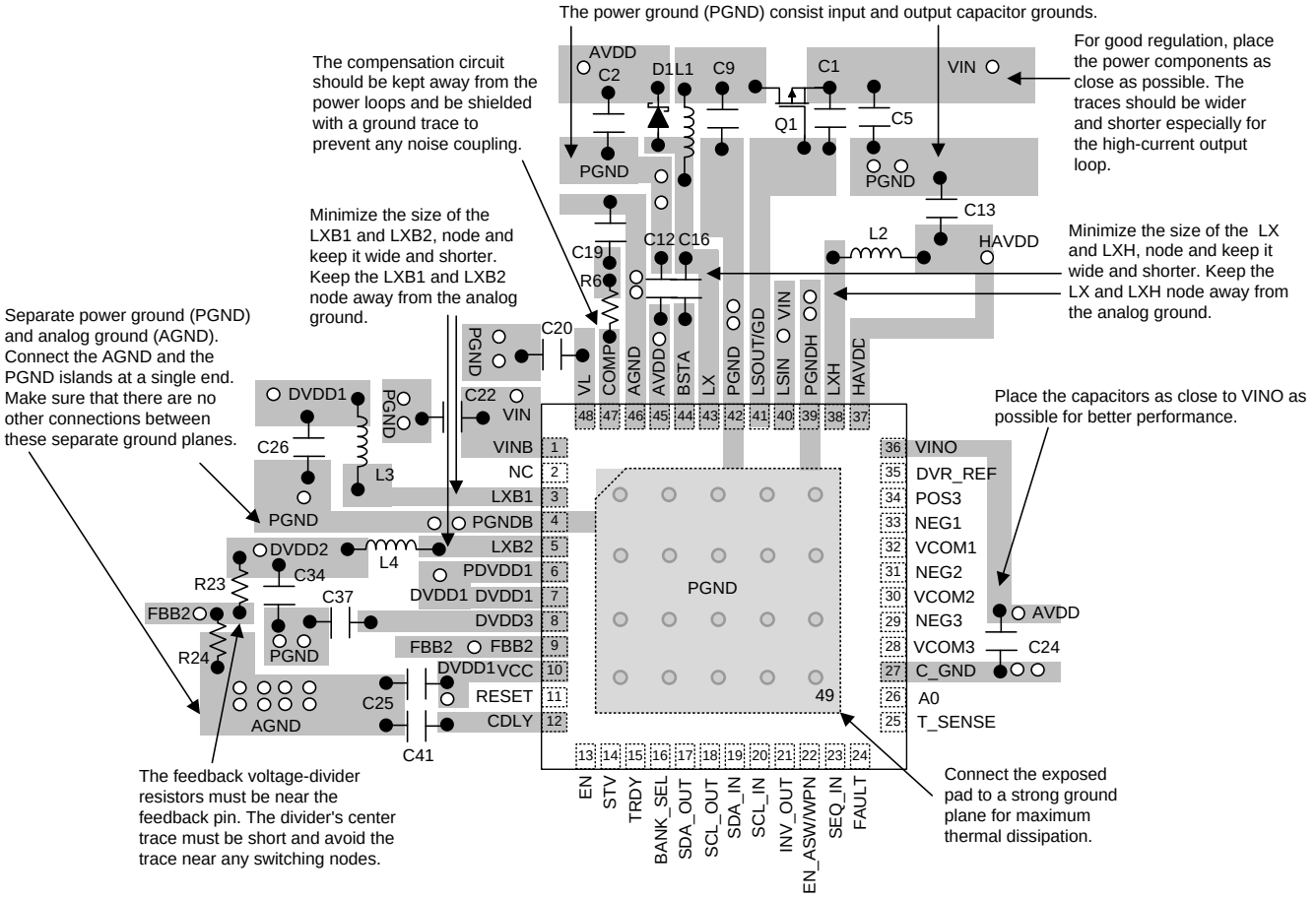
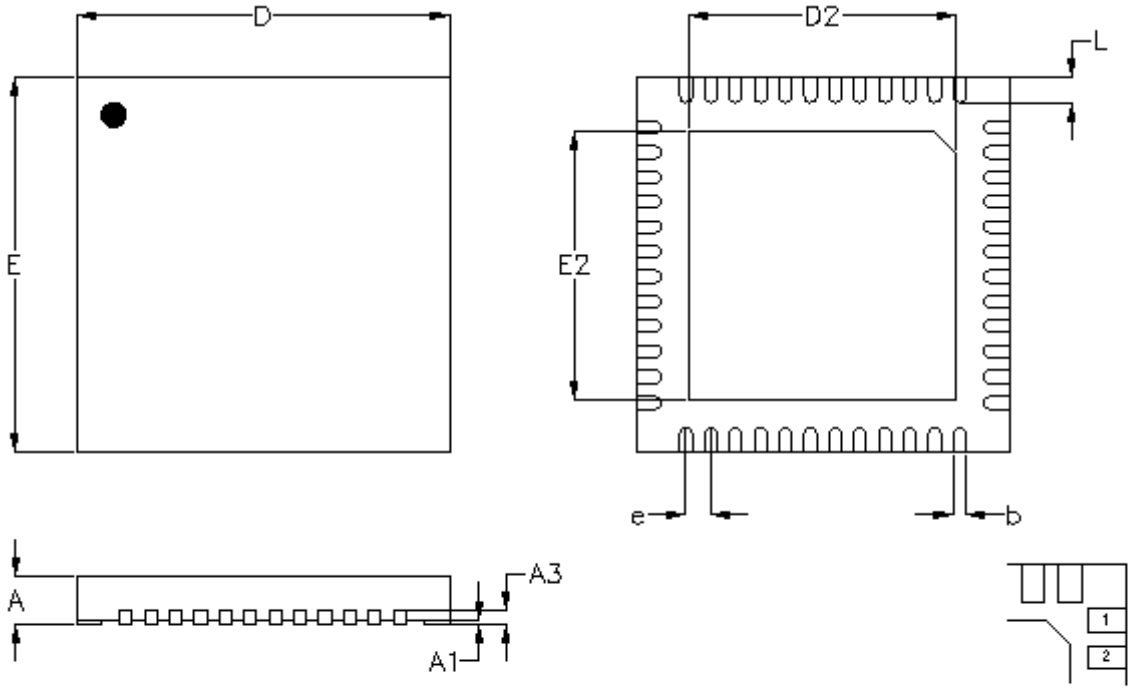


Figure 31. PCB Layout Guide

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min.	Max.	Min.	Max.
A		0.700	0.800	0.028	0.031
A1		0.000	0.050	0.000	0.002
A3		0.175	0.250	0.007	0.010
b		0.150	0.250	0.006	0.010
D		5.950	6.050	0.234	0.238
D2	Option 1	4.250	4.350	0.167	0.171
	Option 2	4.350	4.450	0.171	0.175
E		5.950	6.050	0.234	0.238
E2	Option 1	4.250	4.350	0.167	0.171
	Option 2	4.350	4.450	0.171	0.175
e		0.400		0.016	
L		0.350	0.450	0.014	0.018

W-Type 48L QFN 6x6 Package

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789