PMIC for TFT-LCD TV Panels

General Description

The RT6936 offers a compact power supply solution to provide all voltages required by a TFT-LCD panel. With its high current capabilities, the device is ideal for large screen monitor panels and LCD TV applications with 12V supply voltage. The RT6936 is available in the WQFN-40L 6x6 package.

Ordering Information

RT6936□□

- Package Type
  QW : WQFN-40L 6x6 (W-Type)
  (Exposed Pad-Option 1)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

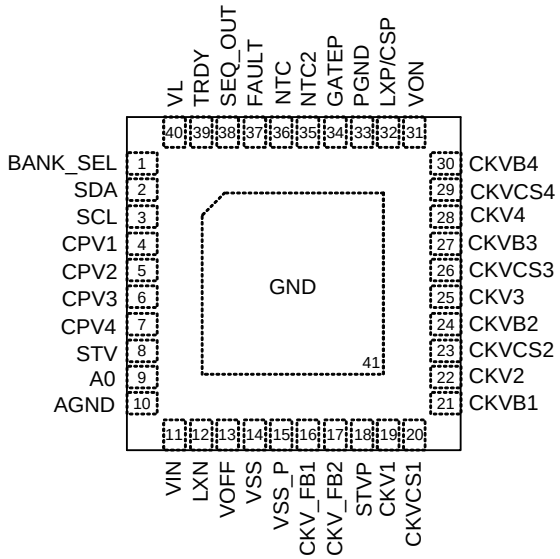
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)



WQFN-40L 6x6

Features

- **9.5V to 14.7V Input Supply Voltage**
- **0.5A to 2.25A Boost Converter for VON with 15V to 45V Programmable Output and OCP**
- **2A Inverting Buck-Boost Converter for VOFF with –5V to –27V Programmable Output**
- **0.1A Negative OP for VSS Regulator with –4V to –25V Programmable Output**
- **Switching Frequency Selectable for VON and VOFF**
- **VON/VOFF/VSS have Temperature Compensation Function**
- **VOFF ΔV Function**
- **Fault Analysis and Monitor Function**
- **4-CH Scan Driver**
- **ASG Error Detect Function**
- **4-Bit Programmable ASG Error with EEPROM**
- **Programmable Sequencing**
- **Over-Temperature Protection**
- **I²C-Compatible Interface for Register Control**
- **Thin 40-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

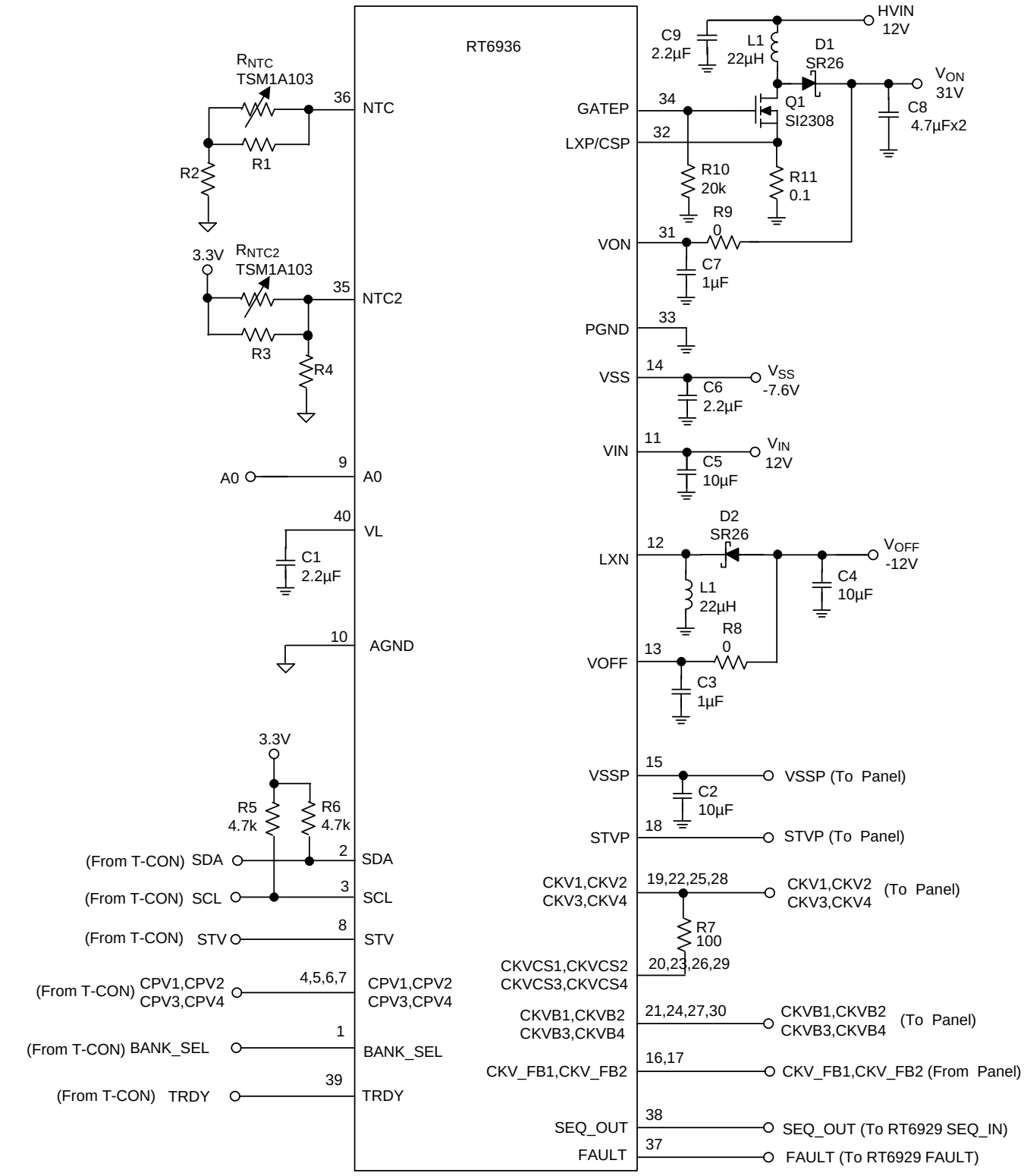
- TFT-LCD TV Panel

Marking Information

RT6936GQW : Product Number

YMDNN : Date Code

Typical Application Circuit



VON Boost Application Circuits

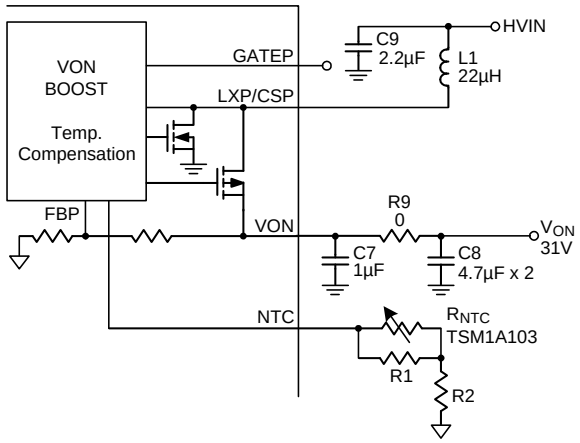


Figure 1. VON Control I : Sync-Boost

Register Address = 11h, Data = 00xxxxx1 or 01xxxxx1.

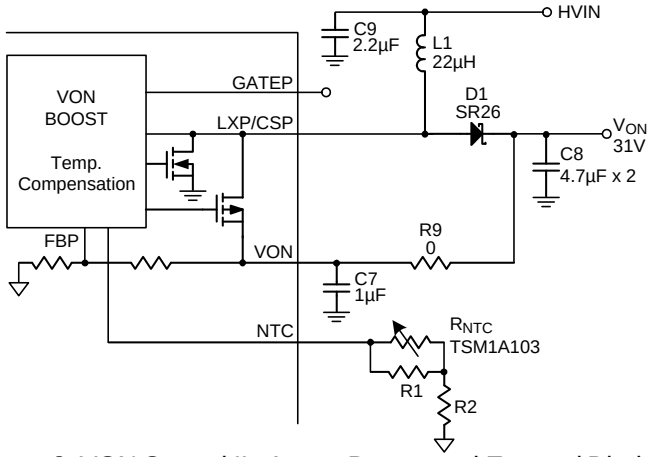


Figure 2. VON Control II : Async-Boost used External Diode

Register Address = 11h, Data = 10xxxxx1.

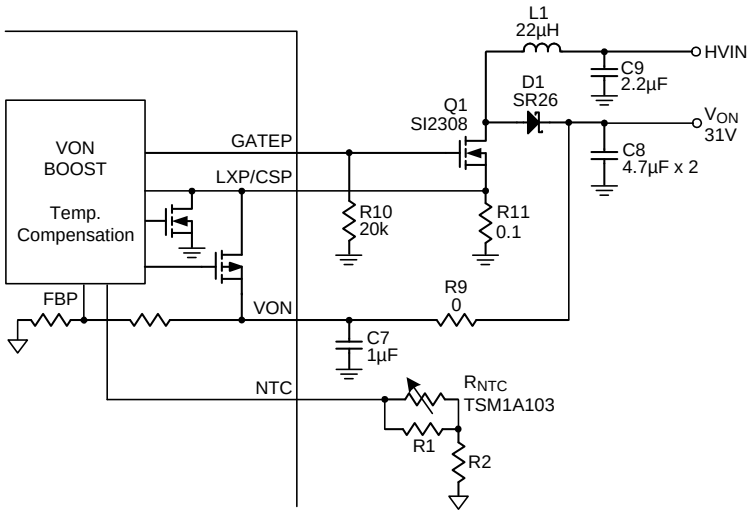


Figure 3. VON Control III : Async-Boost used External MOS and External Diode

Register Address =11h, Data = 11xxxxx1.

VOFF Buck-Boost Application Circuits

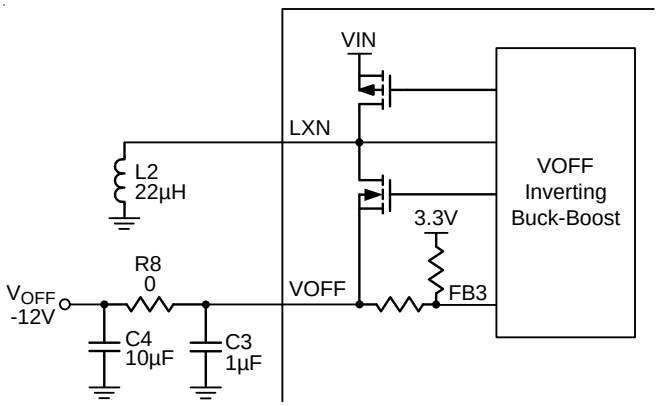


Figure 4. VOFF Control I : Sync-Buck-Boost

Register Address = 11h, Data = xx0xxxx1.

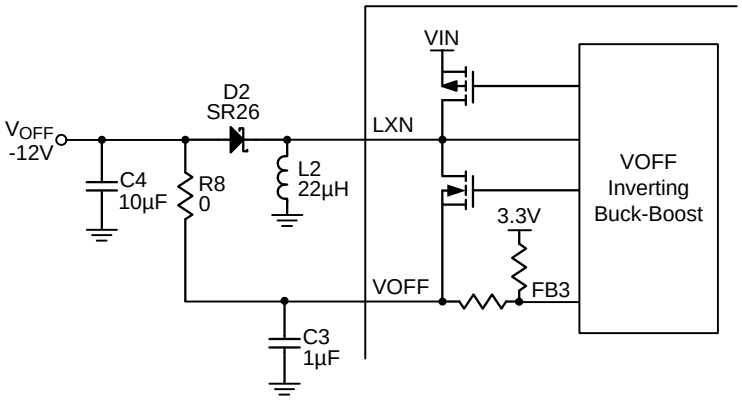


Figure 5. VOFF Control II : Async-Buck-Boost

Register Address = 11h, Data = xx1xxxx1.

VOFF Operating Frequency for Different Type Inductor		
Operating Frequency (kHz)	**Coil Inductor = 22µH**	**Chip Inductor = 6.8µH**
450	○	
600	○	
750	○	
900	○	○
1200		○
1350		○
1500		○
1800		○
2250		○
2700		○

Timing Diagram

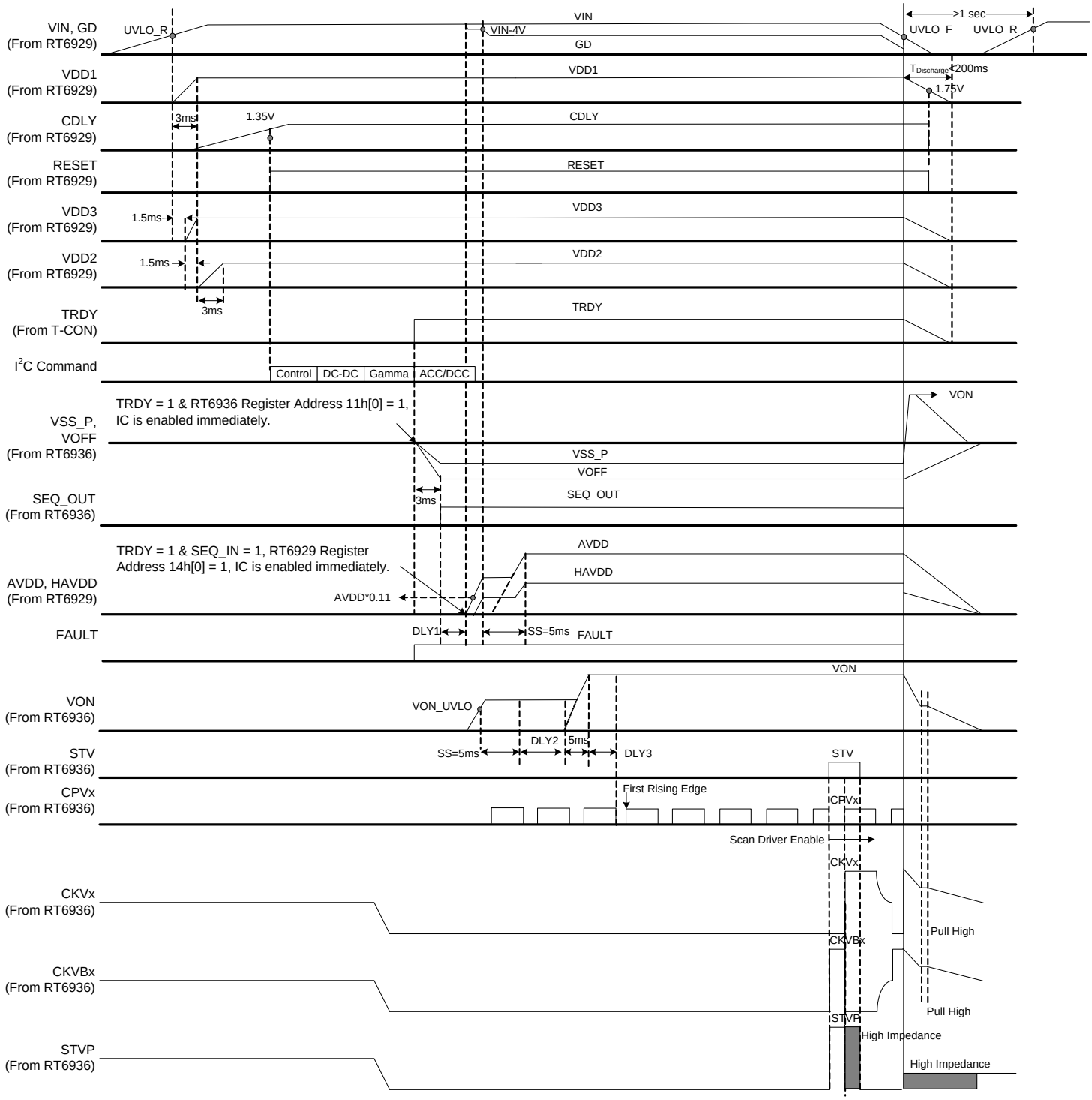


Figure 6. Normal Power Sequence

IC Standby

- TRDY = 0
- Register Address = 11h[0] = 0

Table 1. IC Shutdown Function

Address	Name	Shutdown Operation	
		Channel Shutdown	IC Shutdown
00h	VON_NT_Bank1	VON_NT_Bank1= 00h	VON_NT_Bank1 > E0h, VON_NT_Bank1 < 4Ah
01h	VOFF_NT_Bank1	VOFF_NT_Bank1= 00h	VOFF_NT_Bank1 > 86h, VOFF_NT_Bank1 < 18h
02h	VSS_Bank1	VSS_Bank1 = 00h	VSS_Bank1 > 7Ch, VSS_Bank1 < 13h
03h	VON_NT_Bank2	VON_NT_Bank2 = 00h	VON_NT_Bank2 > E0h, VON_NT_Bank2 < 4Ah
04h	VOFF_NT_Bank2	VOFF_NT_Bank2 = 00h	VOFF_NT_Bank2 > 86h, VOFF_NT_Bank2 < 18h
05h	VSS_Bank2	VSS_Bank2 = 00h	VSS_Bank2 > 7Ch, VSS_Bank2 < 13h
06h	VON_LT	VON_LT = 00h	VON_LT > E0h, VON_LT < 4Ah
07h	VOFF_LT	VOFF_LT = 00h	VOFF_LT > 86h, VOFF_LT < 18h
09h	VSS_HT	VSS_HT = 00h	VSS_HT > 7Ch, VSS_HT < 13h
			VON-VOFF > 60V

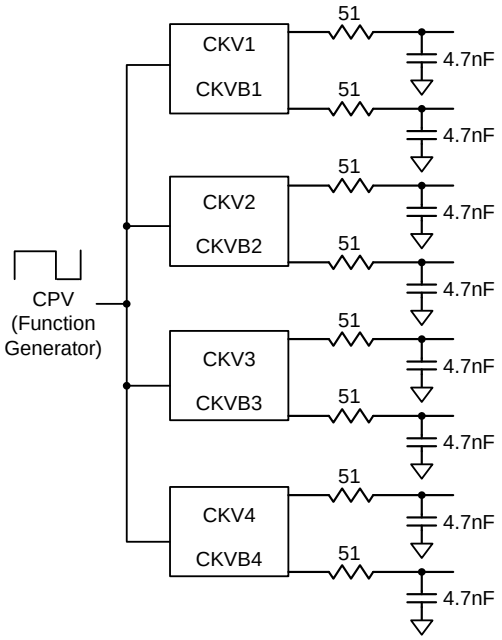
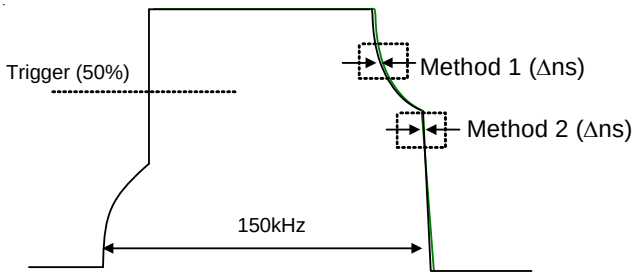


Figure 7. Output Loading of CKVx/CKVBx



Specification

Δns < ±0.01 x (1/150k) should be guaranteed at the same Load and the CPV of 150kHz (Oscilloscope Bandwidth = 500MHz)

Figure 8. Measurement Method

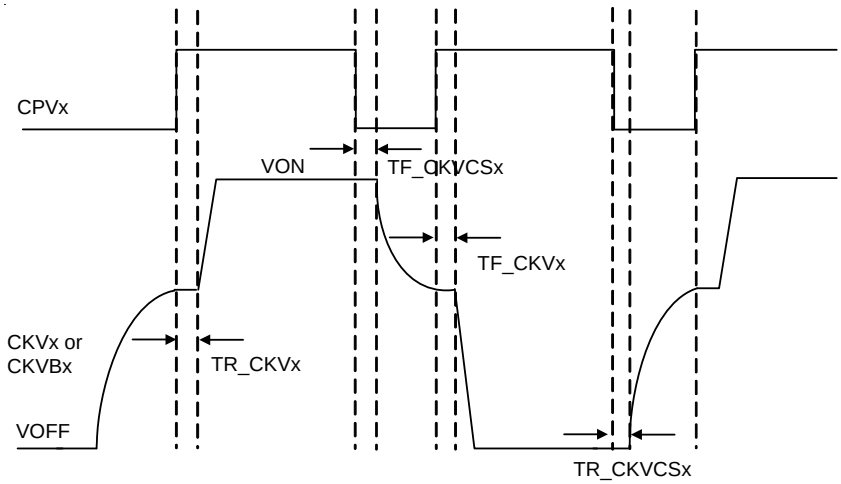


Figure 9. Propagation Delay Time of CKVx, CKVBx (STV = GND)

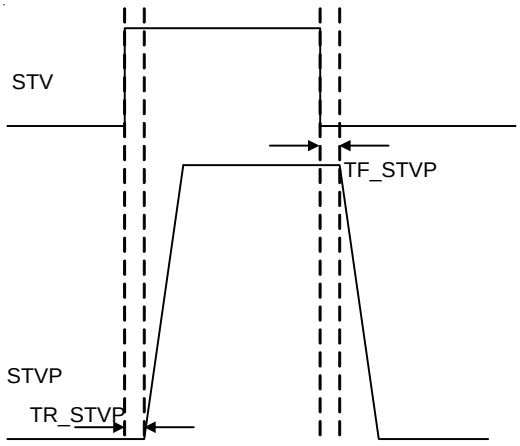


Figure 10. Propagation Delay Time of STVP (CKV1 = L)

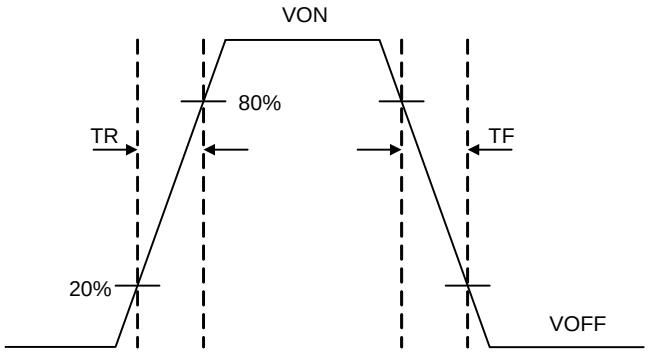


Figure 11. Rising Time and Falling Time of CKVx, CKVBx (STV = H) and STVP (CKV1 = L)

ASG Error Detect Method

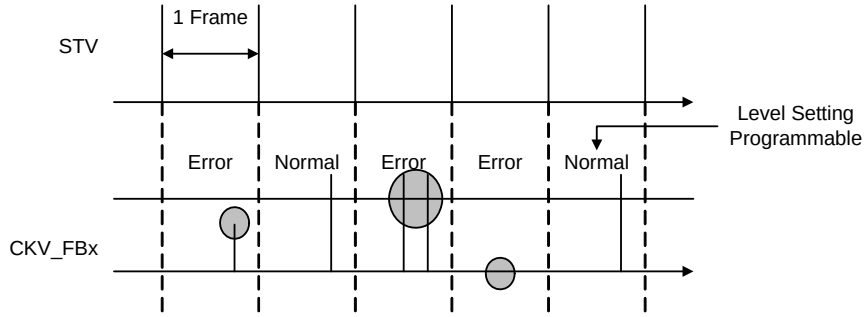


Figure 12 . STV 64 Time Count : Setting Error Count Detect→Data Writing (0→1)

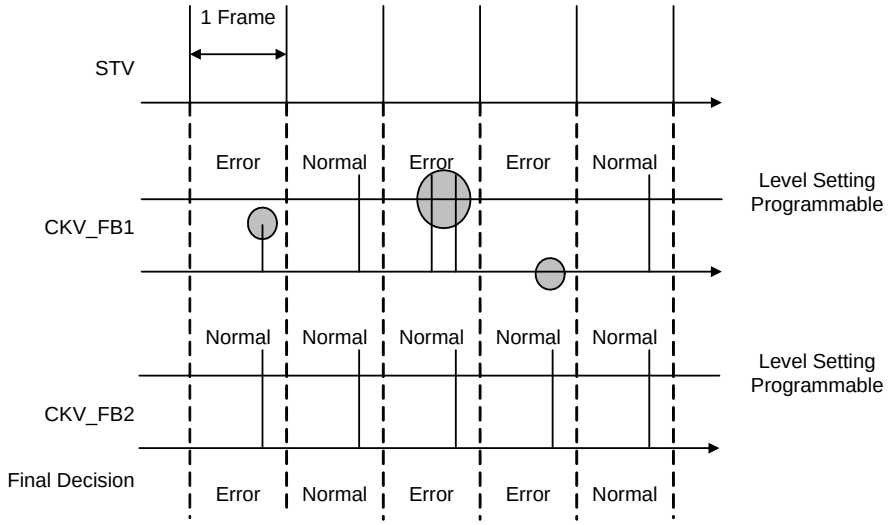


Figure 13. Dual Operating Detect Method

CKV Output Condition

A0 = 0 : Slave Address : 48h; Data →Normal : 00h ; Fault : A5h

A0 = 1 : Slave Address : 68h; Data →Normal : 00h ; Fault : A5h

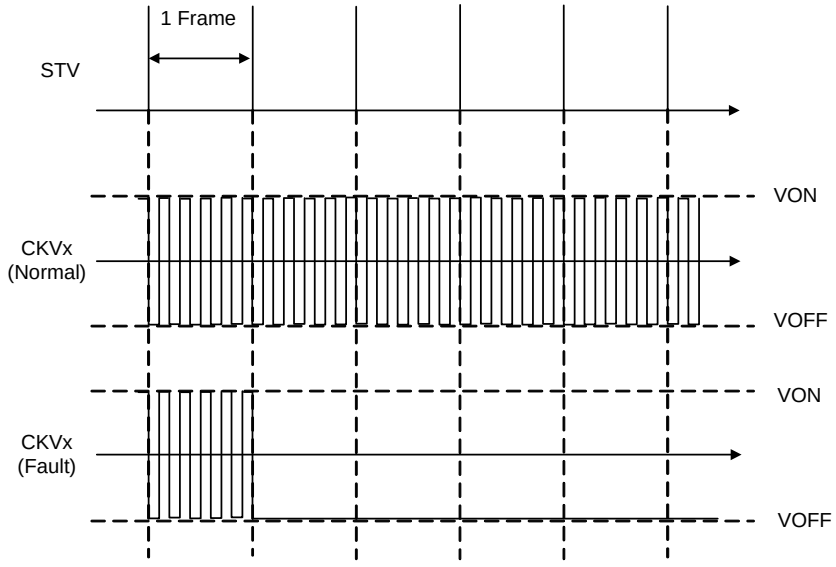
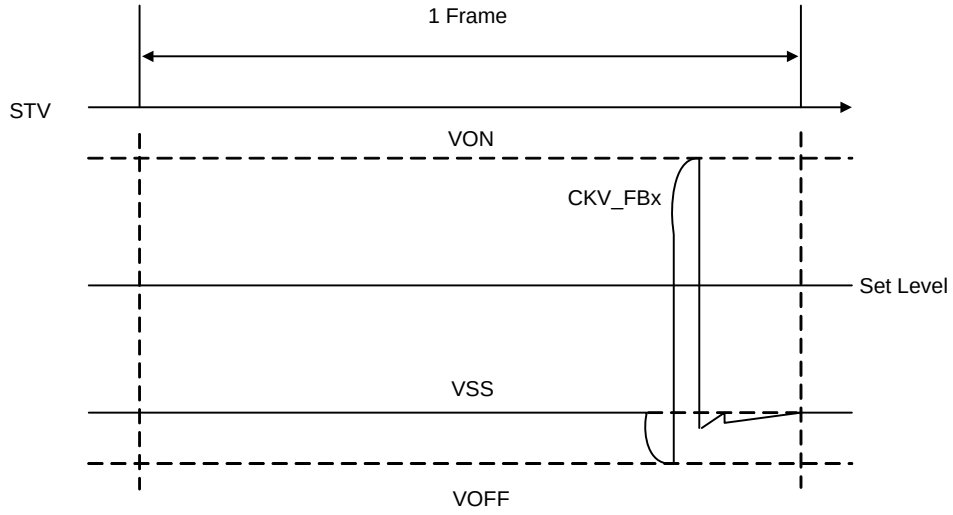


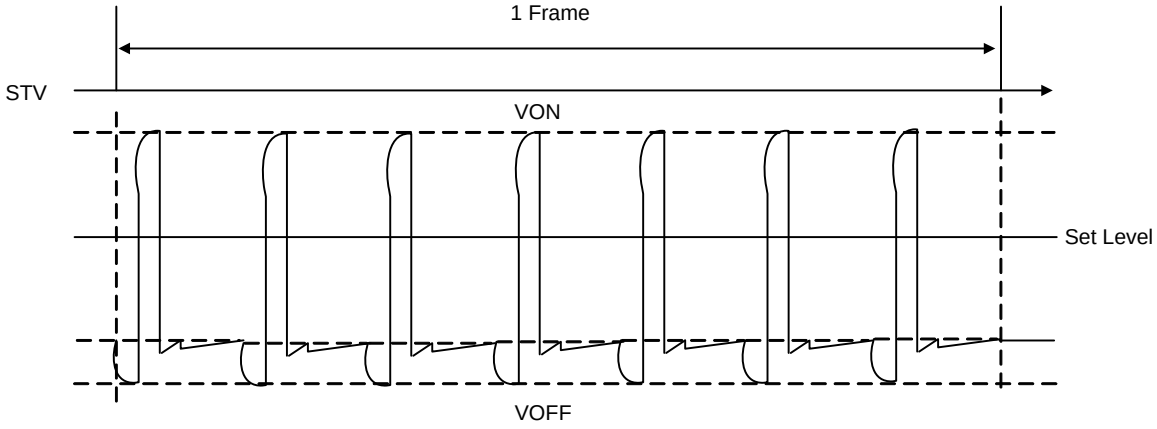
Figure 14. SCAN DRIVER Output Ratio During ASG Error

ASG Carry Waveform

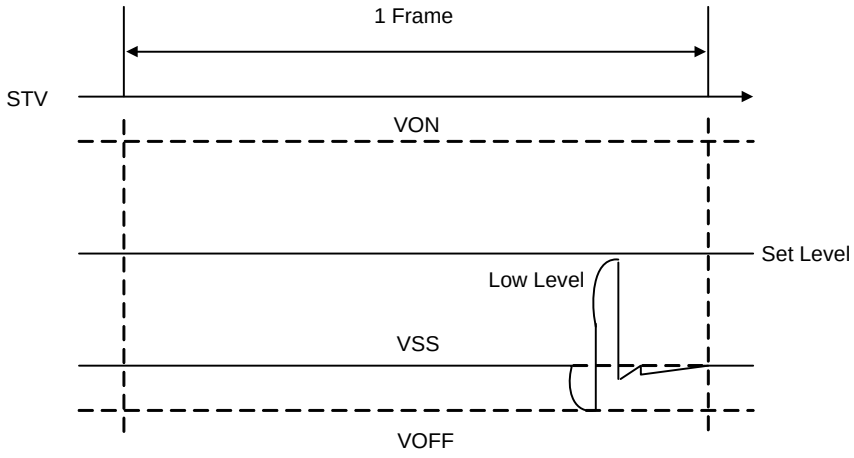
- **Normal Waveform (One Signal)**



- **Error Waveform Type (Normal Level Multi-Signal)**

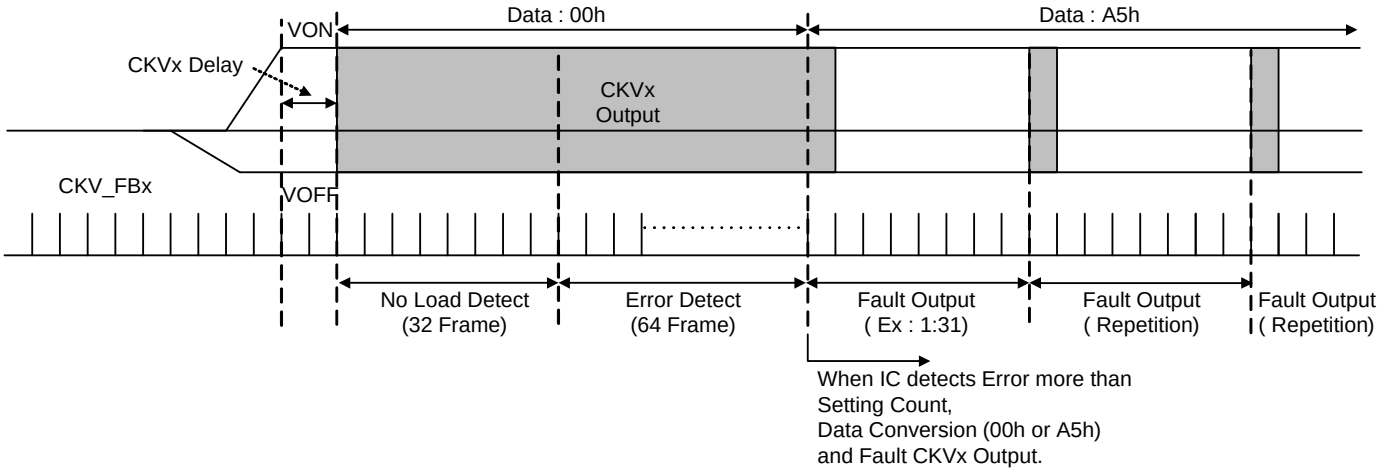


- **Error Waveform Type (Low Level Signals, or No Signal)**

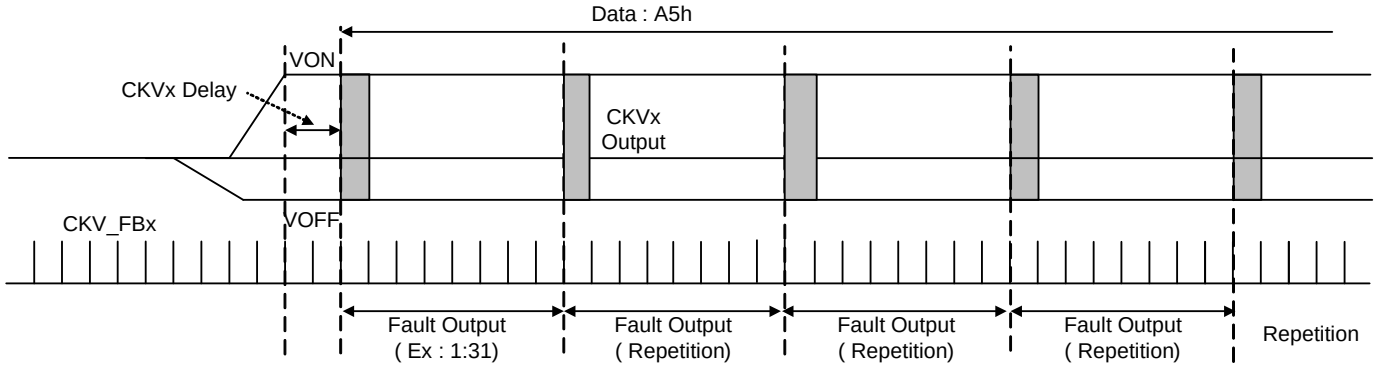


ASG Error

- **Normal Output with Slave Address 48h/68h data = 00h→A5h when power on.**



- **Abnormal Output with Slave Address 48h/68h data = A5h when power on.**

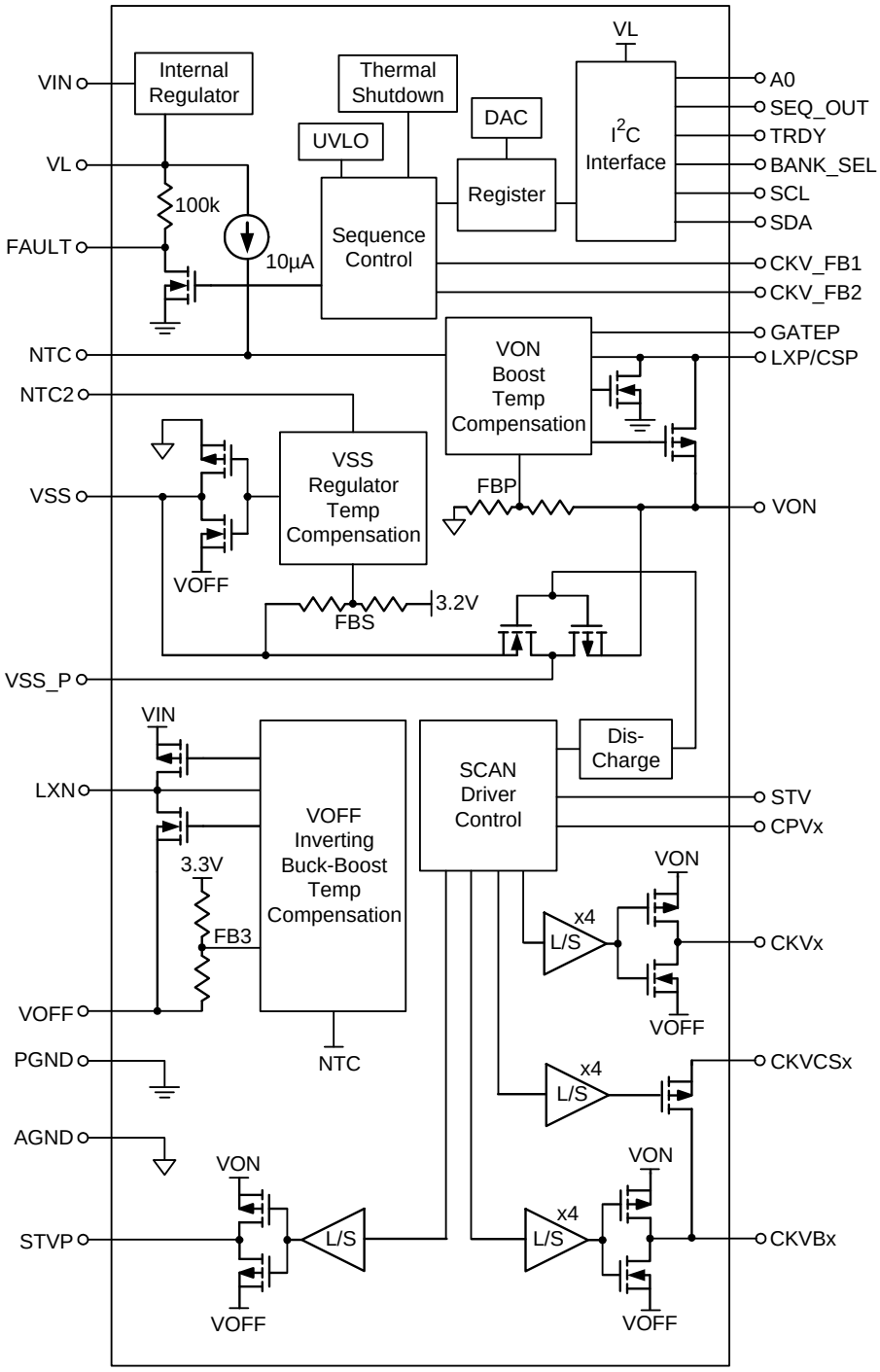


Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BANK_SEL	Bank select input for VON/VOFF/VSS of 2D/3D; 0 = output bank 1, 1 = output bank 2.
2	SDA	DATA I/O pin for the I^2C serial interface.
3	SCL	Clock input pin for the I^2C serial interface.
4	CPV1	SCAN driver clock signal 1 input pin.
5	CPV2	SCAN driver clock signal 2 input pin.
6	CPV3	SCAN driver clock signal 3 input pin
7	CPV4	SCAN driver clock signal 4 input pin.
8	STV	SCAN driver start signal input pin.
9	A0	Slave address assignment.
10	AGND	Analog ground.
11	VIN	Supply voltage input of VOFF buck-boost converter and VL internal regulator.
12	LXN	Switching node of VOFF inverting converter.
13	VOFF	Power input of SCAN driver. VOFF Inverting Feedback Input.
14	VSS	VSS negative linear regulator output.
15	VSS_P	VSS discharge switch output.
16	CKV_FB1	ASG carry feedback signal input1.
17	CKV_FB2	ASG carry feedback signal input2.
18	STVP	SCAN driver start signal output pin.
19	CKV1	SCAN driver clock signal 1 output pin.
20	CKVCS1	SCAN driver CKV1 charge share pin.
21	CKVB1	SCAN driver clock signal 1 inverting output pin.
22	CKV2	SCAN driver clock signal 2 output pin.
23	CKVCS2	SCAN driver CKV2 charge share pin.
24	CKVB2	SCAN driver clock signal 2 inverting output pin.
25	CKV3	SCAN driver clock signal 3 output pin.
26	CKVCS3	SCAN driver CKV3 charge share pin.
27	CKVB3	SCAN driver clock signal 3 inverting output pin.
28	CKV4	SCAN driver clock signal 4 output pin.
29	CKVCS4	SCAN driver CKV4 charge share pin.
30	CKVB4	SCAN driver clock signal 4 inverting output pin.
31	VON	VON boost feedback input and power input of SCAN driver.
32	LXP/CSP	Switching node of VON boost converter or switch current sensing input for VON boost converter.

Pin No.	Pin Name	Pin Function
33	PGND	Power ground.
34	GATEP	Gate drive output for VON boost converter.
35	NTC2	Slope setting pin for temperature compensation of the VSS converter.
36	NTC	Slope setting pin for temperature compensation of the VON and VOFF converter
37	FAULT	FAULT signal (DATA EN, SCP, TSD, UVLO) output & enable signal input.
38	SEQ_OUT	AVDD/HAVDD (RT6929) enable signal output.
39	TRDY	Enable signal input from T-CON.
40	VL	Internal linear regulator output.
41 (Exposed Pad)	PGND	Power ground. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- VIN to PGND ---------- –0.3V to 20V
- VIN to LXN ---------- –0.3V to 50V
- VOFF, VSS to PGND ---------- –30V to 0.3V
- VON, LXP/CSP to PGND ---------- –0.3 to 50V
- NTC, NTC2, SDA, SCL, CPVx, STV, TRDY, BANK_SEL, A0, GATEP, FAULT, SEQ_OUT, VL to AGND ---------- –0.3 to 6V
- CKVFB1, CKVFB2, VSS_P, STVP, CKVx, CKVBx, CKVCSx to PGND ---------- –30 to 47V
- VON to VOFF ---------- 60V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-40L 6x6 ---------- 3.69W
- Package Thermal Resistance (Note 2)
  WQFN-40L 6x6, θ_{JA} ---------- 27.1°C/W
  WQFN-40L 6x6, θ_{JC} ---------- 4.9°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, V_{ON} = 31V, V_{OFF} = –12V, V_{SS} = –7.6V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
Input Voltage Range	V_{IN}		9.5	--	14.7	V
VIN Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} Falling	7.7	8.15	8.6	V
		V_{IN} Rising	8.5	8.8	9.1	V
VIN Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}		0.5	0.65	0.8	V
VON Start-up Trigger Voltage	V_{ON_SS}	V_{ON} Falling	6.8	7.25	7.7	V
		V_{ON} Rising	7.6	7.9	8.2	V
VON Start-up Trigger Voltage Hysteresis	$V_{ON\_SS\_HYS}$		0.5	0.65	0.8	V
Quiescent Current into VIN	I_{Q_VIN}	LXP/CSP, LXN No Switching	--	3.3	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VL Output Voltage	V_L		4.5	5	5.5	V
VL Start Threshold Voltage	V_{L_START}		--	4.1	--	V
VL Stop Threshold Voltage	V_{L_STOP}		--	3.5	--	V
VL UVLO Hysteresis	V_{L_HYS}		--	0.6	--	V
EEPROM Write Guarantee			1000	--	--	Count
Thermal Shutdown Threshold			150	165	180	°C
Thermal Shutdown Hysteresis			--	20	--	°C
Internal Oscillator						
Oscillator Frequency11	F_{OSC11}	Initial Frequency 10h[3:2] = “00”	360	450	540	kHz
Oscillator Frequency12	F_{OSC12}	Initial Frequency 10h[3:2] = “01”	480	600	720	kHz
Oscillator Frequency13	F_{OSC13}	Initial Frequency 10h[3:2] = “10”	600	750	900	kHz
Oscillator Frequency14	F_{OSC14}	Initial Frequency 10h[3:2] = “11”	720	900	1080	kHz
Oscillator Frequency21 (VOFF)	F_{OSC21}	Initial Frequency “00” x 2	720	900	1080	kHz
Oscillator Frequency22 (VOFF)	F_{OSC22}	Initial Frequency “01” x 2	960	1200	1440	kHz
Oscillator Frequency23 (VOFF)	F_{OSC23}	Initial Frequency “10” x 2	1200	1500	1800	kHz
Oscillator Frequency24 (VOFF)	F_{OSC24}	Initial Frequency “11” x 2	1440	1800	2160	kHz
Oscillator Frequency31 (VOFF)	F_{OSC31}	Initial Frequency “00” x 3	1080	1350	1620	kHz
Oscillator Frequency32 (VOFF)	F_{OSC32}	Initial Frequency “01” x 3	1440	1800	2160	kHz
Oscillator Frequency33 (VOFF)	F_{OSC33}	Initial Frequency “10” x 3	1800	2250	2700	kHz
Oscillator Frequency34 (VOFF)	F_{OSC34}	Initial Frequency “11” x 3	2160	2700	3240	kHz
BOOST Converter (VON)						
Soft Start Period	T_{SS_VON}		4	5	6	ms
Adjustable Normal VON Output Voltage Range	V_{ON}	Register Address = 00h/03h/06h, 8 bits, V_{ON} = 15V to 45V, [4Ah to E0h]	15	--	45	V
VON Regulation Voltage (Normal Temp Default)	V_{ON_NT}	No Load, ±3.0% Error	30.07	31	31.93	V
VON Regulation Voltage (Low Temp Default)	V_{ON_LT}	No load, ±3.0% Error, NTC Option 10h[4] = 0	36.86	38	39.14	V
VON Fault Trip Level	V_{FT_VON}	VON Falling, 0Ch[0] = 0	VON x 0.7125	VON x 0.75	VON x 0.7875	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
LXP/CSP Current Limit	$I_{LIM\_LXP/CSP}$	Register Address = 0Dh, (Internal MOS) [7:5] = 111 VON_OCP[7:5] Control OCPLevel from 0.5A to 2.25A, 1 Step 0.25A	2.25	2.8	3.35	A
LXP/CSP Maximum Duty	$D_{MAX\_LXP/CSP}$		--	90	--	%
LXP/CSP to PGND N-MOSFET On-Resistance	$R_{DS(ON)\_LXP\_LG}$	$I_{LXP/CSP}$ = 0.2A	0.3	0.5	0.7	Ω
LXP/CSP to VON N-MOSFET On-Resistance	$R_{DS(ON)\_LXP/CSP\_UG}$	$I_{LXP/CSP}$ = 0.2A	0.3	0.5	0.7	Ω
LXP/CSP to PGND N-MOSFET Leakage Current	$I_{LEAK\_LXP\_LG}$	$V_{LXP/CSP}$ – PGND = 45V	--	--	5	μA
LXP/CSP to VON N-MOSFETLeakage Current	$I_{LEAK\_LXP\_UG}$	V_{ON} – V_{LXP} = 45V	--	--	5	μA
Load Regulation		0 < I_{LOAD} < 0.2A	–1	--	1	%
Line Regulation		V_{IN} = 9.5 to 14.7V, I_{LOAD} = 0.1A	–1	--	1	%
VON Over-Voltage Protection	V_{ON_OVP}	VON Rising	45.6	47.5	49.4	V
LXP/CSP Threshold Voltage	$V_{LXP/CSP}$	Sense Resistor = 0.1Ω Register Address = 0Dh, (External MOS) [7:5] = 111 VON_OCP[7:5] Control OCP Level from 0.05V to 0.225V, 1 step = 0.025V	0.225	0.28	0.335	V
GATEP High Voltage	V_{GPH}		2	--	VL	V
GATEP Low Voltage	V_{GPL}		0	-	1	V
GATEP ON-Resistance	R_{GP_UG}	Register Address = 0Eh, [5:4] = 00 GATEP_SR[5:4], 10/20/40/80Ω I_{GATEP} = 10mA for External MOS	--	10	--	Ω
Output Resolution	RES_{VON}		--	0.2	--	V
Integral Non-Linearity	INL_{VON}		–1	--	1	LSB
Differential Non-Linearity	DNL_{VON}		–1	--	1	LSB
Device Temperature Control						
NTC Source Current	I_{NTC}		9	10	11	μA
DTC Gain (VON)	$Gain_{VON}$	NTC Select = 0	--	1.5	--	V/V
DTC Gain (VOFF)	$Gain_{VOFF}$	NTC Select = 1	--	2	--	V/V
DTC Gain (VSS)	$Gain_{VSS}$	Register Address = 09h, VSS_HT_Sel [7] = 0	--	0.5	--	V/V
NTC Hysteresis	NTC_{HYS}	For VON and VOFF	--	50	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Negative BUCK-BOOST Converter (VOFF)						
Soft Start Period	T_{SS_VOFF}		2.4	3	3.6	ms
VIN Overvoltage Protection	V_{OVP_VIN}	VIN Rising, Hysteresis = 0.3V	15	--	18	V
Adjustable Normal VOFF Output Voltage Range	V_{OFF}	Register Address = 01h/04h/07h, 8 bits, V_{OFF_NT} = –5V to –27V [18h to 86h]	–27	--	–5	V
VOFF Regulation Voltage (Normal Temp Default)	V_{OFF_NT}	No load, ±3.0% Error	–12.36	–12	–11.64	V
VOFF Regulation Voltage (Low Temp Default)	V_{OFF_LT}	No load, ±3.0% Error, NTC Option 10h[4] = 1	–22.66	–22	–21.34	V
VOFF Fault Trip Level	V_{FT_VOFF}	VOFF Falling	VOFF x 0.7125	VOFF x 0.75	VOFF x 0.7875	V
VIN to LXN MOSFET On-Resistance	$R_{DS(ON)\_LXN\_LG}$	I_{LXN} = 0.2A	0.6	1	1.4	Ω
LXN to VOFF MOSFET On Resistance	$R_{DS(ON)\_LXN\_UG}$	I_{LXN} = 0.2A	0.3	0.5	0.7	Ω
LXN Current Limit	$I_{LIM\_LXN2,3}$	Frequency Select 10h[1:0] = x2, x3	1	1.25	1.5	A
LXN Current Limit	I_{LIM_LXN1}	Initial Frequency 10h[3:2] = x1	2	2.5	3	A
LXN Maximum Duty	D_{MAX_LXN}		--	90	--	%
VIN to LXN Leakage Current	$I_{Leak\_LXN\_LG}$	V_{IN} - V_{LXN} = –40V	--	--	5	μA
LXN to VOFF Leakage Current	$I_{Leak\_LXN\_HG}$	V_{LXN} - V_{OFF} = –40V	--	--	5	μA
Load Regulation		0 < I_{LOAD} <0.2A	–1	--	1	%
Line Regulation		V_{IN} = 9.5 to 14.7V, I_{LOAD} = 0.1A	–1	--	1	%
VOFF Over-Voltage Protection	V_{OVP_VOFF}		–27.5	–28.5	–30	V
Output Resolution	RES_{VOFF}		--	-0.2	--	V
Integral Non-Linearity	INL_{VOFF}		–1	--	1	LSB
Differential Non-Linearity	DNL_{VOFF}		–1	--	1	LSB
VOFF Discharge ON Resistance	$R_{ON\_DIS\_VOFF}$		--	100	--	Ω
VOFF ΔV Function						
ΔV Voltage	V_{Delta}	ΔV = VSS – VOFF	1.6	4	14	V
Output Resolution	V_{RES}		--	0.2	--	V
ΔV Voltage	V_{VDelta}	No load, ±3% Error	3.88	4	4.12	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Negative Regulator (VSS)							
Soft-Start Period		T_{SS_VSS}		2.4	3	3.6	ms
Adjustable Normal VSS Output Voltage Range		V_{SS}	Register Address = 02h/05h/09h, 8bits, V_{SS} = –4V to –25V. [13h to 7Ch]	–25	--	–4	V
VSS Regulation Voltage (Normal Temp Default)		V_{SS_NT}	No load, ±3% Error	–7.83	–7.6	–7.37	V
VSS Fault Trip Level		V_{FT_VSS}	VSS Falling	VSS x 0.7125	VSS x 0.75	VSS x 0.7825	V
Output Voltage Swing Low		V_{OL_VSS}	I_{VSS} = 10mA	--	VOFF +0.2	--	V
VSS Continuous Current		I_{VSS_CC}	VSS = –7.6V, Source or Sink	100	--	--	mA
VSS_P SW On Resistance		R_{VSS_P}	VSS –VSS_P, I_{VSS_P} = 10mA	--	1.2	--	Ω
Discharge SW ON Resistance		R_{ON_DIS}	I_{DIS} = 10mA	--	75	--	Ω
Output Resolution		Res		--	–0.2	--	V
Integral Non-Linearity		INL_{VSS}		–1	--	1	LSB
Differential Non-Linearity		DNL_{VSS}		–1	--	1	LSB
Sequence Control Pins SEQ_OUT, FAULT							
FAULT Trigger Duration		T_{DFAULT}		2.5	3	3.5	ms
FAULT Pull Up Resistance		R_{SEQ}		100	--	--	kΩ
FAULT Output Voltage	High Level	VOH_{FAULT}		2	--	--	V
	Low Level	VOL_{FAULT}		--	--	1	V
Pull Low Voltage (FAULT)			I_{ON} = 3mA	--	--	0.4	V
SEQ_OUT Output Voltage	High Level	$V_{SEQ\_OUT\_OH}$	I_{OUT} = 2mA	VL – 0.2	VL – 0.1	VL – 0.01	V
	Low Level	$V_{SEQ\_OUT\_OL}$	I_{OUT} = 2mA	0.01	0.1	0.2	V
Logic Signals SDA, SCL, CPVx, STV, TRDY, BANK_SEL, A0							
Input Voltage	High-Level	V_{IH}		1.5	--	--	V
	Low-Level	V_{IL}		--	--	0.8	V
A0 Pull Up Resistance		R_{A0}	VL Pull Up	100	--	--	kΩ
TRDY Pull Down Resistance		R_{TRDY}		100	--	--	kΩ
BANK_SEL Input current		$I_{IN\_BANK\_SEL}$	V_{BANK_SEL}= 2V	9.3	13.3	17.3	µA
SDA, SCL Input current		$I_{IN\_SDA/SCL}$	$V_{SDA/SCL}$= 2V	–2	0	2	µA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
CPVx Pull Down Resistance		R_{CPV}		100	--	--	kΩ
STV Pull Down Resistance		R_{STV}		100	--	--	kΩ
SDA_ACK ON Voltage		V_{ACK}	I_{SDA} = 3mA	--	--	0.4	V
SCL Frequency		F_{CLK}		--	--	1	MHz
SCL Period	High Period	t_{HIGH}		0.3	--	--	μs
	Low Period	t_{LOW}		0.4	--	--	μs
SCL Rise Time		t_{R_SCL}		--	--	0.12	μs
SCL Fall Time		t_{F_SCL}		--	--	0.12	μs
Start Condition Hold Time		t_{HD_STA}		0.25	--	--	μs
Start Condition Setup Time		t_{SU_STA}		0.25	--	--	μs
SDA Hold Time		t_{HD_DAT}		50	--	--	ns
SDA Setup Time		t_{SU_DAT}		50	--	--	ns
ACK Delay Time		t_{PD}		--	--	0.35	μs
ACK Hold Time		t_{HD}		--	0.1	--	μs
Stop Condition Setup Time		t_{SU_STO}		0.25	--	--	μs
Bus Free Time		t_{BUF}		0.5	--	--	μs
Bus Capacitance		C_B		--	--	400	pF
Spike Rejection Pulse Width		t_L		--	0.05	--	μs
Monitoring Function							
VON Voltage Resolution		RES_{M_VON}		--	4	--	Bit
Voltage Monitoring Tolerance		TL_{VON}		–3	--	3	%
Die Temperature Resolution		RES_{DT}		--	4	--	Bit
Die Temperature Monitoring Tolerance		TL_{DT}		–7	--	7	%
Scan Driver							
VON-VOFF				--	--	60	V
VON Quiescent Current		I_{Q_VON}	No Switching	--	1.3	--	mA
VOFF Quiescent Current		I_{Q_VOFF}	No Switching	--	1.45	--	mA
CPVx Input Frequency		F_{CPV}		--	--	150	kHz

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
CKVx, CKVBx Output Voltage	Logic-High	V_{OH}	I_{SOURCE} = 10mA	VON–0.15	VON–0.05	VON–0.02	V
	Logic-Low	V_{OL}	I_{SINK} = 10mA	VOFF + 0.02	VOFF + 0.05	VOFF+0.15	V
STVP Output Voltage	Logic-High	V_{OH}	I_{SOURCE} = 10mA	VON – 0.3	VON–0.15	VON – 0.05	V
	Logic-Low	V_{OL}	I_{SINK} = 10mA	VOFF+ 0.05	VOFF + 0.15	VOFF+ 0.3	V
STVP Output Rising Slew Rate		$Slew+_{STVP}$	R_{LOAD} = 51Ω, C_{LOAD} = 4.7nF	100	1000	--	V/μs
STVP Output Falling Slew Rate		$Slew-_{STVP}$		100	1000	--	V/μs
STVP Rising Edge Propagation Delay Time		$T_{pr-STVP}$	No capacitive Load	--	90	150	ns
STVP Falling Edge Propagation Delay Time		$T_{pf-STVP}$		--	90	150	ns
CKVx Output Rising Slew Rate		$Slew+_{CKVx}$	F_{CPVx} = 85kHz, STV= 3.3V, R_{LOAD} = 51Ω, C_{LOAD} = 4.7nF	700	1000	1300	V/μs
CKVx Output Falling Slew Rate		$Slew-_{CKVx}$		700	1000	1300	V/μs
CKVBx Output Rising Slew Rate		$Slew+_{CKVBx}$		700	1000	1300	V/μs
CKVBx Output Falling Slew Rate		$Slew-_{CKVBx}$		700	1000	1300	V/μs
CKVx Rising Edge Propagation Delay Time		T_{r-CPVx_CKVx}	No capacitive Load	--	90	150	ns
CKVx Falling Edge Propagation Delay Time		T_{f-CPVx_CKVx}		--	90	150	ns
CKVBx Rising Edge Propagation Delay Time		T_{r-CPVx_CKVBx}		--	90	150	ns
CKVBx Falling Edge Propagation Delay Time		T_{f-CPVx_CKVBx}		--	90	150	ns
CKVxCS Rising Edge Propagation Delay Time		$T_{csr-CPVx\_CKVx}$	F_{CPVx} = 85kHz, STV = 0V, No capacitive Load	--	150	300	ns
CKVxCS Falling Edge Propagation Delay Time		$T_{csr-CPVx\_CKVBx}$		--	150	300	ns
Propagation Delay Time Relative Variation			⊿Tf_cs_typ = ⊿Tf_ckv_typ = 1/150kHz	–1	0	1	%
Scan Driver OCP Filter Check		T_{FLT}	08h [1:0] = 0h	0.85	1.13	1.41	μs
			08h [1:0] = 1h	1.7	2.27	2.84	
			08h [1:0] = 2h	3.4	4.53	5.66	
			08h [1:0] = 3h	5.95	7.93	9.91	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Scan Driver OCP Filter Check	$T_{ILIM\_CKVx, CKVBx}$	0Ch, CKVOCP Level [4:1] = 1h	14	28	34	mA
		0Ch, CKVOCP Level [4:1] = 2h	40	47	54	
		0Ch, CKVOCP Level [4:1] = 3h	60	71	82	
		0Ch, CKVOCP Level [4:1] = 4h	80	94	108	
		0Ch, CKVOCP Level [4:1] = 5h	100	118	136	
		0Ch, CKVOCP Level [4:1] = 6h	120	141	162	
		0Ch, CKVOCP Level [4:1] = 7h	140	165	190	
		0Ch, CKVOCP Level [4:1] = 8h	160	188	216	
		0Ch, CKVOCP Level [4:1] = 9h	180	212	244	
		0Ch, CKVOCP Level [4:1] = Ah	200	235	270	
		0Ch, CKVOCP Level [4:1] = Bh	220	259	298	
		0Ch, CKVOCP Level [4:1] = Ch	240	282	324	
		0Ch, CKVOCP Level [4:1] = Dh	260	306	352	
		0Ch, CKVOCP Level [4:1] = Eh	280	329	378	
		0Ch, CKVOCP Level [4:1] = Fh	300	353	406	
ASG Error Detect Function						
CKV_FB1,2 Input Range	$V_{CKV\_FB1,2}$		VOFF	--	VON	V
CKV_FB1,2 Pull Down Resistance (to VSS)	$R_{CKV\_FB1,2}$		100	--	--	kΩ
ASG Error Detect Voltage	V_{ASG_DET}		VON *1/8	--	VON *7/8	V
No Load Detect Voltage	NL_DET	0Bh[4:3] = 01	4	--	--	V

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

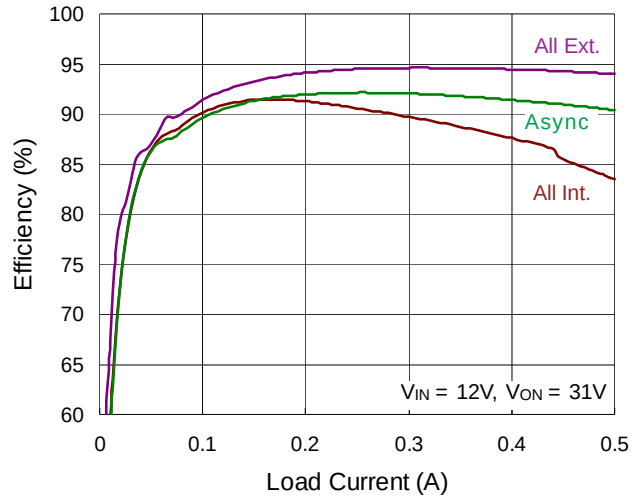
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

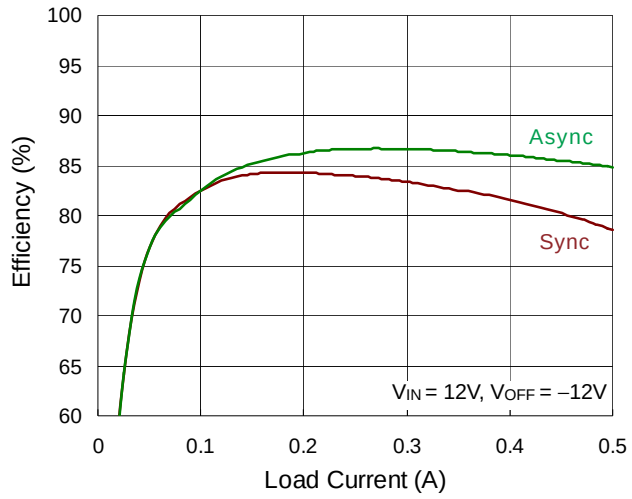
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

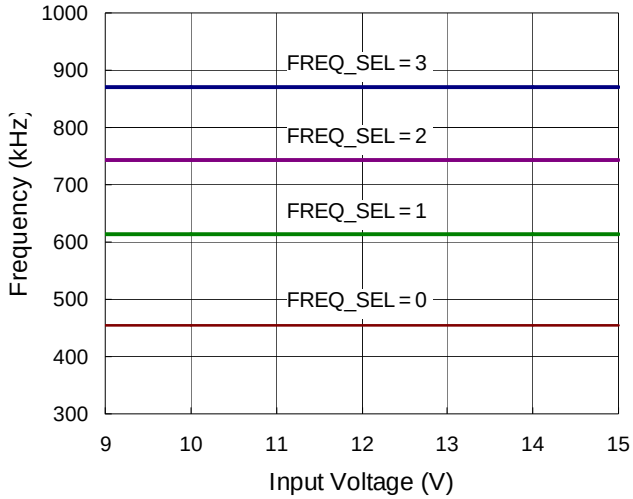
VON Boost Efficiency vs. Load Current



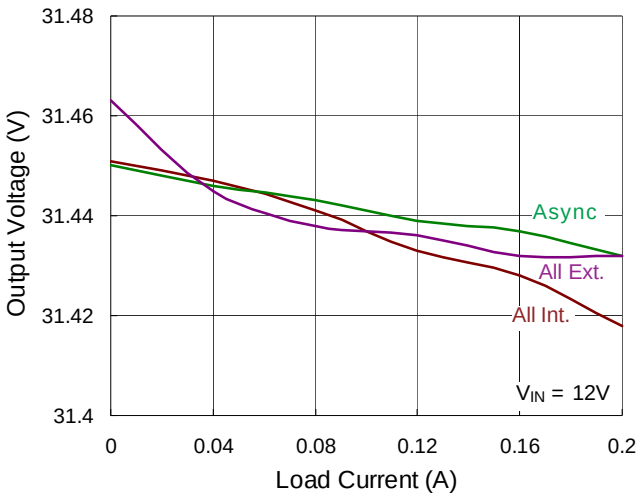
VOFF Inverting Efficiency vs. Load Current



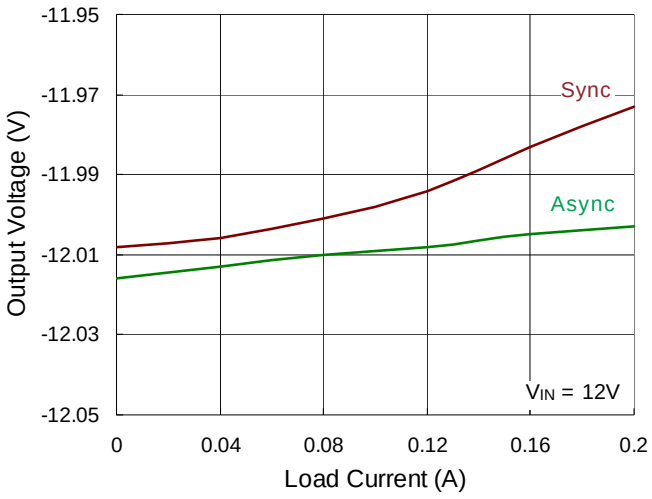
VON/VOFF Initial Switching Frequency vs. Input Voltage



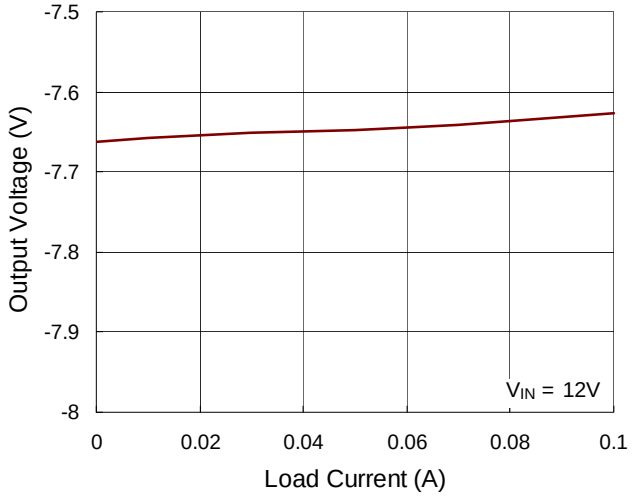
VON Output Voltage vs. Load Current



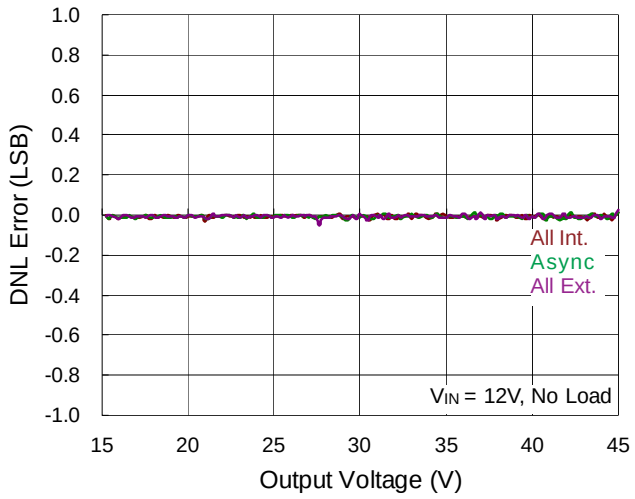
VOFF Output Voltage vs. Load Current



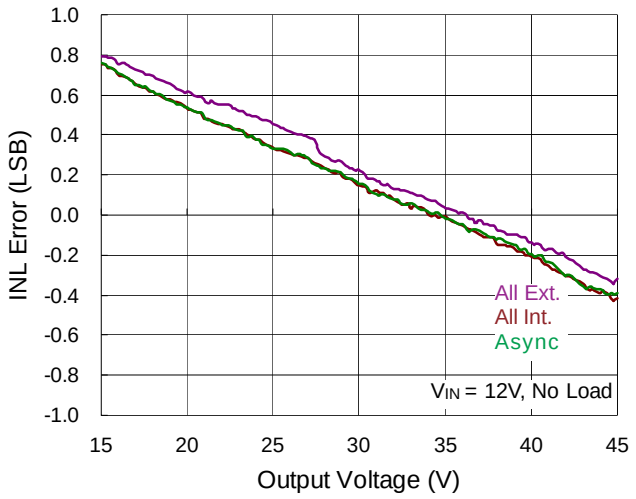
VSS Output Voltage vs. Load Current



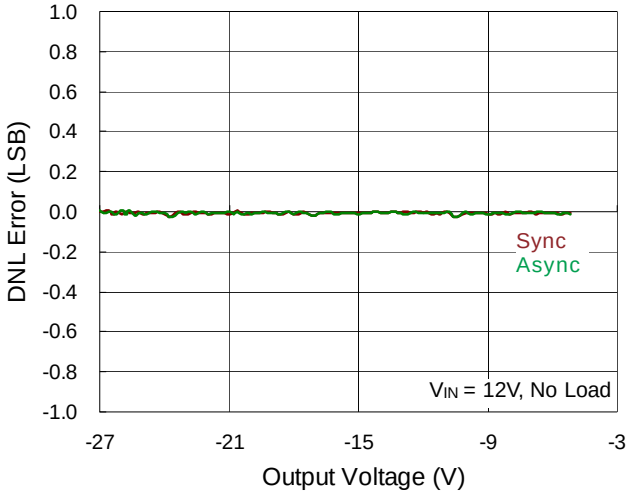
VON DNL Error vs. Output Voltage



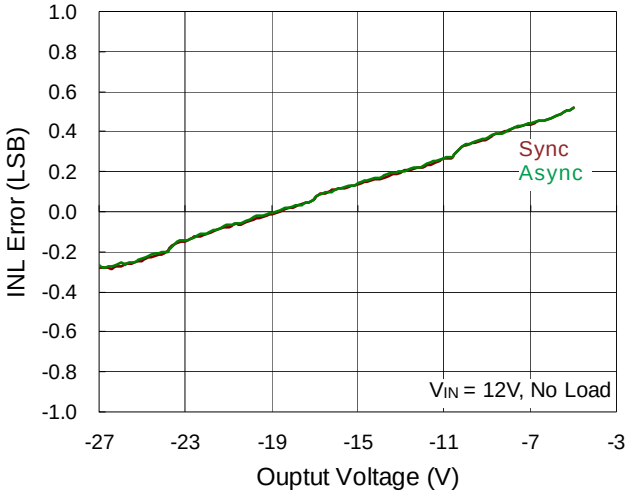
VON INL Error vs. Output Voltage



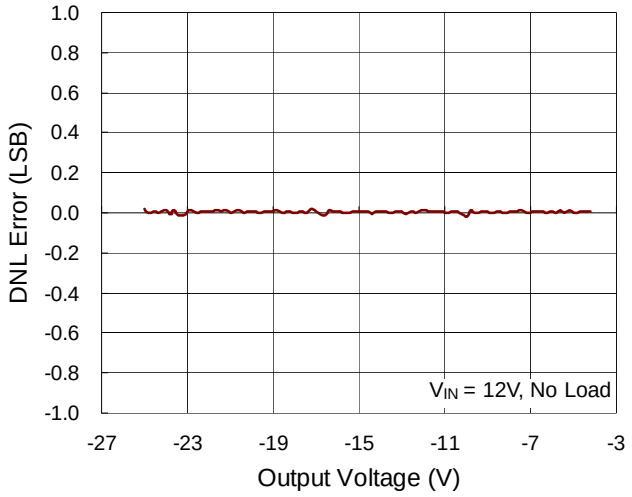
VOFF DNL Error vs. Output Voltage



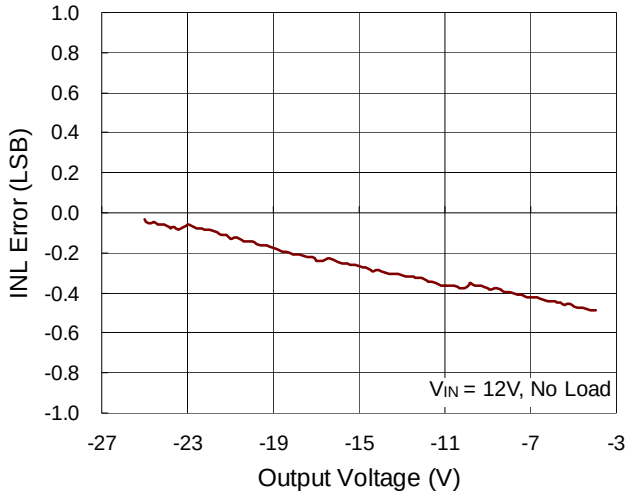
VOFF INL Error vs. Output Voltage



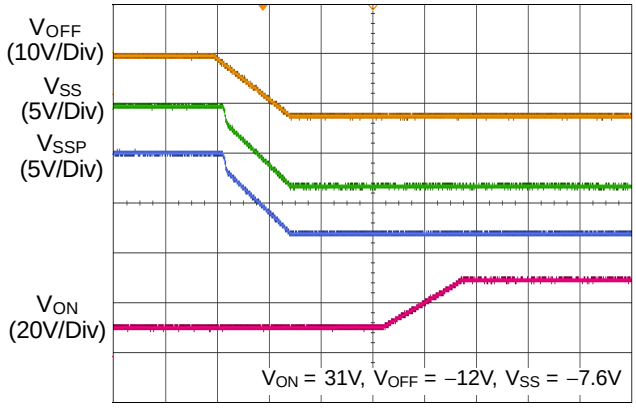
VSS DNL Error vs. Output Voltage



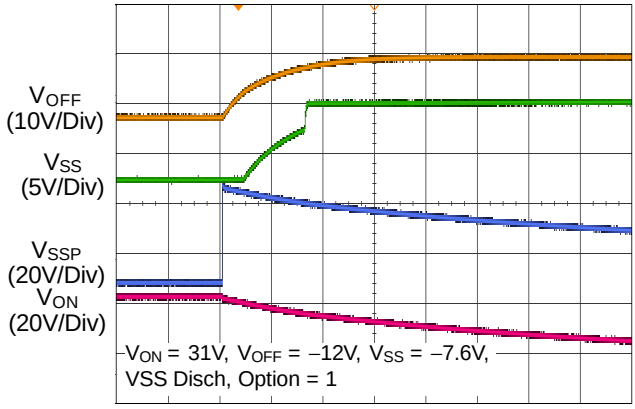
VSS INL Error vs. Output Voltage



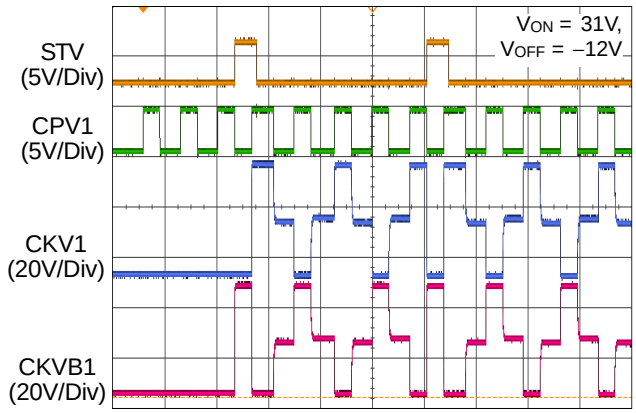
Power On



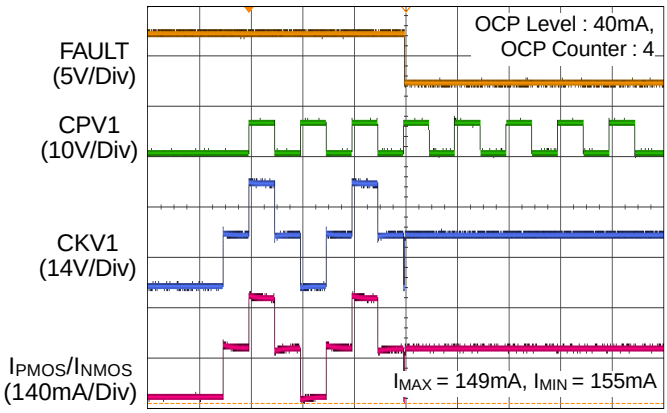
Power Off



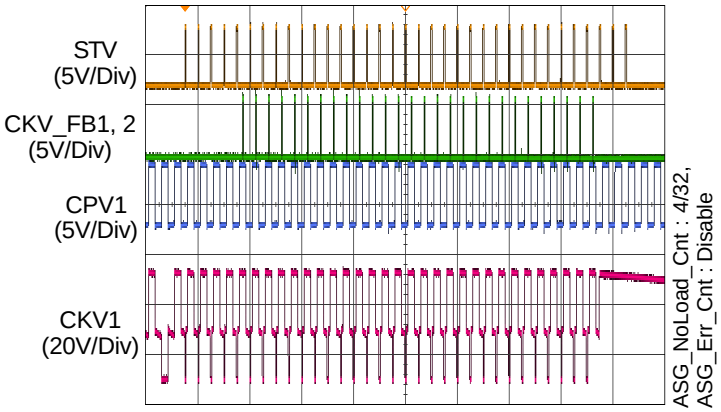
Scan Driver Function



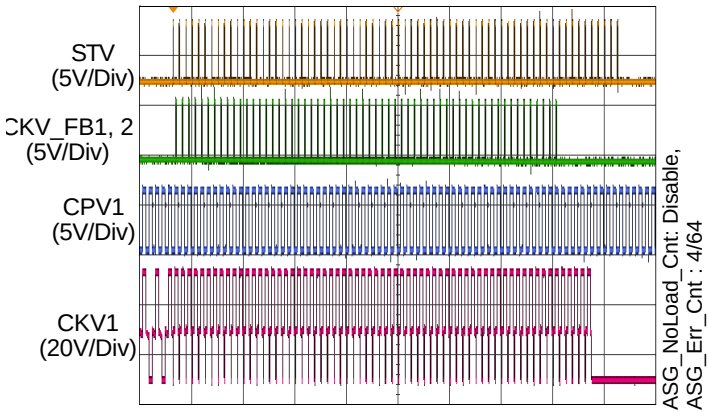
Scan Driver OCP Function



ASG No Load Detect Function



ASG Error Detect Function



I²C Command

Single I²C Register Write Protocol

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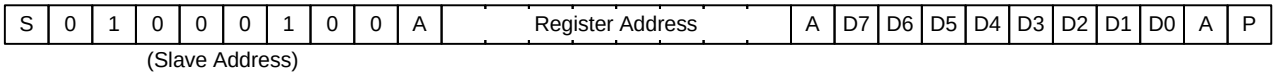

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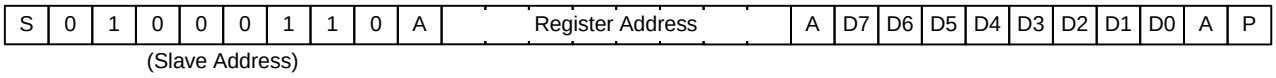

Single I²C Register Read Protocol

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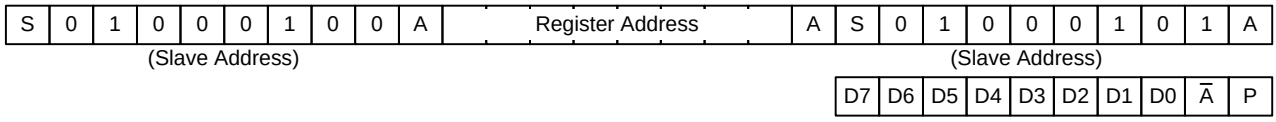

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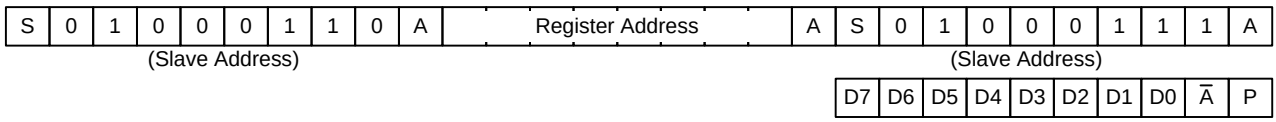

Multiple I²C Register Write Protocol

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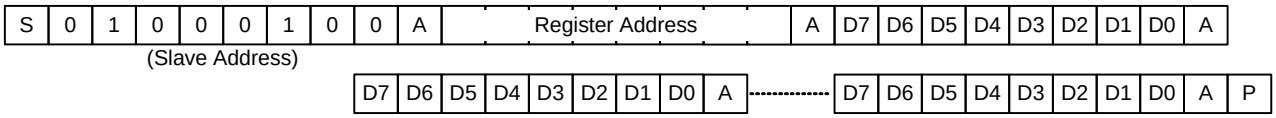

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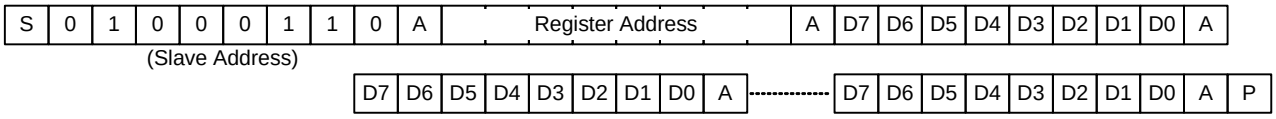

Multiple I²C Register Read Protocol

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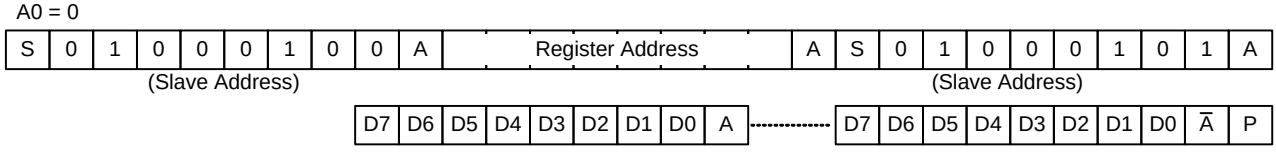
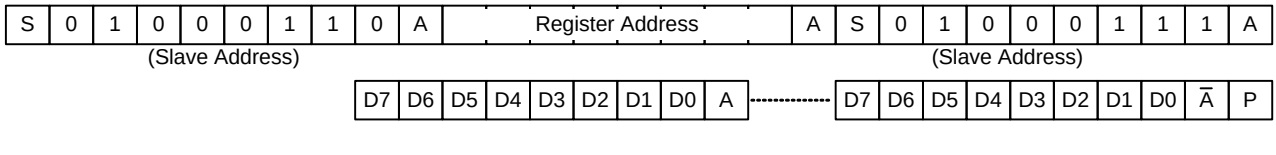


A0 = 1



Note 5. I²C Register Data Address is 0100010x(A0=0) or 0100011x(A0=1).

Note 6. ASG Error Detect Register/EEPROM Address is 0100100x(A0=0) or 0110100x(A0=1).

Note 7. Fault Analysis & Monitoring Registor is 0101010x(A0=0) or 0101011x(A0=1).

Register Map

Address	Name	Description	Default Value	Resolution	Range	00h Function
00h	VON (Bank1)	[7:0] VON_NT_Bank 1	31V (9Ah)	0.2V	15V to 45V, (4Ah to E0h)	VON Shutdown
01h	VOFF (Bank1)	[7:0] VOFF_NT_Bank 1	-12V (3Bh)	0.2V	-5V to -27V, (18h to 86h)	VOFF Shutdown
02h	VSS (Bank1)	[7:0] VSS_Bank 1	-7.6V (25h)	0.2V	-4V to -25V, (13h to 7Ch)	VSS Shutdown
03h	VON (Bank2)	[7:0] VON_NT_Bank 2	31V (9Ah)	0.2V	15V to 45V, (4Ah to E0h)	VON Shutdown
04h	VOFF (Bank2)	[7:0] VOFF_NT_Bank2	-12V (3Bh)	0.2V	-5V to -27V, (18h to 86h)	VOFF Shutdown
05h	VSS (Bank2)	[7:0] VSS_Bank2	-7.6V (25h)	0.2V	-4V to -25V, (13h to 7Ch)	VSS Shutdown
06h	VON Temp. Compensation (Low Temp)	[7:0] VON_LT	35V (AEh)	0.2V	15V to 45V, (4Ah to E0h)	VON Shutdown
07h	VOFF Temp. Compensation (Low Temp)	[7:0] VOFF_LT	-20V (63h)	0.2V	-5V to -27V, (18h to 86h)	VOFF Shutdown
08h	VSS - VOFF	[7:2] ΔV	00h	0.2V	00h : Function OFF 01h to 3Fh : 1.6V to 14V	
	CKV OCP Detect Time	[1:0] CKV_OCP_Det Time	1h		00 : 0.85μs 01 : 1.7μs 10 : 3.4μs 11 : 5.95μs	
09h	VSS NTC2 Option	[7] VSS_NTC2	0h		0 : ON 1 : OFF	
	VSS Temp. Compensation (High Temp)	[6:0] VSS_HT	-9V (2Ch)	0.2V	-4V to -25V, (13h to 7Ch)	VSS Shutdown
0Ah	ASG Error Detect Count	[7:4] ASG_Err_Cnt	3h	4(N+1)	(4counts to 64counts) [of the 64 counts window]	
	No Load Detect Count for ASG Error Detect	[3:2] ASG_NoLoad_Cnt	1h	4(N+1)	00 : 4 Counts 01 : 8 Counts 10 : 16 Counts 11 : 32 Counts [of the 32 counts window]	
	ASG Error Output Status ASG Error	[1:0] ASG_Err_Out	3h		00 : Function disable 01 : 31, 10: 63, 11: 127	
0Bh	No Load Detect Option [7]	[7] ASG_NoLoad_Sel	1h		0 : Shutdown 1 : Skip (Don't achieve ASG Error Detect)	
	Status of ASG Error [6]	[6] ASG_Err_Status	0h		0 : Shutdown 1 : Low Frame (Achieve Low frame output)	
	ASG Error Data Change (Only EEPROM) [5]	[5] ASG_Err_Data	0h		0 : No Change 1 : Change	
	No Load Detect Level	[4:3] ASG_NL_Level	1h		00 : Function Disable (Ignore level for 32frame) 01 : 4V 10 : 8V 11 : 10V	
	ASG Error Detect Level	[2:0] ASG_Err_Level	5h	8	000 : Function Disable 001 to 111 : VON*1/8 to VON*7/8	

Address	Name	Description	Default Value	Resolution	Range	00h Function
0Ch	Aging Mode Option	[7] Aging_Mode_Sel	1h		0 : Apply NTC2 1 : Bank2(Don't apply NTC2)	
	CKV OCP Detect Count	[6:5] CKV_OC_Cnt	1h		00 : 4 Counts 01 : 8 Counts 10 : 16 Counts 11 : 32 Counts	
	CKV OCP Level	[4:1] CKV_OC_Level	0h	20mA	0000 : Function Disable 0001 to 1111 : 20mA to 300mA	
	Applied Point for VON Detect Count	[0] VON_Det_Cnt_Sel	0h		0 : at Initial OLP 1 : at OLP 95%	
0Dh	VON OCP Level	[7:5] VON_OCP_Level	3h	0.25A	Internal MOSFET = 0.5A to 2.25A	
	VON OLP Level	[4:3] VON_OLP_Level	0h	5%	00 : Default (75%) 01 : 80% 10 : 85% 11 : 90%	
	VON OCP Current Detect Count	[2:1] VON_OCP_Cnt	0h	64 Counts	00 : Disable 01 : 64 Counts 10 : 128 Counts 11 : 256 Counts	
	VON Shut-down Time after OLP	[0] VON_SD_Time	1h	1.5ms	0 : 1.5ms 1 : 3ms (Min : 2.5ms, Typ. : 3ms, Max : 3.5ms)	
0Eh	CKV Slew Rate	[7:6] CKV_SR	0h		00 : 1kV/μs 01 : 100V/μs 10 : 50V/μs 11 : 15V/μs	
	RON for GATEP Slew Rate	[5:4] GATEP_SR	0h	2^(N+1)	00 : 10Ω 01 : 20Ω 10 : 40Ω 11 : 80Ω	
	VON FET Switching Slew Rate	[3:2] VON_FET_SR	0h		00 : 100% (Default) 01 : 75% 10 : 50% 11 : 25%	
	VOFF FET Switching Slew Rate	[1:0] VOFF_FET_SR	0h		00 : 100% (Default) 01 : 75% 10 : 50% 11 : 25%	
0Fh	VON Delay Time	[7:4] DLY2	0h	5ms	0ms to 75ms	
	Eagle Delay Time	[3:0] DLY3	0h	5ms	0ms to 75ms	

Address	Name	Description	Default Value	Resolution	Range	00h Function
10h	TSD Option	[7] TSD_Sel	0h		0 : ON 1 : OFF	
	Monitoring Low Frame Setting	[6:5] Monit_LF_Set	2h		00 : Function OFF (Include Fault) 01 : 8Frame 10 : 32Frame 11 : 128Frame	
	NTC Option	[4] NTC	0h		0 : VON 1 : VOFF	
	Initial frequency	[3:2] Init_Freq	2h	150kHz	00 : 450kHz 01 : 600kHz 10 : 750kHz (Default) 11 : 900kHz	
	VOFF Frequency Select	[1:0] VOFF_Freq_Sel	0h		00 : Initial Frequency 01 : X2 10 : X3 11 : X3	
11h	VON Diode Option	[7] VON_Diode_Sel	0h		0 : Intermal 1 : External	
	VON FET Option	[6] VON _FET_Sel	0h		0 : Intermal 1 : External	
	VOFF Diode Option	[5] VOFF_Diode_Sel	0h		0 : Intermal 1 : External	
	VSS Discharge Option	[4] VSS_Disch_Sel	1h		0 : Disable 1 : Enable	
	Transient Time for Bank Select	[3:1] Bank_Sel Transient Time_VON, VOFF, VSS	0h	1.5ms	000 : Disable 001 to 111 : 1ms to 10ms	
	Start-up Enable	[0] Start-up Enable	1h		0 : Standby 1 : Enable	

Fault Analysis & Monitoring

Address	Name	Description	Default Value	Resolution	Range
00h	Die Temperature	[7:4] Die_Temp		5°C	75°C to 150°C
	ASG Error Count	[3:0] ASG_Err_Cnt		4 Count	4 count to 64count
01h	VON Voltage	[7:4] VON		2V	13V to 43V
02h	Analog EN	[6] Analog_EN			0 : Normal 1 : Error
	I2C	[5] I2C			0 : Normal 1 : Error
	Wrong Data	[4] Wrong Data			0 : Normal 1 : Error
	No-load	[2] No_Load			0 : Normal 1 : Error
	ASG Error	[1] ASG_Err			0 : Normal 1 : Error
	CKV OCP	[0]CKV_OCP			0 : Normal 1 : Error
03h	VON OVP	[6] VON_OVP			0 : Normal 1 : Error
	VON OLP	[5] VON_OLP			0 : Normal 1 : Error
	VOFF OVP	[4] VOFF_ OVP			0 : Normal 1 : Error
	VOFF OLP	[3] VOFF_OLP			0 : Normal 1 : Error
	VSS OLP	[2] VSS_OLP			0 : Normal 1 : Error
	VON-VOFF	[1] VON-VOFF			0 : Normal 1 : Error
	TSD	[0] TSD			0 : Normal 1 : Error

Fault Type	Fault Judgment
I^2C Error	When the I^2C enable signal is not detected in 10 seconds(typ.) after releasing VIN UVLO
Analog EN (Masking “Low” during the operation)	When the TRDY signal from T-con is not detected in 10 seconds(typ.) after completion of I^2C communication.
Wrong DATA	When any register data is out of range
OVP	When any output voltage is over the OVP detect level 10 times (When STV signal starts , the OVP function resets the OVP level count)
OLP	When the IC is latched in shut-down condition due to the SCP
TSD	When the IC falls to TSD condition irrespective of TSD on/off option.
CKV OCP	When all outputs are latched in shut-down condition due to the CKV OCP irrespective of CKV OCP option
VON-VOFF	When the different voltage between VON(2D/3D) and VOFF(2D/3D) becomes higher than 60V 10times (When STV signal starts, the subtract function resets the count)
No-load	When the IC detects the no-load status in case of shut-down option only.
ASG Error	When the IC falls to ASG Error condition irrespective of ASG option

Monitoring Data

Code	Die Temp. (°C)	ASG Error Count (Times)	VON Voltage (V)
0000	70 to 75	01 to 04	0 to 13
0001	75 to 80	05 to 08	13 to 15
0010	80 to 85	09 to 12	15 to 17
0011	85 to 90	13 to 16	17 to 19
0100	90 to 95	17 to 20	19 to 21
0101	95 to 100	21 to 24	21 to 23
0110	100 to 105	25 to 28	23 to 25
0111	105 to 110	29 to 32	25 to 27
1000	110 to 115	33 to 36	27 to 29
1001	115 to 120	37 to 40	29 to 31
1010	120 to 125	41 to 44	31 to 33
1011	125 to 130	45 to 48	33 to 35
1100	130 to 135	49 to 52	35 to 37
1101	135 to 140	53 to 56	37 to 39
1110	140 to 145	57 to 60	39 to 41
1111	145 to 150	61 to 64	41 to 43

Application Information

The RT6936 is a multi-functional power solution for LCD panels. The RT6936 contains a negative regulator VSS and a triple high-voltage scan driver to drive an ASG (Amorphous Silicon Gate) circuit on TFT glass for GIP panels. Moreover, a Boost converter and a negative Buck-Boost regulator with temperature compensation are also included to provide adjustable regulated VON and VOFF to generate gate high and gate low voltages. Two converters are both operate with selectable switching frequency by setting I^{2}C register 10h[3:2] and 10h[1:0].

VON Boost Converter

The non-synchronous Boost converter generates high level voltage to the level shifter. The Boost circuit be used the external MOS. The converter's temperature compensation feature allows for different VON level at a certain temperature range.

VON Boost Soft-Start

The VON Boost converter has an internal soft-start to reduce the input inrush current. When the converter is enabled, the output voltage rises slowly from VIN to VON. The soft-start time is around 5ms.

VON Boost Output Voltage Setting

The output voltage can be achieved by setting the I^{2}C Register 00h and Register 03h. The VON setting is from 15V to 45V when Register 00h and Register 03h data from 4Ah to E0h. Refer to Register Map and Output Code Table. The output voltage can be disabled by I^{2}C register 00h / 03h data setting 00h. If V_{ON} setting is over E0h or under 4Ah, IC will shut down.

VON Boost Over-Voltage Protection

In case, VON pin is above 47.5V (typ.), the converter turns the MOSFET switch off. As soon as the output voltage falls below the over voltage threshold, the converter resumes operation.

VON Boost Over-Current Protection

The RT6936 can limit the peak current to achieve over current protection. The IC senses the inductor current that is flowing into the LXP/CSP pin during an ON period. The external or internal N-MOSFET will be turned off if the peak inductor current reaches 2.8A (typ.). The OCP can be achieved by setting the I^{2}C Register address is 0Dh and VON_OCP 0Dh[7:5] control OCP level from 0.5A to 2.25A with setting internal N-MOSFET. When setting external N-MOSFET, VON OCP 0Dh[7:5] control OCP sense voltage level from 0.05V to 0.225V.

VON Boost Over-Current Protection

As shown in Figure 15 and Figure 16.When OCP occurred, IC will latch in shutdown. The OLP level of VON is controllable by setting I^{2}C Register 0Dh [4:3]. VON have only two shutdown time (1.5ms or 3ms) after OLP and controlled by setting I^{2}C Register 0Dh [0].

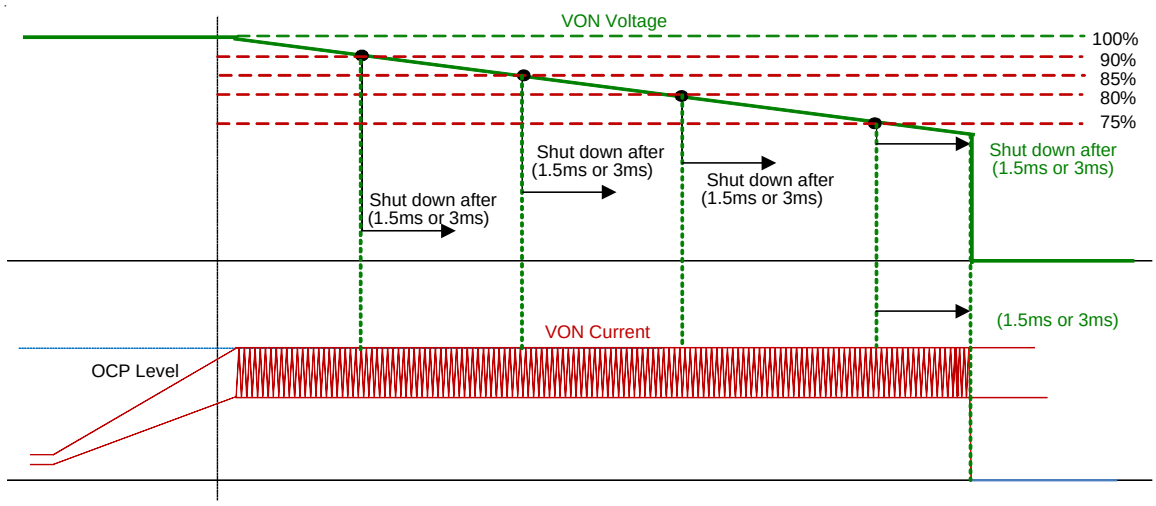


Figure 15. VON OLP Setting Level after OCP Occurred

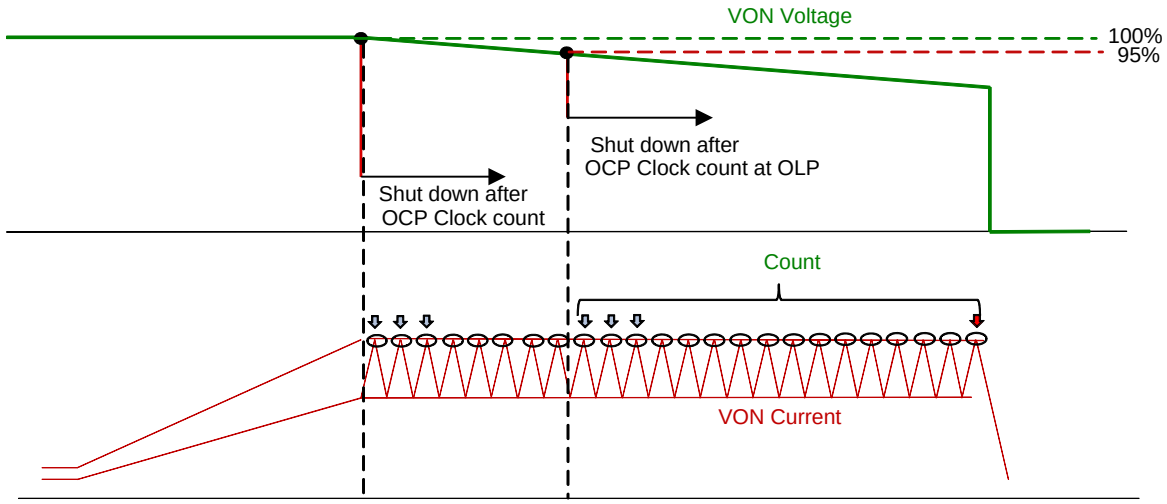


Figure 16. Applied Point for VON Detect Count

VON Temperature Compensation

The VON output voltage is temperature compensated by setting I²C Register 10h bit [4] = 0 and fully adjustable from VON_NT to VON_LT by setting I²C Register 00h (Bank1)/03h (Bank2) and Register 06h. The external resistive between pins NTC and GND allows programming voltage of different temperature. The thermal compensation function block and curve are shown in Figure 17 and Figure 18.

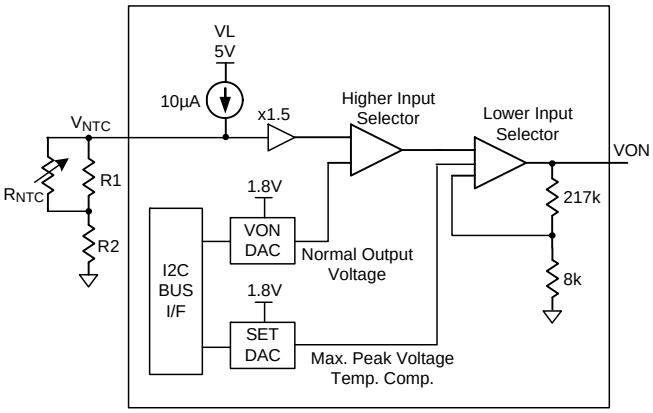


Figure 17 . VON Temperature Compensation Function Block

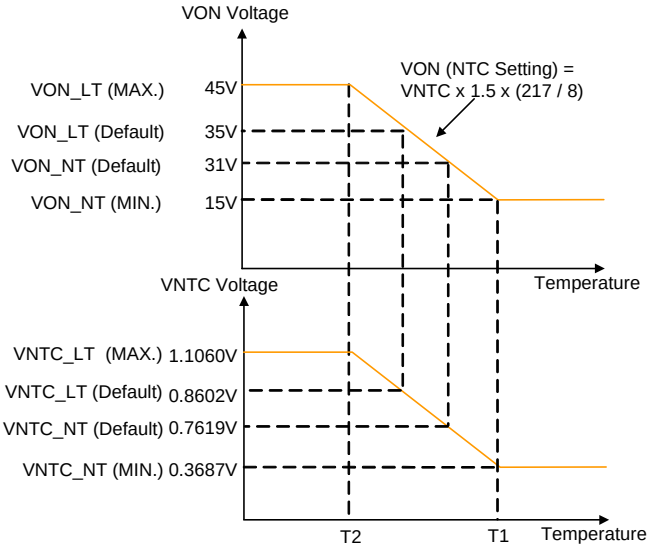


Figure 18. VON Temperature Compensation Curve

$V_{NTC} = I_{NTC} \times [(R_{NTC} // R1) + R2]$

Where I_{NTC} is the reference current and the typical value is 10μA. The V_{ON} voltage can be set as the following equation.

If the $V_{NTC} < V_{ON\_NT(Default)} \times \left(\frac{8}{217}\right) \div 1.5$, $V_{ON} = V_{ON\_NT}$

If the $V_{NTC} > V_{ON\_LT(Default)} \times \left(\frac{8}{217}\right) \div 1.5$, $V_{ON} = V_{ON\_LT}$

Comparators should have the hysteresis function at boundary Region A and B. As shown in Figure 19. (The noise of V_{NTC} is possible to occur the oscillation at the boundary region)

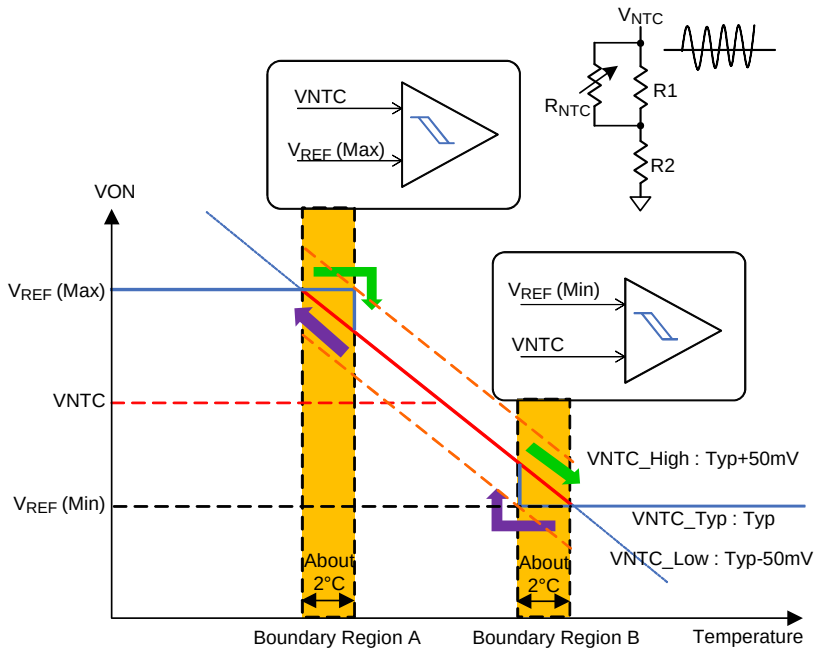


Figure 19. VON Temperature Compensation Hysteresis

Boost Inductor Selection

The inductor value depends on the maximum input current. As a general rule the inductor ripple current is 20% to 40% of maximum input current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equation :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN}}$$

$$I_{RIPPLE} = 0.4 \times I_{IN(MAX)}$$

Wher η is the efficiency of the Boost converter, $I_{IN(MAX)}$ is the maximum input current and I_{RIPPLE} is the inductor ripple current. The input peak current can be obtained by adding the maximum input current with half of the inductor ripple current as shown in the following equation :

$I_{PEAK} = 1.2 \times I_{IN(MAX)}$

Note that the saturated current of inductor must be greater than I_{PEAK}. The inductance can eventually be determined according to the following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT(MAX)} \times f_{OSC}}$$

where f_{OSC} is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

Boost Diode Selection

Schottky diode is a good choice for an asynchronous Boost converter due to its small forward voltage. However, when it selects Schottky diodes, important parameters such as power dissipation, reverse voltage rating and pulsating peak current should all be taken into

consideration. For better performance, it is recommended to choose a suitable diode with reverse voltage rating greater than the maximum output voltage and its average current rating must exceed the average output current.

Boost Input Capacitor Selection

Low ESR ceramic capacitors are recommended for input capacitor applications. Low ESR will effectively reduce the input ripple voltage caused by the switching operation. 4.7µF x 2 low ESR ceramic capacitors are sufficient for most applications. Nevertheless, this value can be decreased for applications with lower output current requirement. Another consideration is the voltage rating of the input capacitor, which must be greater than the maximum input voltage.

Boost Output Capacitor Selection

Output ripple voltage is an important index for estimating the performance. This portion consists of two parts, one is the product of I_{IN} and ESR of output capacitor, another part is formed by charging and discharging process of output capacitor. As shown in Figure 20, ΔV_{OUT1} can be evaluated based on the ideal energy equalization. According to the definition of Q, the Q value can be calculated as the following equation :

$$Q = \frac{1}{2} \times \left[\left(I_{IN} + \frac{1}{2} \Delta I_L - I_{OUT} \right) + \left(I_{IN} - \frac{1}{2} \Delta I_L - I_{OUT} \right) \right] \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f_{OSC}} = C_{OUT} \times \Delta V_{OUT1}$$

where f_{OSC} is the switching frequency and the ΔI_L is the inductor ripple current. Move C_{OUT} to the left side to estimate the value of V_{OUT1} as the following equation :

$$\Delta V_{OUT1} = \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

Finally, the output ripple voltage can be determined as the following equation :

$$\Delta V_{OUT} = I_{IN} \times ESR + \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

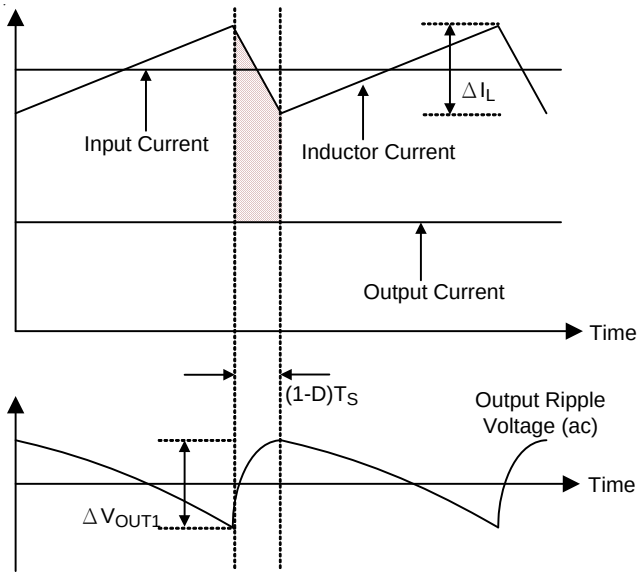


Figure 20. The Output Ripple Voltage without the Contribution of ESR

Over-Temperature Protection

The RT6936 equips an Over Temperature Protection (OTP) to prevent the excessive power dissipation from overheating. The OTP will shut down switching operation while junction temperature exceeds 165°C. Main converter starts switching while junction temperature is cooled by approximately 20°C. Prevent the maximum junction temperature over around 125°C to maintain the continuous operation.

Negative VOFF Buck-Boost Converter Soft-Start

The Buck-Boost converter has an internal soft-start to reduce the input inrush current. When the converter is enabled, the output voltage falls slowly from zero to VOFF. The maximum soft-start time is around 3ms.

VOFF Buck-Boost Output Voltage Setting

The output voltage can be achieved by setting the I^2C Register 01h / 04h. The VOFF setting is from –5V to –27V when Register 01h or 04h data from 18h to 86h. Refer to Register Map and Output Code Table. The output voltage can be disabled by I^2C Register 01h / 04h / 07h data setting 00h. If VOFF setting is over 86h or under 18h or |VON – VOFF| > 60V, IC will shut down.

1. Converter Duty Cycle :

$$D = \frac{-V_{OUT}}{V_{IN} \times \eta - V_{OUT}}$$

2. Maximum output current :

$$I_{OUT} = \left(I_{LPEAK} - \frac{V_{IN} \times D}{2fs \times L} \right) \times (1 - D)$$

3. Peak switch current :

$$I_{LPEAK} = \frac{I_{OUT}}{1 - D} + \frac{V_{IN} \times D}{2fs \times L}$$

VOFF Buck-Boost Inductor Selection

The Buck-Boost converter is able to operate with 10µH to 47µH inductors, but a 22µH inductor is typical. The main parameter for inductor selection is the saturation current of the inductor which should be higher than the peak switch current as calculated in the Design Procedure section with additional margin to cover for heavy load transients. Another important parameter is the inductor DC resistance. Usually, lower DC resistance has higher efficiency. The type and core material of the inductor influence the efficiency as well.

VOFF Buck-Boost Diode Selection

To achieve high efficiency, a Schottky diode should be used. The reverse voltage rating should be higher than the maximum output voltage of the Buck-Boost converter. The average rectified forward current, I_{AVG}, the Schottky diode needs to be rated for, is equal to the output current, I_{OUT}.

$P_D = I_{AVG} \times V_{FORWARD}$

VOFF Buck-Boost Output Capacitor Selection

For the best output voltage filtering, low ESR ceramic capacitors are recommended. One 10µF/X7R or two 4.7µF/X7R output capacitors with sufficient voltage ratings in parallel are adequate for most applications. Additional capacitors can be added to improve load transient regulation.

VOFF Buck-Boost Over-Current Protection

The RT6936 can limit the peak current to achieve over current protection. The IC senses the inductor current that is flowing into the LXN pin during an on period. The internal P-MOSFET will be turned off if the peak inductor current reaches 2.5A (typ.)

VOFF Buck-Boost Over-Voltage Protection

In case of VOFF pin falls below –28.5V(typ.), the converter turns the MOSFET switch off. As soon as the VOFF pin rises higher than the over voltage threshold, the converter will resume operation.

VOFF Buck-Boost Fault Protection

The Buck-Boost converter has a fault protection feature to protect the IC when the output becomes shorted to GND. This is achieved by using the comparator to monitor the VOFF voltage. This function can disable the Buck-Boost converter if VOFF above VOFF x 0.75 and keeps 3ms. The Buck-Boost converter will turn on until power on again.

VOFF Temperature Compensation

There is a thermal compensation feature in the RT6936. Thermal compensation mode can be selected with the control register 10h[4]. If the 10h[4] = 1, VOFF temperature compensation function is enabled. The V_{NTC} voltage can be compensated via external thermal sensing element and resistors, which determine the slope of the compensation. The thermal compensation function block and curves are shown in Figure 21 and Figure 22.

VOFF Temperature Compensation

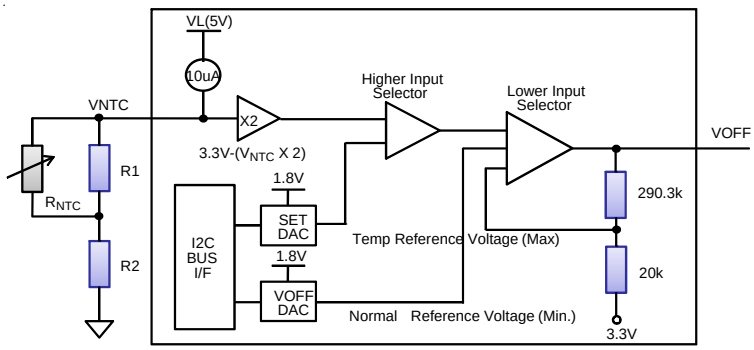


Figure 21 . VOFF Temperature Compensation Function Block

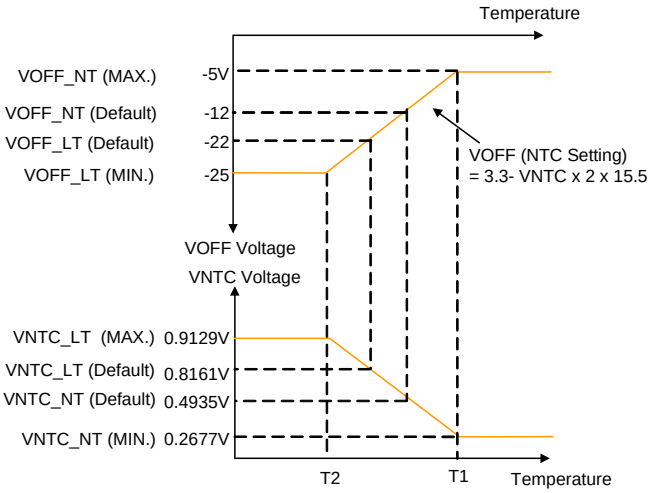


Figure 22. VOFF Temperature Compensation Curves

$V_{NTC} = I_{NTC} \times [(R_{NTC} // R1) + R2]$

Where I_{NTC} is the reference current and the typical value is 10μA. The VOFF voltage can be set as the following equation.

If the $V_{NTC} < 3.3 - V_{OFF\_NT(Default)} \div 2 \div 15.5$,

$V_{OFF} = V_{OFF\_NT}$

If the $V_{NTC} > 3.3 - V_{OFF\_LT(Default)} \div 2 \div 15.5$,

$V_{OFF} = V_{OFF\_LT}$

VSS Regulator Soft-Start

The VSS regulator can provide negative voltage. It has an internal soft-start to reduce the input inrush current. When the regulator is enabled, the output voltage rises slowly from 0V to negative VSS. The typical soft-start time is around 3ms.

VSS Regulator Output Voltage Setting

The output voltage can be achieved by setting the I^2C Register 02h / 05h. The V_{SS} setting is from –4V to –25V when Register 02h / 05h data from 13h to 7Ch. Refer to Register Map and Output Code Table. The output voltage can be disabled by setting I^2C Register 02h / 05h data 00h. If V_{SS} setting is over 7Ch or under 13h, IC will shut down.

VSS Regulator Fault Protection

The VSS regulator has a fault protection. This function can disables the VSS regulator if protect circuit is detected, VSS falls below VSS x 0.75 and keeps 3ms. The VSS regulator will turn on until power on again

VSS Discharge Function

The VSS discharge function can be achieved by setting the I^2C Register address 11h[4]. If the 11h[4] is set high, VSS discharge function is enabled and the switch S1 is turned on and S2 is turned off. Thus, VSSP equals VON. If the 11h bit [4] is set low, the function is disabled. Then S1 is turned off and S2 is turned on. Thus, VSSP equals VSS. As show in Figure 23 and Figure 24.

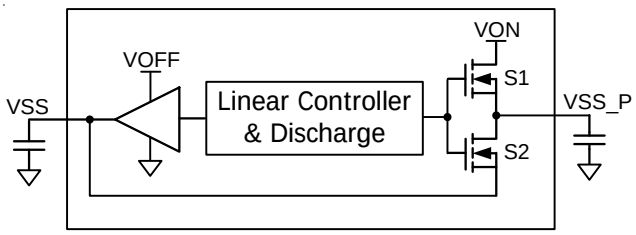


Figure 23 . VSS Discharge Function Block

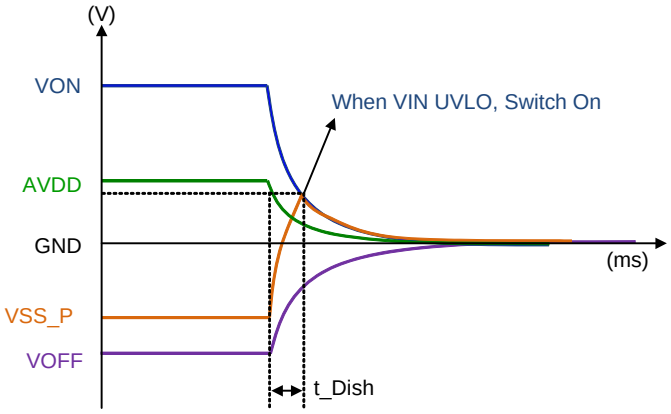


Figure 24. VSS Discharge Function Curve

VSS Temperature Compensation

The VSS thermal compensation mode can be selected with the control register 09h[7]. If the 09h[7] = 0, VSS temperature compensation function is enabled. The VNTC2 voltage can be compensated via external thermal sensing element and resistors, which determine the slope of the compensation. The thermal compensation function block and curve are shown in Figure 25 and Figure 26.

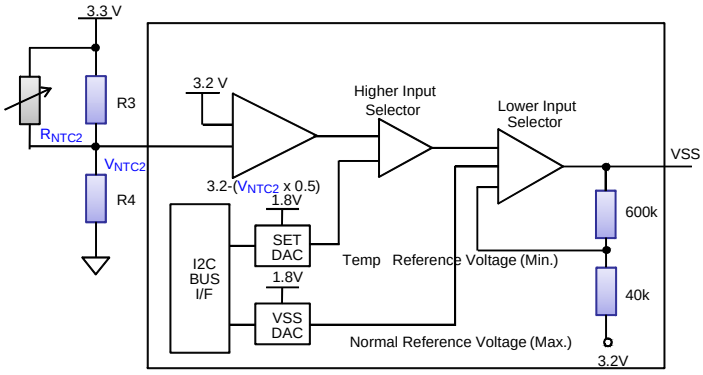


Figure 25 . VSS Temperature Compensation Function Block

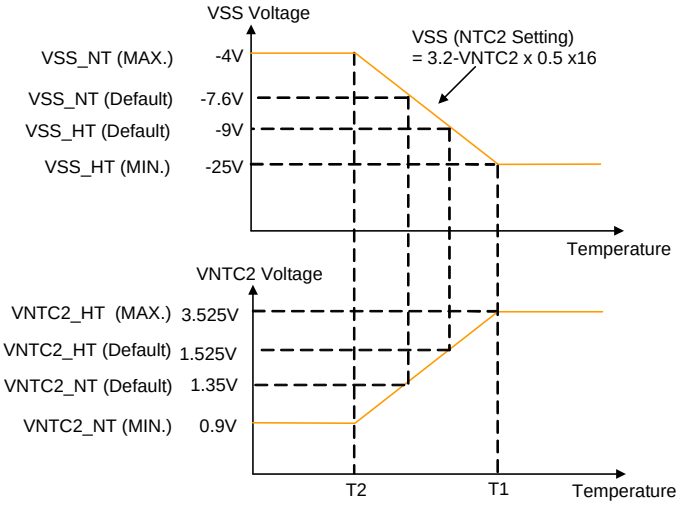


Figure 26. VSS Temperature Compensation Curves

$$V_{NTC2} = 3.3 \times \frac{(R_{NTC2} \ // \ R3)}{(R_{NTC2} \ // \ R3) + R4}$$

Where I_{NTC2} is the reference voltage and the typical value is 3.2V. The V_{ON} voltage can be set as the following equation.

If the

$$V_{NTC2} < (3.2 - V_{SS\_NT(Default)}) \div 0.5 \div 16,\ V_{SS} = V_{SS\_NT}$$

If the

$$V_{NTC2} > (3.2 - V_{SS\_HT(Default)}) \div 0.5 \div 16,\ V_{SS} = V_{SS\_HT}$$

ΔV (VSS-VOFF) Function

VOFF should be variable according to VSS voltage. The variable VOFF voltage should be maintained to ΔV = (VSS – VOFF). If VOFF (= VSS – ΔV) is lower than –27V, VOFF should be clamped to –27V. ΔV Function is disable at VOFF NTC Option and VSS "00" and NTC should be achieved.

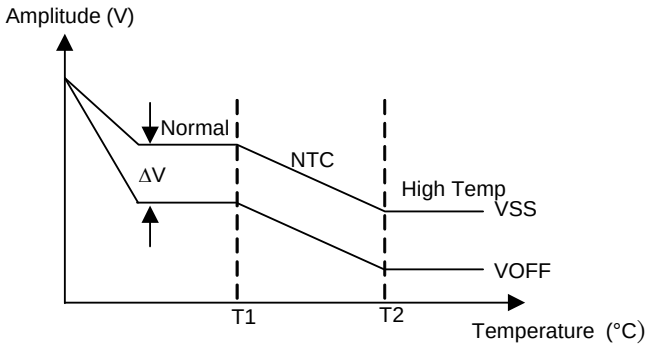


Figure 27. ΔV (VSS – VOFF) Function Curves

Scan Driver Level Shifter

The level shifter which generates high voltage signals for driving the TFT-LCD panel. Each single high-voltage scan driver receives logic-level inputs of CPVx and generates two high-voltage outputs of CKVx, CKVBx. The device receives a logic-level input of STV and generates a high-voltage output of STVP. These outputs are swings from VOFF (–12 V) to VON (31V) and are used to drive the ASG circuit and charge/discharge the capacitive loads of the TFT-LCD. The RT6936 implements a charge share function which could reduce power dissipation.

Scan Driver Under-Voltage-Lockout

The under voltage lockout function ensures that the input voltage is high enough for reliable operation. When VON is smaller than 7.9V, the IC will shut down and all output signals are at high impedance state. At the rising edge of STV, the Scan Driver Output (CKVx/CKVBx) should be reset.

Scan Drive Logic Chart

Table 3. Toggle State is Reset by Rising Edge of STV

Input		Output
STV	CPV1	STVP
Low	Don't Care	Low
High	Low	High
High	High	High Impedance

Input			Output	
STV	CPVx	CKVx	CKVBx	CKVCSx
Low	Low	High Impedance	High Impedance	ON
Low	Rising Edge	Toggle State	Toggle State	OFF
High	Rising Edge	Toggle State	Toggle State	OFF

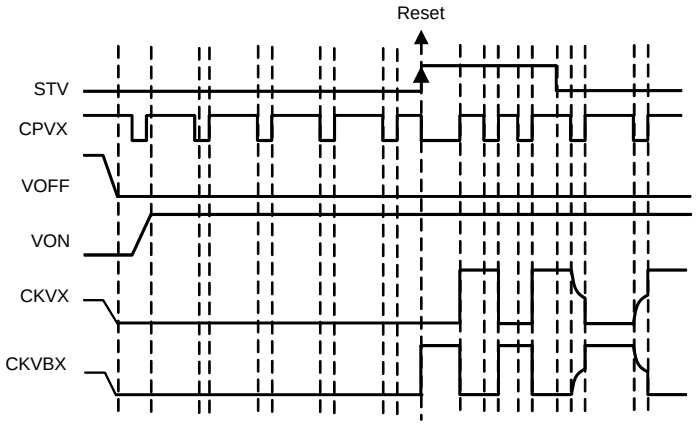


Figure 28. CPVx Edge Overlap to STV (ODD)

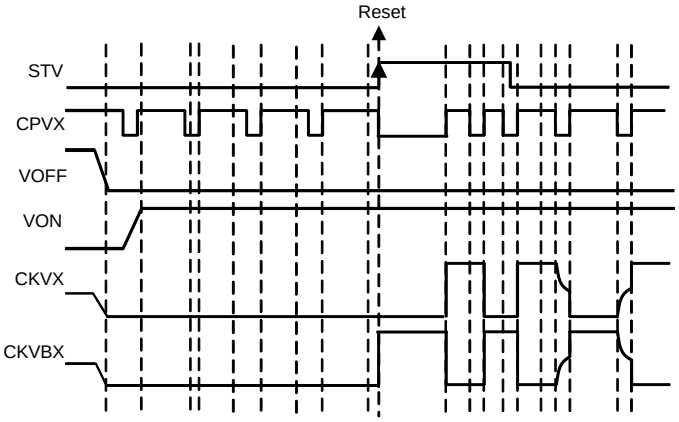


Figure 29. CPVx Edge Overlap to STV (EVEN)

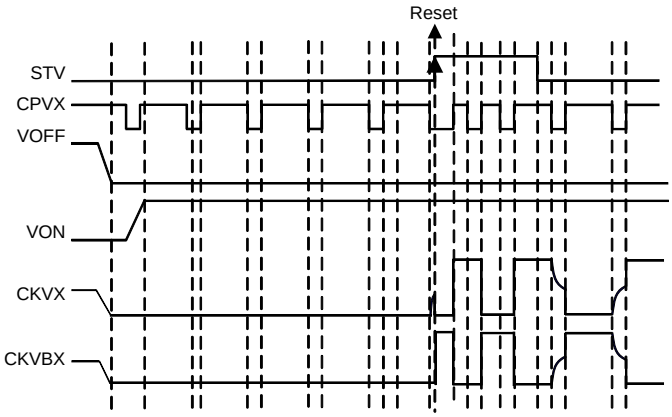


Figure 30. Two CPV inside STV (ODD)

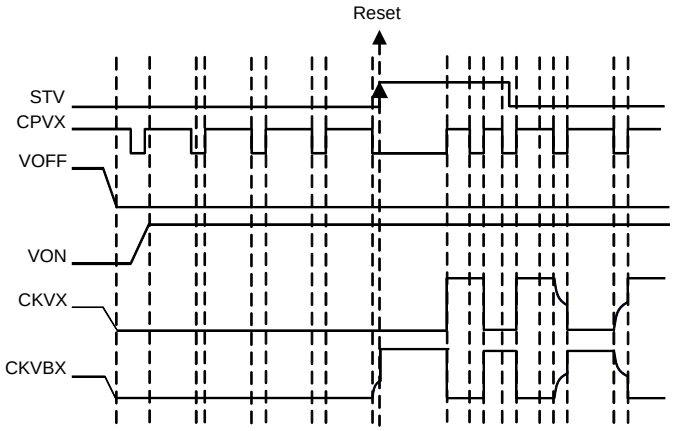


Figure 31. Two CPV inside STV (EVEN)

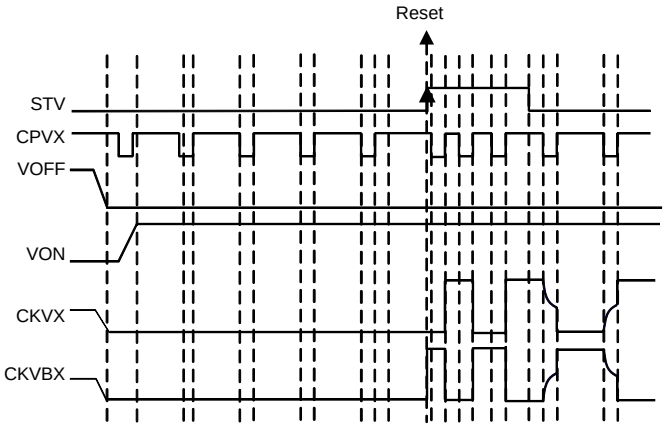


Figure 32. CPVx Edge Overlap and Inside to STV (EVEN)

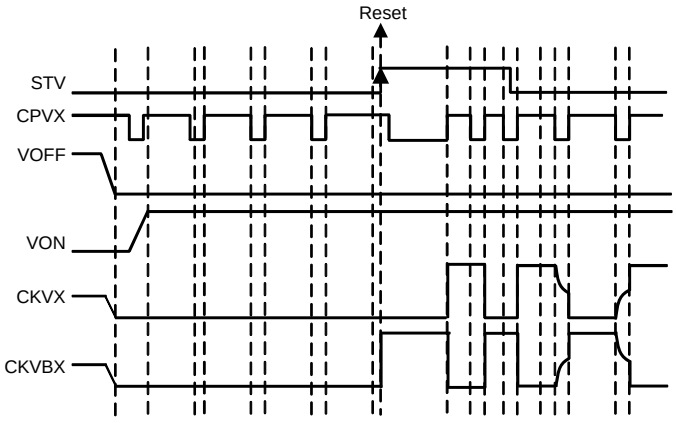


Figure 33. CPVx Edge Overlap and Inside to STV (ODD)

Scan Driver Charge Sharing

CKVCSx is charge share inputs. The function can decrease power loss. When the function is enabled, charge sharing resistors limit the current into the charge share inputs. The larger the value of the charge sharing resistors, the smaller the peak current into the charge share inputs and the gentler the slope of the output charge share waveform.

Scan Driver OCP Function

The Scan Driver OCP function detects the current of each of the CKVx channel OCP level has 8 steps including "Function Disable". When the CKVx level is bigger more than OCP setting level, the level is detected. And detecting count becomes more than setting counter in CPV 32 times, IC becomes shut down. The CKVx OCP detecting time is fixed to 1.7μs and detecting level is adjustable to 20mA to 300mA by setting I^2C Register 0Ch [4:1].

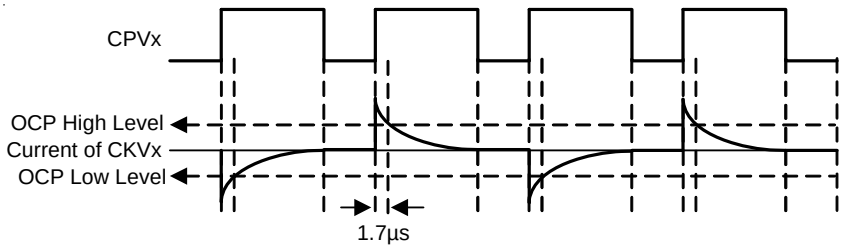


Figure 34. Scan Driver OCP Detection of CKVx

Table 4. SCAN DRIVER OCP Setting Step

0Ch[4:1]	0	1	2	3	4	5	6	7
Timing (Min.)	1.7μs							
Min [mA]	Disable	20	40	60	80	100	120	140

0Ch[4:1]	8	9	A	B	C	D	E	F
Timing (Min.)	1.7μs							
Min [mA]	160	180	200	220	240	260	280	300

Scan Driver OCP Function should count each CPV1, CPV2, CPV3 and CPV4 on the basis of STV. If STV start again before 32 counts finish, Scan Driver OCP Count Block should renew OCP count. OCP level has upper and lower level two kinds. IC should ignore CPV clock during STV pull high, and count again form 1st CPV (rising edge) after STV falling.

RT6936 ties up CKV1/CKVB1, CKV2/CKVB2, CKV3/CKVB3, CKV4/CKVB4 and counts independently. IC recognizes the total event number of CKV1/CKVB1 during counting CPV1. If detected count becomes more than setting count in total 32 times, IC becomes shutdown. In the same way, it counts for each CPV2, CPV3 and CPV4 independently and scan driver OCP detect count by setting I^2C Register 0Ch [6:5].

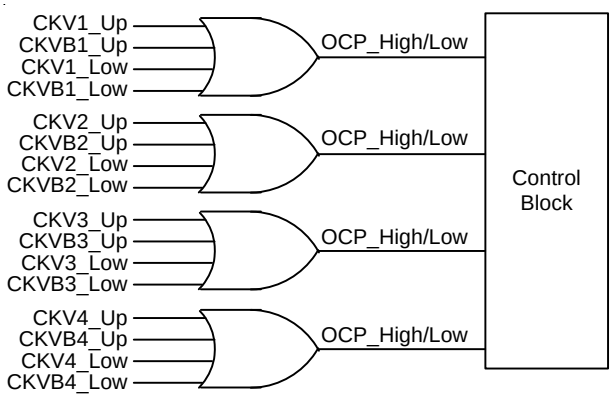


Figure 35. Scan Driver OCP Function Block

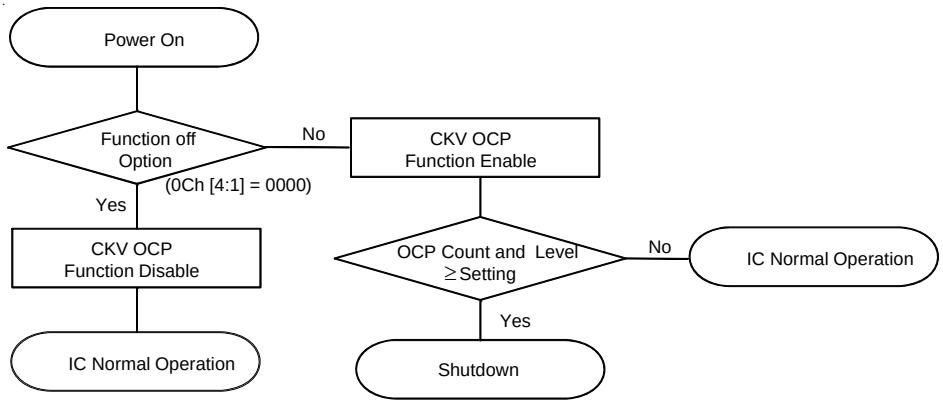


Figure 36. Scan Driver OCP Function Flow Chart

Table 5. Scan Driver OCP Detect Count

0Ch [6:5]	0	1	2	3
Detect Count (Total : 32 Frame)	4	8	16	32

ASG Error Detect Function

For a start, IC counts STV pulse (8 frame) after DLY3 and shown in the Figure 37. If ASG carry signals are GND level over setting count times (Table 6.) during STV 32 frame, IC should mask ASG Error detect function. Therefore, In case of no load, the ASG Error detect function doesn be operated.

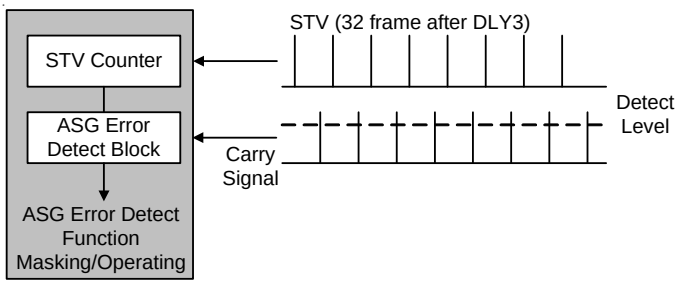


Figure 37. ASG Function Detection

Table 6. No Load Detect Count Setting for ASG Error

0Ah[3:2]	0	1	2	3
Detect Count (Total : 32 Frame)	4	8	16	32

In case that ASG Error detect function operates normally, If ASG carry signals are over setting count times (Table 7.) under setting Detect level (Table 8.) during STV 64 frame, scan driver should output abnormal CKVx waveforms. And, abnormal CKVx's VOFF level frame can be set by Register (Table 9). (ex. 1:31 setting : normal CKV 1frame, VOFF level 31 Frame)

Table 7. ASG Error Detect Count

0Ah[7:4]	0	1	……	14	15
Detect Count (Total : 64 Frame)	4	8	……	60	64

Table 8. ASG Error Detect Level

0Bh[2:0]	0	1	2	3
Min [V]	Function Disable	VON·1/8	VON·2/8	VON·3/8

0Bh[2:0]	4	5	6	7
Min [V]	VON·4/8	VON·5/8	VON·6/8	VON·7/8

Note 7 : Function Disable : ASG Error Detect Function OFF.

Table 9. SCAN DRIVER Output Ratio during ASG Error

0Ah[1:0]	0	1	2	3
Normal Frame : VOFF Level Frame	Function Disable	1:31	1:63	1:127

Note 8 : Function Disable : Normal Scan Driver Output

Fault Function

During normal operating, each fault pin becomes high-state. If the one chip becomes the fault-state, the fault pin becomes low-state. Thus, the fault pin of the other chip becomes also low-state and shut-down. If the RT6929 becomes the fault-state, the RT6936 becomes shut down. If the RT6936 becomes the fault-state, the RT6929 becomes shut down except for logic power. If the resister R removes, the fault pin of the other chip becomes high-state and normal operation. As show in Figure 38.

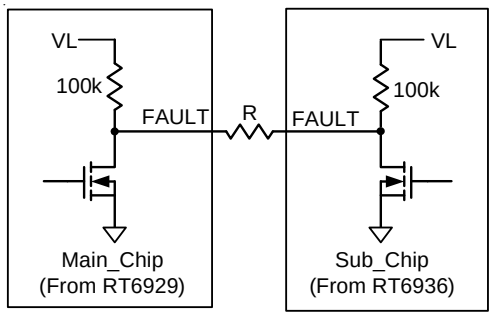


Figure 38. Fault Function Block

Fault and Monitoring Function

The monitoring and update is synchronized by STV. The update point is next frame of setting frame that is controlled by 2 bit by setting I²C Register 10h [6:5]. As shown in Table 10. The update data is the average of monitoring data during the setting frame and should be transferred in max 0.5ms.

Table 10. Data Monitoring & Update Period

10h [6:5]	00	01	10	11
Frame	Function OFF (Include Fault)	8 Frame	32 Frame	128 Frame

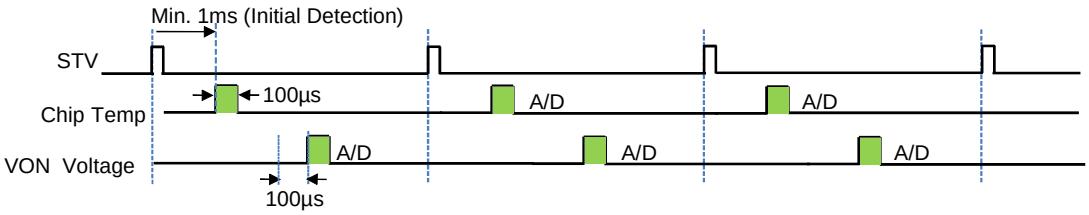


Figure 39. Data Monitoring Sequence

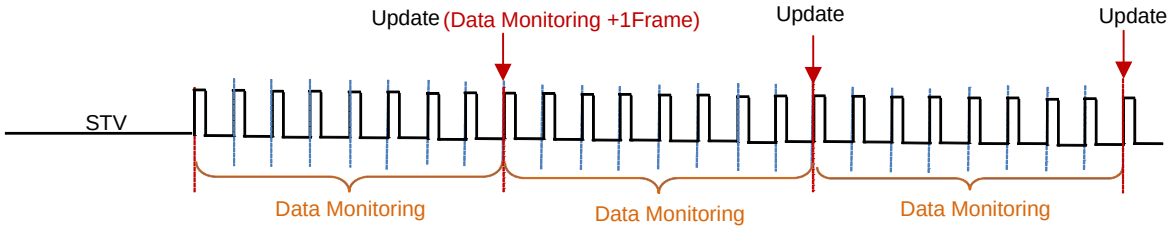


Figure 40. Data Monitoring & Update Period

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-40L 6x6, the thermal resistance, θ_{JA}, is 27.1°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (27.1°C/W) = 3.69W for a WQFN-40L 6x6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 41 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

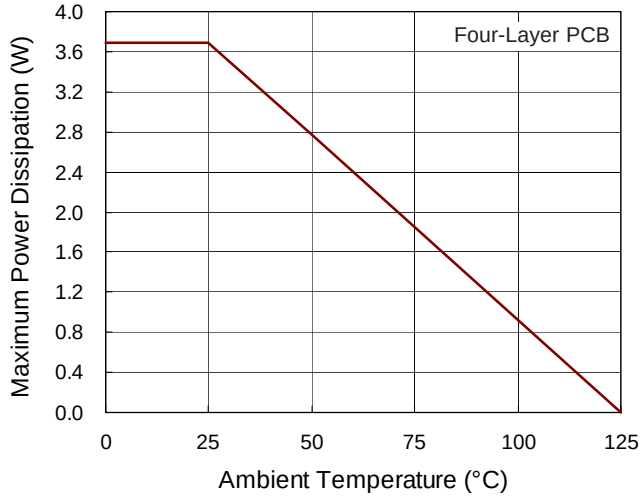


Figure 41. Derating Curve of Maximum Power Dissipation

Layout Consideration

PCB layout is very important for designing power switching converter circuits. For best performance of the RT6936, the following layout guidelines must be followed :

- For good regulation, place the power components as close as possible. The traces should be wider and shorter especially for the high current output loop.
- The output sense voltage must be near the sense pin. The sense voltage pin trace must be short and avoid the trace near any switching nodes.
- Minimize the size of the LXP/CSP and LXN node and keep it wide and shorter. Keep the LX node away from the analog ground.
- The power ground (PGND) consists of input and output capacitor grounds.
- Separate power ground (PGND) and analog ground (AGND). Connect the AGND and the PGND islands at a single end. Make sure that there are no other connections between these separate ground planes. Connect the exposed pad to a strong ground plane for maximum thermal dissipation.

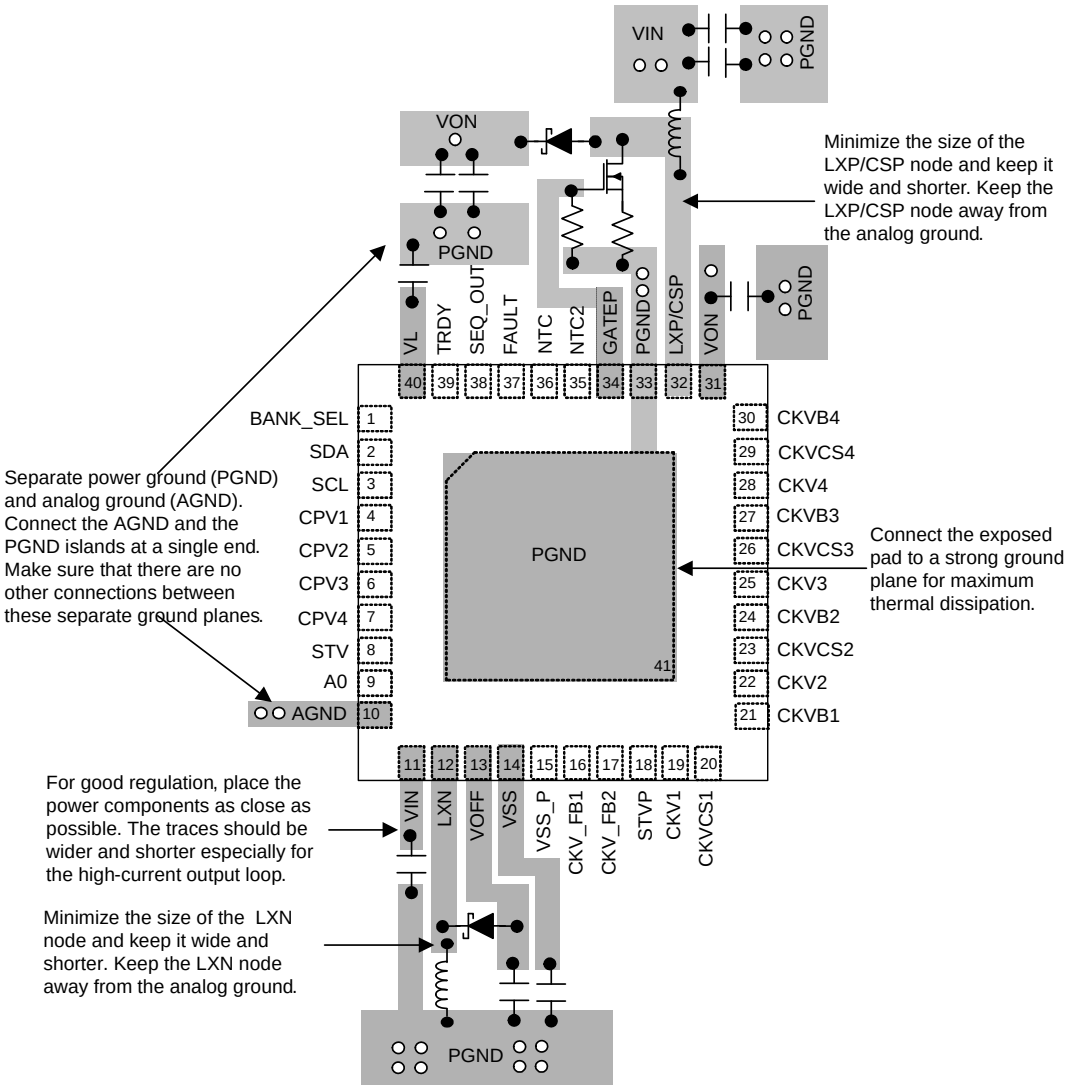
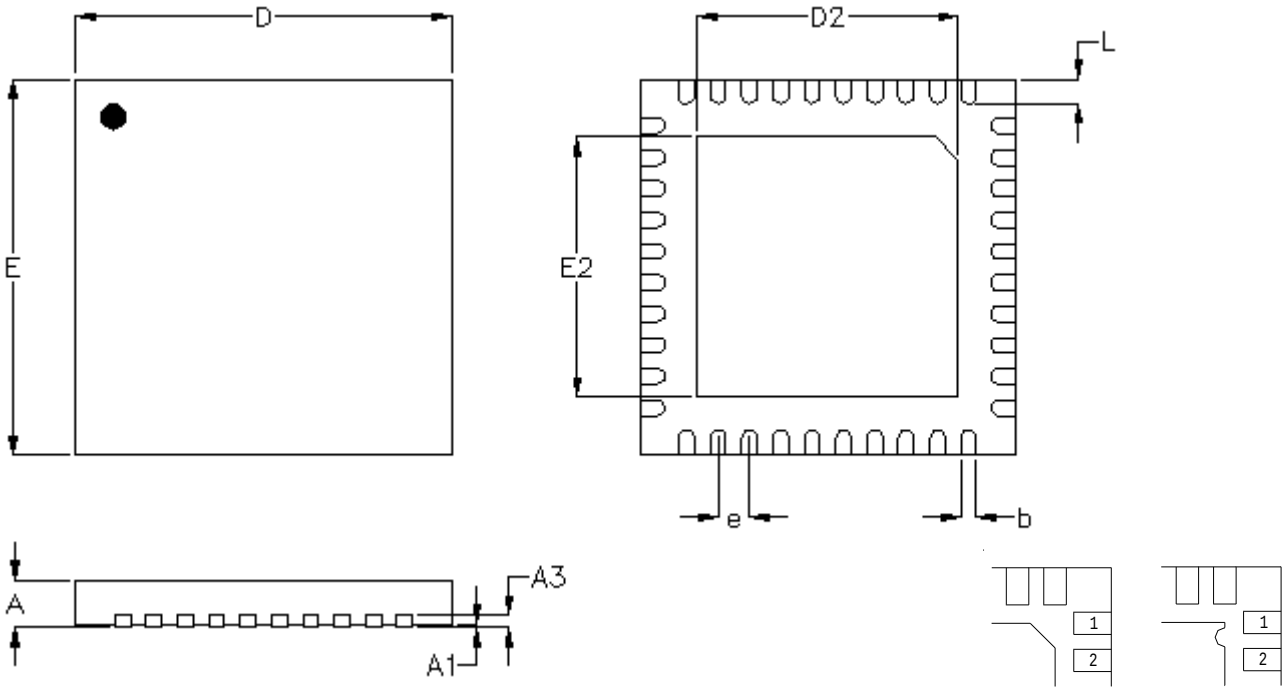


Figure 42. PCB Layout Guide

Outline Dimension



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol		Dimensions In Millimeters			Dimensions In Inches		
		Min.	Typical	Max.	Min.	Typical	Max.
A		0.700	0.750	0.800	0.028	0.030	0.031
A1		0.000	0.020	0.050	0.000	0.001	0.002
A3		0.175	0.203	0.250	0.007	0.008	0.010
b		0.180	0.250	0.300	0.007	0.010	0.012
D		5.950	6.000	6.050	0.234	0.236	0.238
D2	Option1	4.000	4.150	4.750	0.157	0.163	0.187
	Option2	3.470	3.520	3.570	0.137	0.139	0.141
E		5.950	6.000	6.050	0.234	0.236	0.238
E2	Option1	4.000	4.150	4.750	0.157	0.163	0.187
	Option2	2.570	2.620	2.670	0.101	0.103	0.105
e		--	0.500	--	--	0.020	--
L		0.350	0.400	0.450	0.014	0.016	0.018

W-Type 40L QFN 6x6 Package

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