PC Power Supply Supervisor

General Description

R7510A is a supervisor IC especially designed for PC power supplies with 3.3V, 5V and 12V outputs. The R7510A integrates a remote ON/OFF control input (PSONB), noise de-bounce/deglitch circuits, timing-and-fault control logics, an output power good indicator (PGO), an input power good input (PGI) and full output protections which include a fault indicator (FPOB), under voltage and over voltage protections. R7510A minimizes external component count and makes the designs of power supply easier.

As the PSONB receives a valid ON/OFF signal from a PC motherboard, the FPOB voltage goes low to start a power-on process. When the power-on process is completed, all of protections are enabled and the PGO voltage goes high to indicate that the output voltages are all in regulation ranges.

Features

- **VDD Under Voltage Lockout Protection**
- **Output Over Voltage Protections (OVP) for 3.3V, 5V and 12V**
- **Output Under Voltage Protections (UVP) for 3.3V and 5V**
- **Open-Drain Power Good (PGO) and Fault Protection (FPOB) Outputs**
- **300ms Power Good Delay Time**
- **38ms PSONB Remote ON/OFF De-bounce Time**
- **55µs OVP and 73µs UVP Noise Deglitch Times**
- **3.5ms PSONB Turn-off Delay Time**
- **Two-Threshold PGI Input with 73µs Noise Deglitch Time**
- **75ms UVP Blanking Time during Start-up**
- **Low Cost and Component Count**
- **RoHS Compliant and Halogen Free**

Ordering Information

R7510A□□

- Package Type
  N : DIP-8
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

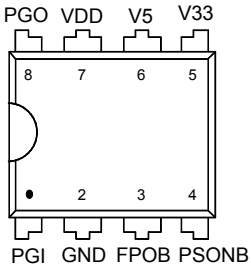
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

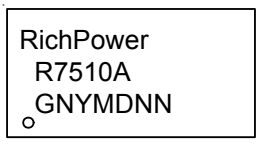
Pin Configuration

(TOP VIEW)



DIP-8

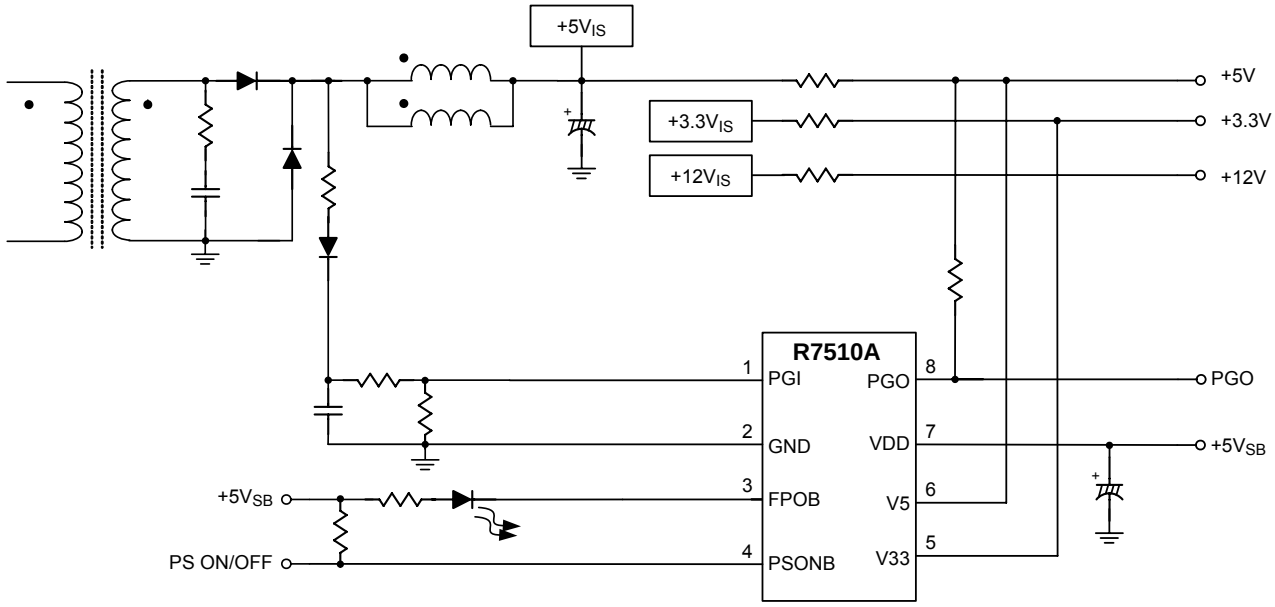
Marking Information



R7510AGN : Product Number

YMDNN : Date Code

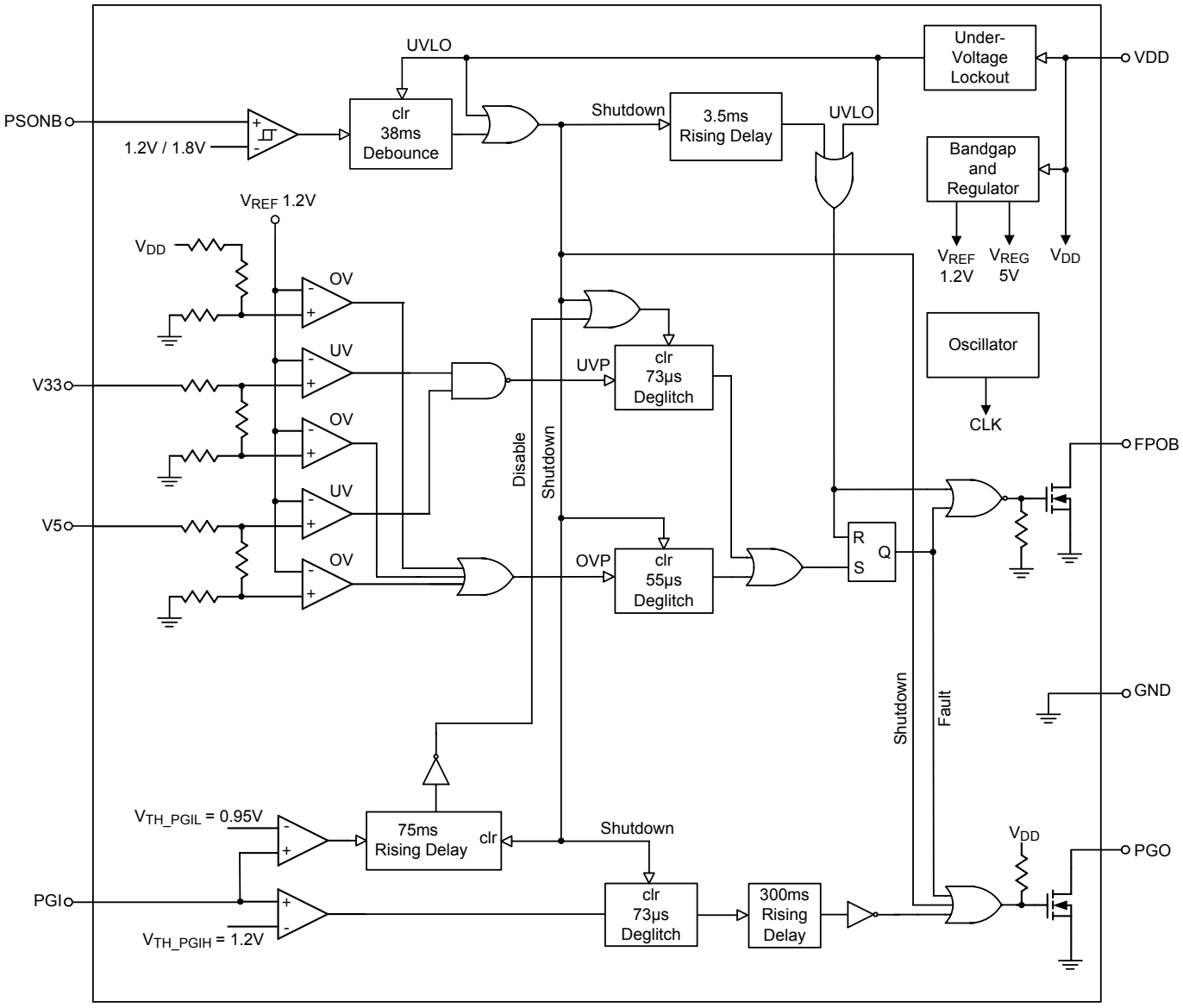
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Description
1	PGI	Power Good Signal Input Pin. This pin senses partial voltage of the system input voltage.
2	GND	Ground Pin of the IC. All voltage levels are measured with respect to this pin. Ties the pin directly to system ground plane with the lowest impedance.
3	FPOB	Fault Protection Output Pin. This pin is pulled low when PSONB = L and no protections happened.
4	PSONB	Remote ON/OFF Control Input Pin. This pin is designed with a 38ms (typical) De-bounce time to avoid input voltage bounce.
5	V33	3.3V OVP and UVP Detection Input Pin.
6	V5	5V OVP and UVP Detection Input Pin.
7	VDD	Supply Voltage and 12V OVP Detection Input Pin. Connect a noise decoupling capacitor between this pin and GND.
8	PGO	Open-Drain Power Good Output Pin. When all output voltages are in their regulation ranges, the PGO voltage goes high.

Functional Block Diagram



Functional Descriptions

VDD Under Voltage Lockout Protection

The R7510A automatically initializes upon receipt of power. The Under Voltage Lockout (UVLO) function continually monitors the bias voltage at VDD pin. When the supply voltage (V_{DD}) exceeds its rising UVLO threshold (3.6V typical), the IC is enabled to work. When the VDD voltage is under the UVLO voltage threshold (UVLO = H), the PGO voltage is pulled low to indicate the output voltages are not ready and the FPOB pin keeps high impedance to disable the primary-side PWM controller. The supply voltage must be below the absolute maximum rating for safety.

Output Under Voltage Protection and PGI Input

The R7510A provides under voltage protection for the 3.3V and 5V outputs. The UVP continuously monitors the voltage on V33 and V5. When an under-voltage (UV) protection condition appears at one of the monitored pins for more than 73μs (typical) deglitch time, the PGO voltage goes low to indicate one of the output voltages is out of regulation. Meanwhile the FPOB also becomes high impedance to disable the primary-side PWM controller and protects the power supply system. The UVP protection condition is latched until PSONB is toggled from low to high or VDD restarts.

The UVP protection can be disabled by the PGI signal. During PSONB start-up or AC power-on, a UVP blanking signal disables the UVP detections to prevent wrong UVP. The blanking time is shown in the following table:

IC	Blanking Time	Start Condition	Stop Condition
R7510A	∞	V_{PGI} < 0.95V	V_{PGI} > 0.95V
	75ms	V_{PGI} > 0.95V	end of 75ms

The UVP protection is disabled when the PGI voltage keeps below the lower PGI voltage threshold 0.95V (typical). After the start-up is completed, the IC enters normal-mode operation. The UVP will be disabled when the PGI voltage falls below the lower voltage threshold 0.95V (typical). This function is designed to keep PWM switching and discharge the high-voltage charge in the bulk capacitors during AC power-off.

Output Over Voltage Protection

The R7510A has an output Over Voltage Protection (OVP) function, which monitors the 3.3V, 5V and 12V output voltages, to prevent power system and loads from damages during one or more output OV condition(s). The OVP starts monitoring the voltages on V33, V5 and VDD at end of the PSONB de-bounce time. When an Over Voltage (OV) condition appears at one of the monitored pins for more than the 55μs (typical) deglitch time, the PGO voltage goes low to indicate one of the output voltages is out of regulation. Meanwhile the FPOB also becomes high impedance to disable the primary-side PWM controller and protects the power supply system. The OVP condition is latched until PSONB is toggled from low to high or VDD restarts.

PSONB De-bounce

R7510A provides a remote ON/OFF control input pin (PSONB) for PC power supply applications. A built-in 38ms (typical) de-bounce circuit performs rising and falling edge noise de-bounce functions to identify valid PSONB input signals. The PSONB also has a TTL logic-compliant input voltage threshold and a hysteresis design against input noise.

FPOB and PGO Outputs

The FPOB and PGO are all open-drain output pins. The PGO voltage, pulled high by an external resistor connected to the 5V output, indicates the status of the outputs. The PGO keeps at low state, when VDD voltage<UVLO threshold, PSONB = H, PGI voltage<1.2V or one of the faults, including UVP and OVP occurs.

In general, the FPOB pin is used to enable the primary-side PWM controller via an opto-coupler. An external series resistor is used to limit the current flowing through the opto-coupler and FPOB pin. The FPOB keeps high impedance, when VDD voltage<UVLO threshold, PSONB = H or one of the faults, including UVP and OVP occurs.

Function Table

Input Signals		Events		Output Signals	
PGI	PSONB	UV Detected	OV Detected	FPOB	PGO
V_{PGI} < 0.95V	L	No	No	L	L
V_{PGI} < 0.95V	L	No	Yes	H	L
V_{PGI} < 0.95V	L	Yes	No	L	L
V_{PGI} < 0.95V	L	Yes	Yes	H	L
V_{PGI} > 0.95V	L	No	Yes	H	L
V_{PGI} > 0.95V	L	Yes	No	H	L
V_{PGI} > 0.95V	L	Yes	Yes	H	L
V_{PGI} > 1.2V	L	No	No	L	H
X	H	X	X	H	L

Note: X = Don't care

FPOB = "L" means fault isn't latched

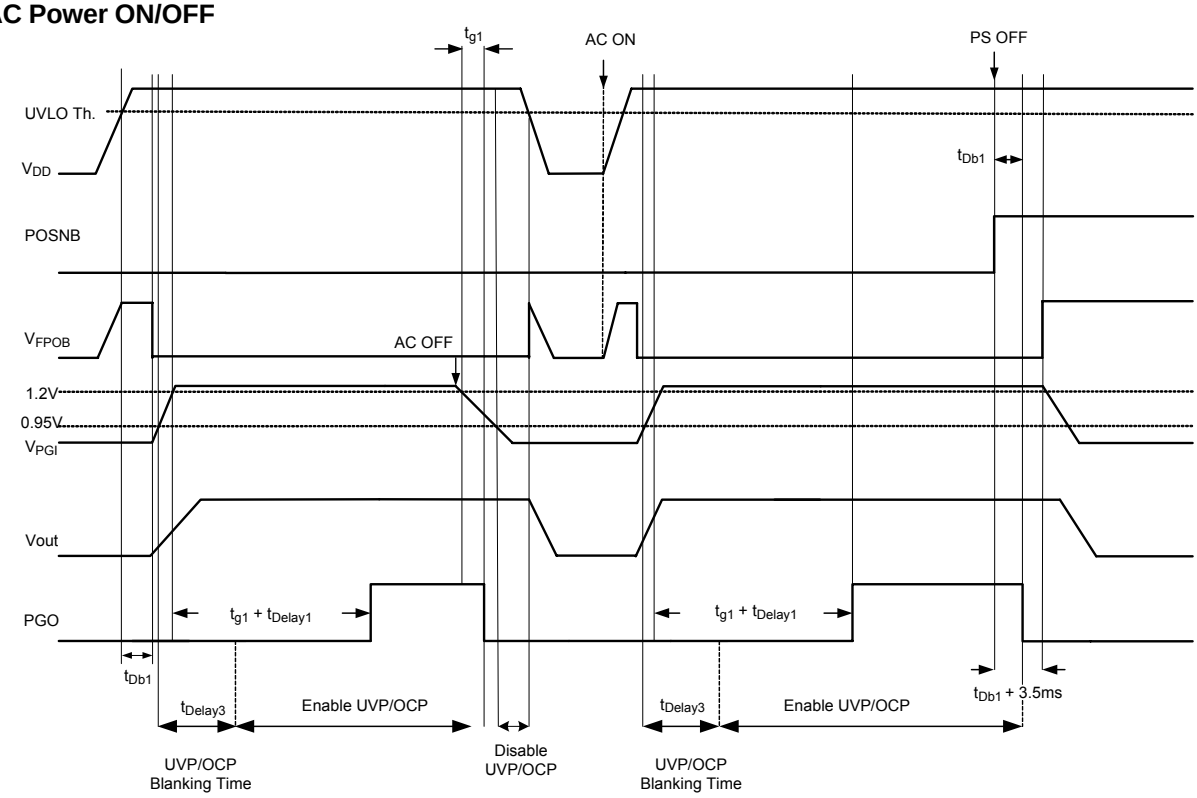
FPOB = "H" means fault is latched

PGO = "L" means fault

PGO = "H" means No fault

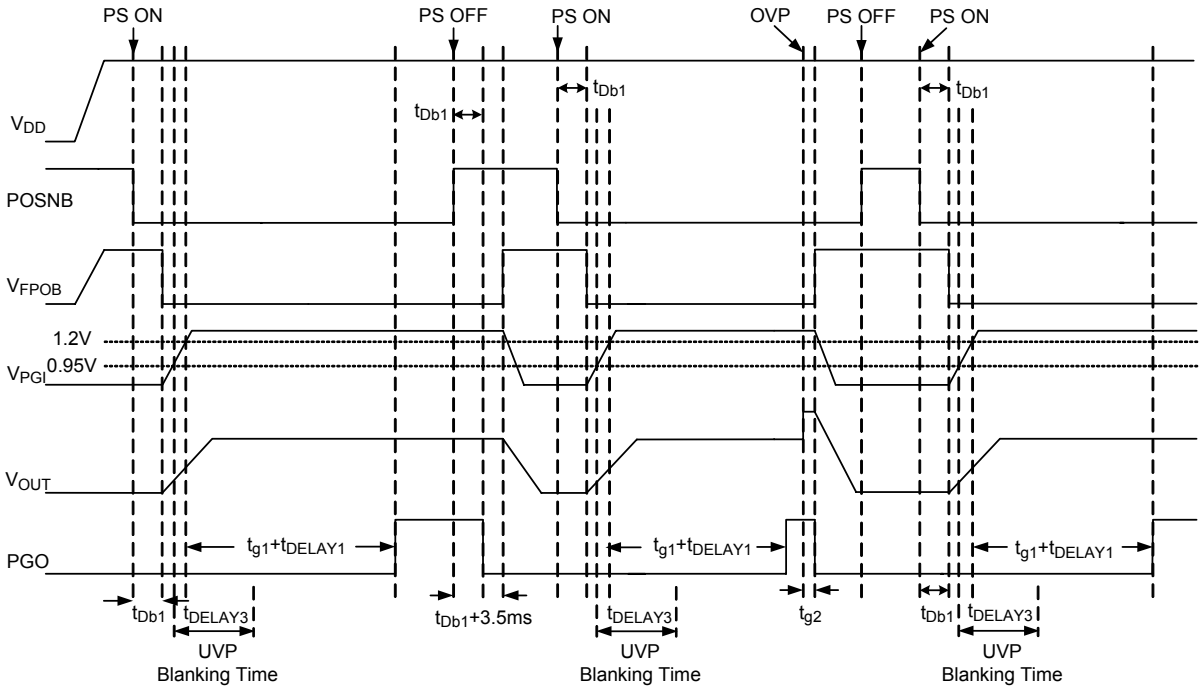
Timing Diagram

(1) AC Power ON/OFF



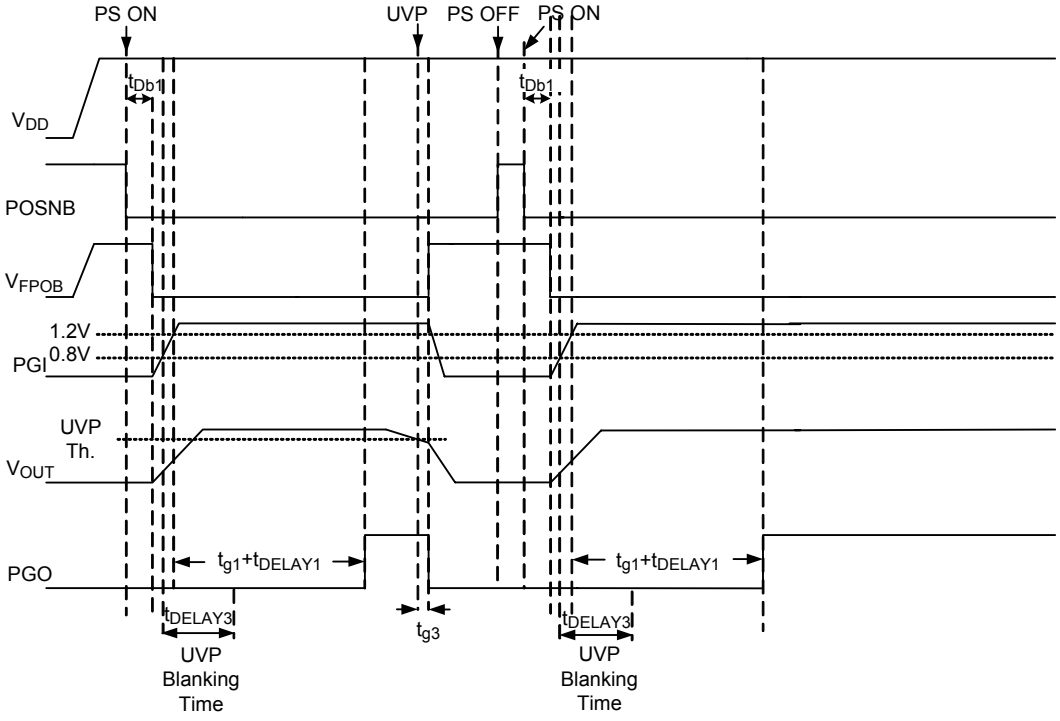
Note : PSONB = L ⟶AC Power-OFF ⟶ AC Power-ON ⟶ PSONB = H.

(2) PS ON/OFF and OVP



Note : PSONB = L ⟶ PSONB = H ⟶ PSONB = L ⟶ OVP Latch ⟶ PSONB = H ⟶ PSONB = L.

(3) UVP



Note : PSONB = L ⟶ UVP Latch⟶ PSONB = H⟶ PSONB = L.

Absolute Maximum Ratings (Note 1)

- VDD Supply Voltage (VDD to GND), V_{DD} ---------- –0.3V to 16V
- PGI, PGO, PSONB, V5, V33 to GND Voltage ---------- –0.3V to 7V
- FPOB to GND Voltage ---------- –0.3V to 16V
- Power Dissipation, P_D @ T_A = 25°C
  DIP-8 ---------- 0.714W
- Package Thermal Resistance (Note 2)
  DIP-8, θ_{JA} ---------- 140°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV

Recommended Operating Conditions (Note 4)

- VDD Supply Voltage Range, V_{DD} ---------- 4V to 15V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Supply Current and Under Voltage Lockout (UVLO)						
VDD Supply Voltage Range	V_{DD}	T_A = –40°C to 85°C	4	--	15	V
VDD Supply Current	I_{DD}	V_{PSONB} = 5V	--	0.5	1	mA
		V_{PSONB} = 0V	--	--	3	mA
Rising UVLO Voltage Threshold	V_{TH_UVLOR}	V_{DD} rising	3.2	3.4	3.6	V
Falling UVLO Voltage Threshold	V_{TH_UVLOF}	V_{DD} falling	2.8	3	3.2	V
Over Voltage Protection Section (OVP)						
V33 Over Voltage Threshold	V_{TH_V33OV}		3.7	3.9	4.1	V
		T_A = –40°C to 85°C	3.66	3.9	4.14	
V5 Over Voltage Threshold	V_{TH_V5OV}		5.7	6.1	6.2	V
		T_A = –40°C to 85°C	5.64	6.1	6.26	
VDD Over Voltage Threshold	V_{TH_V12OV}		12.9	13.4	13.9	V
		T_A = –40°C to 85°C	12.76	13.4	14.04	
Under Voltage Protection (UVP)						
V33 Under Voltage Threshold	V_{TH_V33UV}		2	2.2	2.4	V
		T_A = –40°C to 85°C	1.97	2.2	2.43	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V5 Under Voltage Threshold	V_{TH_V5UV}		3.3	3.5	3.7	V
		T_A = –40°C to 85°C	3.26	3.5	3.74	
V33 Pin Input Resistance			--	150	--	kΩ
V5 Pin Input Resistance			--	300	--	kΩ
PGO and FPOB Outputs						
PGO Leakage Current	I_{LK_PGO}	V_{PGO} = 5V, the internal NMOS is off	--	--	5	μA
PGO Low-level Output Voltage	V_{OL_PGO}	I_{SINK} = 10mA	--	0.23	0.3	V
PGO Rising Time	t_{R_PGO}	Pull-up Resistance = 1kΩ	--	--	100	ns
FPOB Leakage Current	I_{LK_FPOB}	V_{FPOB} = 5V, PSONB = Open	--	--	5	μA
FPOB Low-level Output Voltage	V_{OL_FPOB}	I_{SINK} = 10mA	--	0.2	0.3	V
PGI and PSONB Input						
Higher PGI Voltage Threshold	V_{TH_PGIH}	(Note 5)	1.16	1.2	1.24	V
Lower PGI Voltage Threshold	V_{TH_PGIL}	(Note 6)	0.9	0.95	1	V
PGI Input Current		V_{PGI} = 1.2V	--	--	1	μA
PSONB Input Pull-up Resistor	R_{PU_PSONB}		--	26	--	kΩ
PSONB Input Pull-up Voltage	V_{PU_PSONB}		--	4.5	--	V
PSONB High-level Input Voltage	V_{IH_PSONB}		1.8	--	--	V
PSONB Low-level Input Voltage	V_{IL_PSONB}		--	--	1.2	V
Timing Characteristics						
PSONB De-bounce Time	t_{Db1}		26	38	50	ms
PGI to PGO Deglitch Time	t_{g1}	Rising V_{PGI} > 1.2V	46	73	100	μs
PGI to PGO Delay Time	t_{DELAY1}	Rising V_{PGI} > 1.2V	200	300	400	ms
OVP Deglitch Time	t_{g2}	$V_{V33/V5/VDD}$ rising	35	55	75	μs
UVP Deglitch Time	t_{g3}	$V_{V33/V5/V12}$ falling	46	73	100	μs
PSONB Turn-Off Delay Time	t_{DELAY2}	from PSONB goes low to FPOB goes high	2 + t_{Db1}	3.5 + t_{Db1}	5 + t_{Db1}	ms
UVP Power-On Blanking Time	t_{DELAY3}	V_{PGI} < 0.95V	Disable			
		V_{PGI} > 0.95V	50	75	100	ms

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

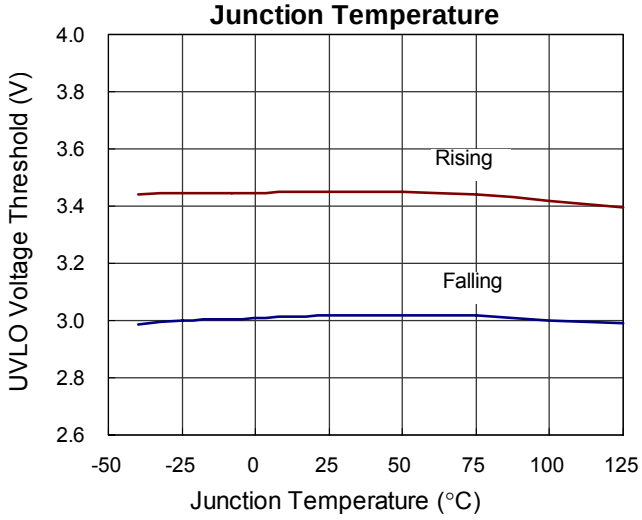
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. The PGO is allowed to indicate the output statuses when PGI voltage rises above this voltage threshold; otherwise the PGO is held at low state.

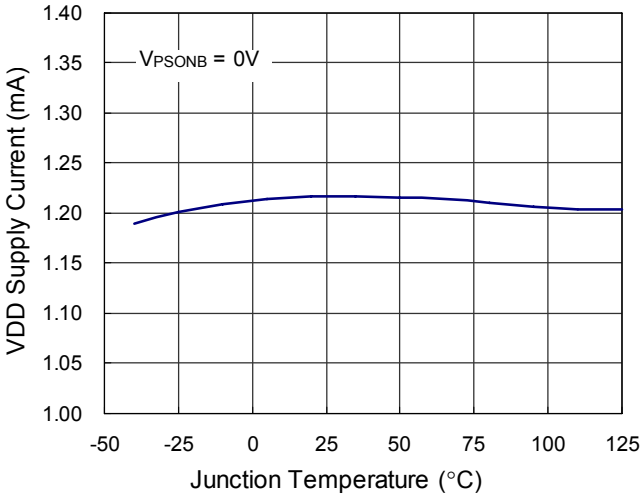
Note 6. This voltage threshold is used to start the UVP blanking time (75ms, when V_{PGI} > 0.95V) and then enable the UVP during power-on. During normal operation, if the PGI voltage is below the threshold, the UVP is disabled.

Typical Operating Characteristics

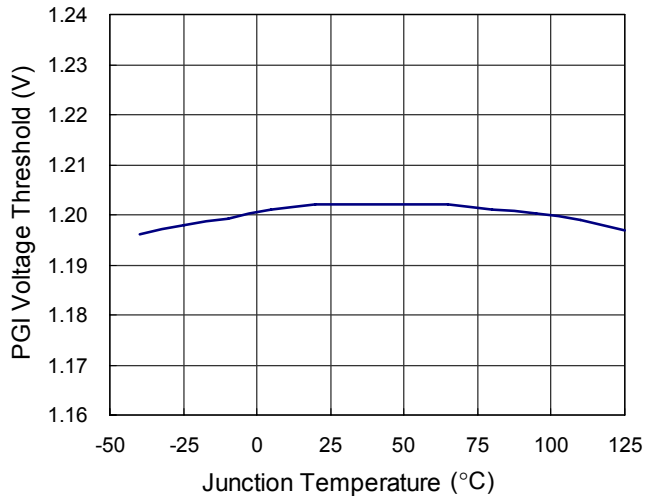
Falling&Rising UVLO Voltage Threshold vs. Junction Temperature



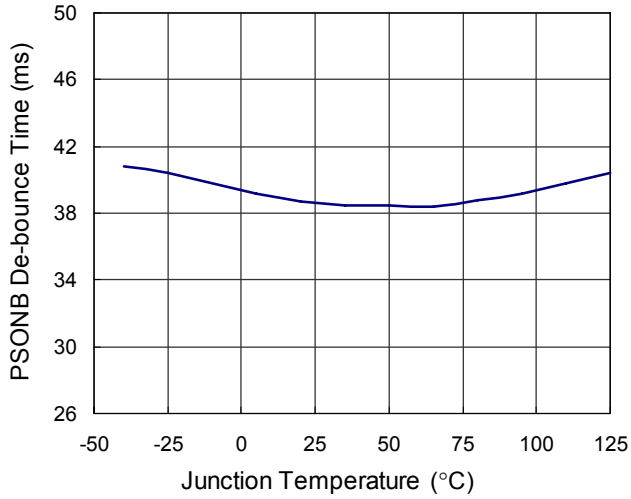
VDD Supply Current vs. Junction Temperature



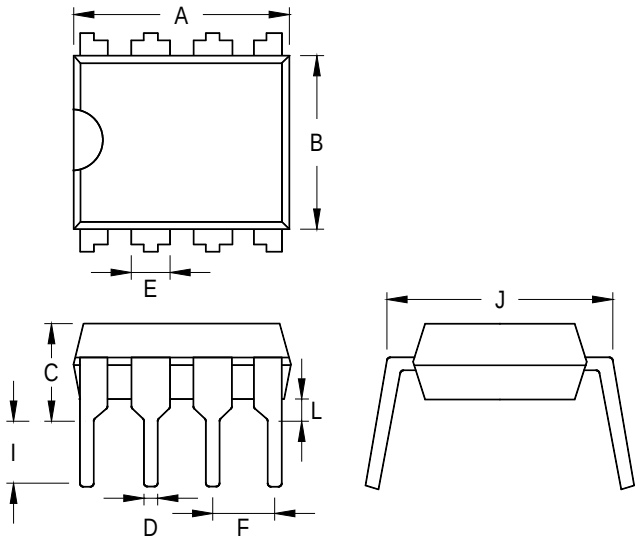
PGI Voltage Threshold vs. Junction Temperature



PSONB De-bounce Time vs. Junction Temperature



Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	9.068	9.627	0.357	0.379
B	6.198	6.604	0.244	0.260
C	3.556	4.318	0.140	0.170
D	0.356	0.559	0.014	0.022
E	1.397	1.651	0.055	0.065
F	2.337	2.743	0.092	0.108
I	3.048	3.556	0.120	0.140
J	7.366	8.255	0.290	0.325
L	0.381		0.015	

8-Lead DIP Plastic Package

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