Compal Confidential

EL5C3/EL531/EL431(C340/S340)

UMA M/B Schematic Document

Intel Whiskey Lake Processor with DDR4

2018-10-18

LA-H102P

REV :0.1

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Title: Cover Page			
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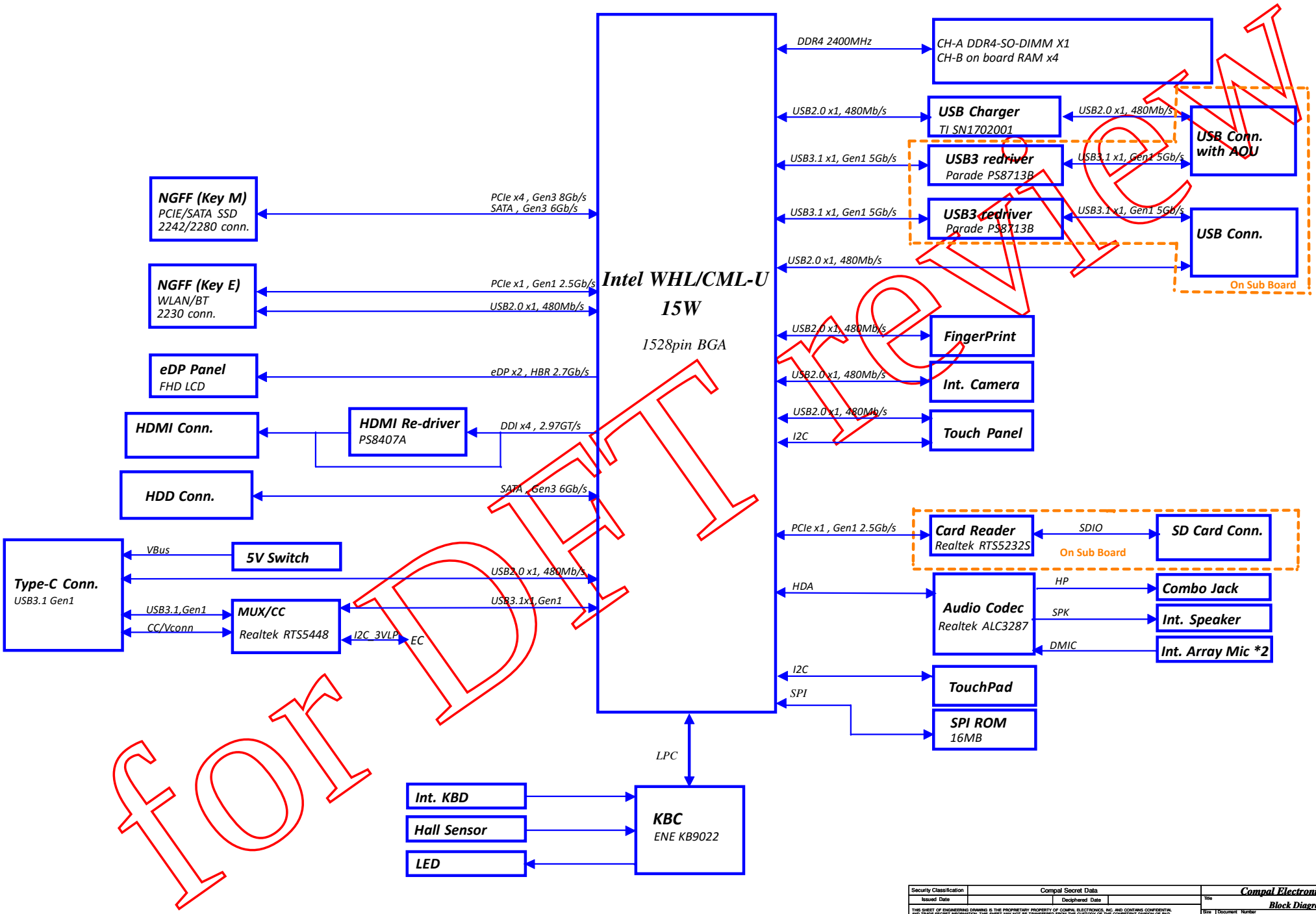

Security Classification	Compal Secret Data		Compal Electronics, Inc.
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Voltage Rails

power plane / State	B+	+5VALW +3VALW +1.8VALW +1.05VALW	+1.2V +2.5V	+5VS +3VS +VCCPLL_OC +1.05VS_VCCSTG +VCC_CORE +VCC_GT +VCC_SA +1.05V_VCCST +1.05VS_VCCIO +1.8VS +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM Structure Table

Item	BOM Structure
DIS Only Components	DIS@
UMA Only Components	UMA@
HDMI Logo	45@
Touch Screen	TS@
Memory Down - SDP Package	SDP@
Memory Down - DDP Package	DDP@
GPU GC6 Components	GC6@
Un-Mount GPU GC6 Components	NOGC6@
Connectors	ME@
Intel CNVi	CNVi@
EMI Category	EMI@
ESD Category	ESD@
RF Category	RF@
Test Point	TP@
Keyboard BackLight	KBL@
	NOKBL@
Project select	S540@
	S340@
	C340@
	S340_14@
	S340_15@
GPU select	N17S_G1@
	N17S_G0@
	N16V@
	N16S@
	N16@
	N17@
Memory Down select	MD@
	NO_MD@
MIC select	Arrary_MIC@
	Single_MIC@
TypeC 20V_PRTCT	20V_PRTCT@

Item	BOM Structure
S340_15 MD (Hynix 4GB)	H4G_S340_15@
S340_15 MD (Micron 4GB)	M4G_S340_15@
S340_15 MD (Samsung 4GB)	S4G_S340_15@
C340 MD (Hynix 4GB)	H4G_C340@
C340 MD (Micron 4GB)	M4G_C340@
C340 MD (Samsung 4GB)	S4G_C340@
On Board RAM X76 Resistors	X76RAM@
S340_15@ VRAM (Hynix 2GB)	VH2G_S340_15@
S340_15@ VRAM (Micron 2GB)	VM2G_S340_15@
S340_15@ VRAM (Samsung 2GB)	VS2G_S340_15@
C340 VRAM (Hynix 2GB)	VH2G_C340@
C340 VRAM (Micron 2GB)	VM2G_C340@
C340 VRAM (Samsung 2GB)	VS2G_C340@
S340_14 MD (Hynix 4GB)	H4G_S340_14@
S340_14 MD (Micron 4GB)	M4G_S340_14@
S340_14 MD (Samsung 4GB)	S4G_S340_14@
S340_14@ VRAM (Hynix 2GB)	VH2G_S340_14@
S340_14@ VRAM (Micron 2GB)	VM2G_S340_14@
S340_14@ VRAM (Samsung 2GB)	VS2G_S340_14@

USB 2.0 Port Table

Port	External USB Port
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	USB2/3 Port (Type-C)
4	Touch Screen
5	
6	Camera
7	Fingrt Print
8	
9	
10	NGFF WLAN+BT

USB 3.0 Port Table

Port	
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	USB2/3 Port (Type-C)
4	
5	
6	

PCIE Port Table

Port	Lane	
1		
2		
3		
4	0	
5	0	
6	1	
7	2	
8	3	
9	1	CardReader
10	0	
11		NGFF WLAN+BT
12	0	
13	3	
14	2	SSD
15	1	
16	0	

SATA Port Table

Port	
0	
1A	HDD
1B	SSD1

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x 16h

EC SM Bus2 address

Device	Address
NCT7718W	1001 100x 98h

PCH SM Bus address

Device	Address
DDR_JDIMM1 Touch Pad	1010 000x A0h

GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111x 9Eh

SMBUS Control Table

	SOURCE	DGPU	BATT	CHARGER	NECP388	SODIMM	Thermal Sensor	G-SENSOR
EC_SMB_CK1 EC_SMB_DA1	NECP388 +3VL	X	V +3VALW	V +19V_VIN	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	NECP388 +3VS	V +3VGS	X	X	V +3VS	X	X	X
EC_SMB_CK4 EC_SMB_DA4	NECP388 +3VS	X	X	X	X	X	X	V +3VS
SOC_SMBCLK SOC_SMBDATA	SOC +3VS	X	X	X	X	V +3VS	X	X
SOC_SML0CLK SOC_SML0DATA	SOC +3VS	X	X	X	V +3VS	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

ON BOARD RAM * 4 (total 4GB)

C340

ZZZ H4G_C340@ — X76 HYNIX 4GB MD — X76860538LA1
ZZZ M4G_C340@ — X76 MICRON 4GB MD — X76860538LA2
ZZZ S4G_C340@ — X76 SAMSUNG 4GB MD — X76860538LA3

S340-15

ZZZ H4G_S340_15@ — X76 HYNIX 4GB MD — X76843381L61
ZZZ M4G_S340_15@ — X76 MICRON 4GB MD — X76843381L62
ZZZ S4G_S340_15@ — X76 SAMSUNG 4GB MD — X76843381L63

S340-14

ZZZ H4G_S340_14@ — X76 HYNIX 4GB MD — XXXXXXXXX
ZZZ M4G_S340_14@ — X76 MICRON 4GB MD — XXXXXXXXX
ZZZ S4G_S340_14@ — X76 SAMSUNG 4GB MD — XXXXXXXXX

WHL CPU

UC1 i3 R1@ — X — I3-8145U — SA0000C6R20
UC1 i5 R1@ — X — I5-8265U — SA0000C6Q20
UC1 i7 R1@ — X — I7-8565U — SA0000C6P20
UC1 i3 R3@ — I3-8145U — SA0000C6R30
UC1 i5 R3@ — I5-8265U — SA0000C6Q30
UC1 i7 R3@ — I7-8565U — SA0000C6P30

PCB

ZZZ PCB@ — PCB — DA6001H6000

HDMI Logo

X4E

S340-15: ZZZ S340_15@ — X4E S340-15 — X4EAF838L51
C340-14: ZZZ C340@ — X4E C340 — X4EAF838L01
S340-14: ZZZ1 S340_14@ — X4E S340-14 — XXXXXXXXX

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Title: Notes List

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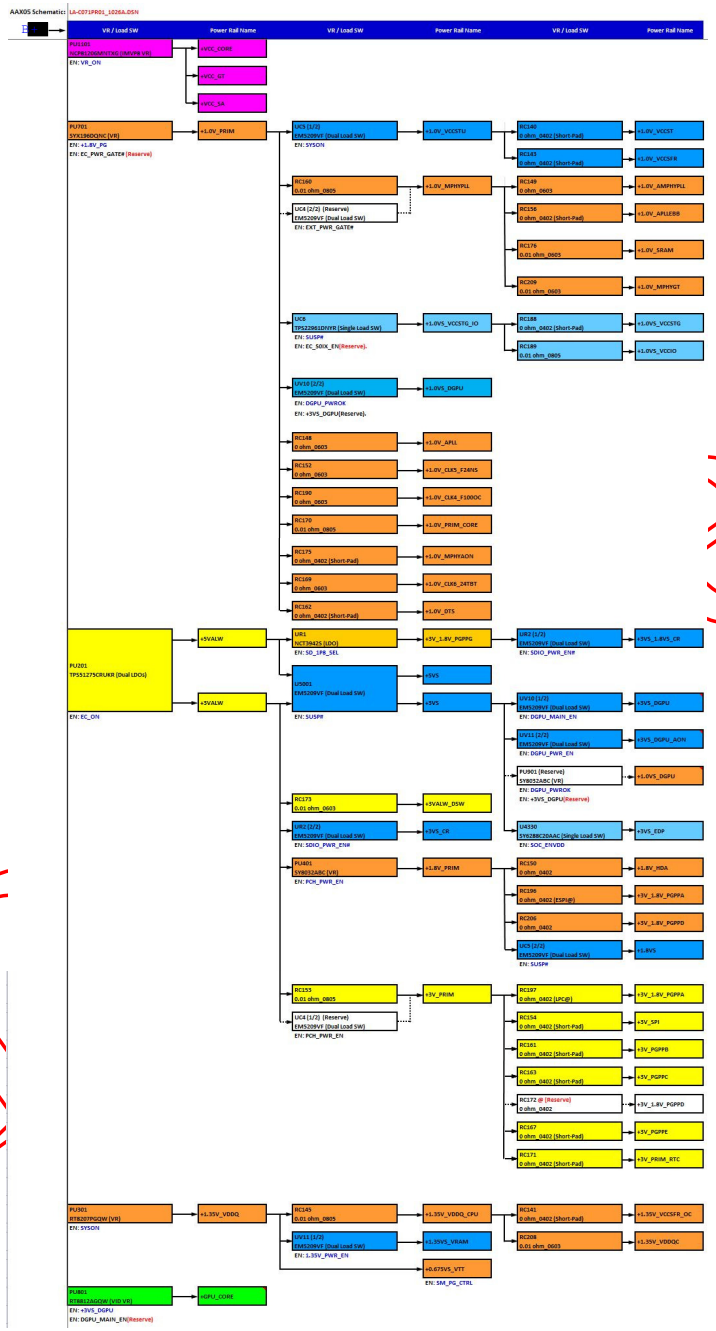
-PowerMap_DDR4_Volume_NON CS]



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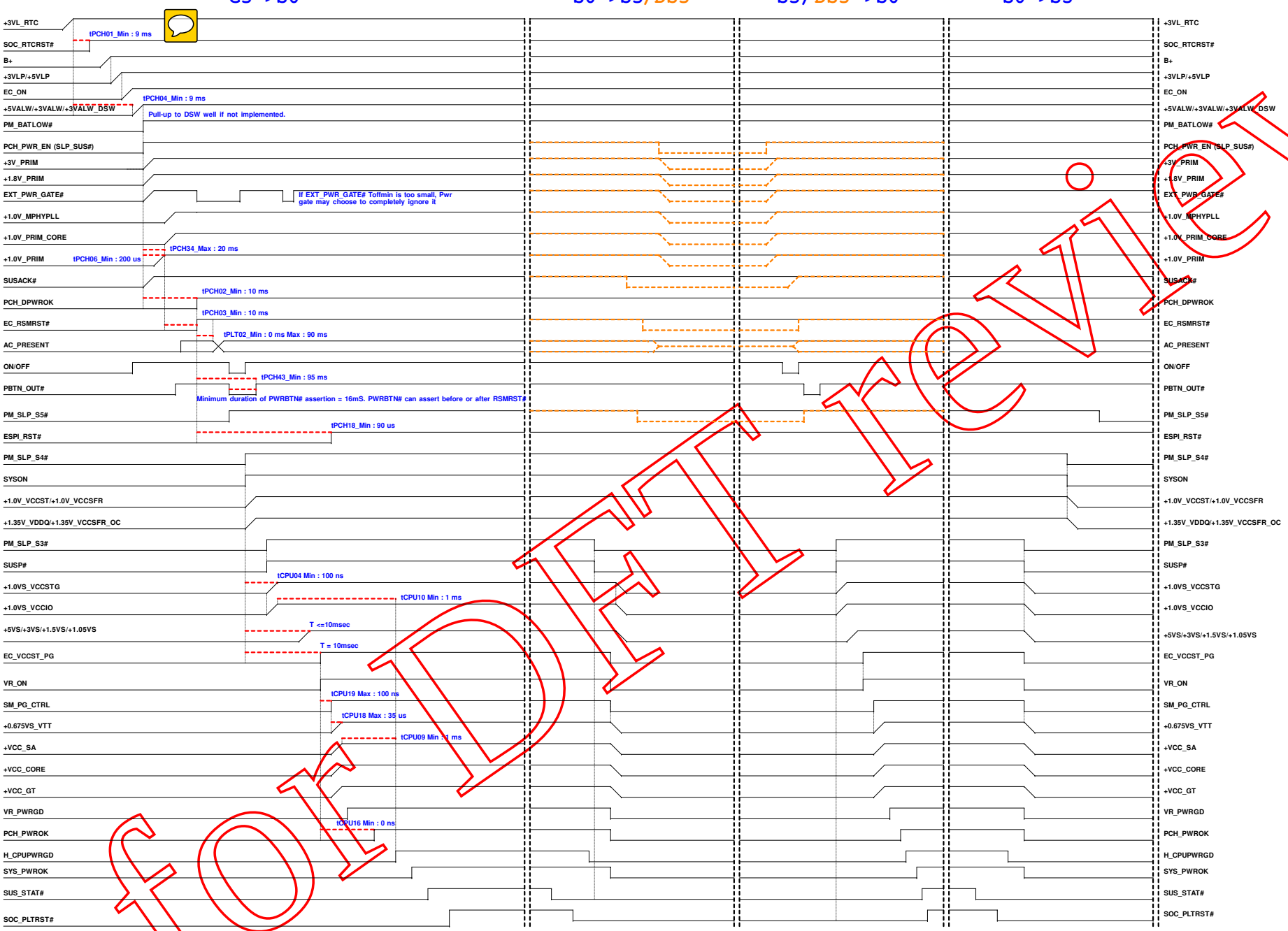

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Compal Electronics, Inc.	
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Table 5-13. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 3	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	
Port 4	DDPF_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm ±5% resistor	

< Compensation PU For eDP >

+1.05VS_VCCIO — RC2 1 — 2 24.9 0201 1% — EDP_COMP

Trace width=20 mils, Spacing=25mil, Max length=600mils

<HDMI>

<29> CPU_DP2_N0
<29> CPU_DP2_P0
<29> CPU_DP2_N1
<29> CPU_DP2_P1
<29> CPU_DP2_N2
<29> CPU_DP2_P2
<29> CPU_DP2_N3
<29> CPU_DP2_P3

UC1A

DDI1_TXN_0 AL5
DDI1_TXP_0 AL6
DDI1_TXN_1 AJ5
DDI1_TXP_1 AJ6
DDI1_TXN_2 AF6
DDI1_TXP_2 AF5
DDI1_TXN_3 AE5
DDI1_TXP_3 AE6

DDI2_TXN_0 AC4
DDI2_TXP_0 AC3
DDI2_TXN_1 AC1
DDI2_TXP_1 AC2
DDI2_TXN_2 AE4
DDI2_TXP_2 AE3
DDI2_TXN_3 AE1
DDI2_TXP_3 AE2

EDP_TXN_0 AG4
EDP_TXP_0 AG3
EDP_TXN_1 AG2
EDP_TXP_1 AG1
EDP_TXN_2 AJ4
EDP_TXP_2 AJ3
EDP_TXN_3 AJ2
EDP_TXP_3 AJ1

EDP_TXN0 <28>
EDP_TXP0 <28>
EDP_TXN1 <28>
EDP_TXP1 <28>
<eDP>

EDP_AUX_N AH4
EDP_AUX_P AH3
DISP_UTILS AM7

EDP_AUXN <28>
EDP_AUXP <28>

DDI1_AUX_N AC7
DDI1_AUX_P AC6
DDI2_AUX_N AD4
DDI2_AUX_P AD3
DDI3_AUX_N AG7
DDI3_AUX_P AG6

+3VS — EC_SCI# — RC1 1 — 2 10K 0402 5%

GPP_E13/DDPB_HPD0/DISP_MISC0 CN6
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6
GPP_E15/DPPD_HPD2/DISP_MISC2 CP7
GPP_E16/DPPE_HPD3/DISP_MISC3 CP6
GPP_E17/EDP_HPD/DISP_MISC4 CM7

CPU_DP2_HPD <29,30> From HDMI
EC_SCI# <34>
EDP_HPD <28>

EDP_BKLTEN CK11
EDP_VDDEN CG11
EDP_BKLTCTL CH11

ENBKL <34>
PCH_ENVDD <28>
INVPWM <28>
From eDP

EDP_COMP AM6
DISP_RCOMP

GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE# CC8
GPP_E19/DPPB_CTRLDATA CC9

HDMI DDC (Port 2)
<29,30> CPU_DP2_CTRL_CLK CH4
<29,30> CPU_DP2_CTRL_DATA CH3

GPP_E20/DPPC_CTRLCLK
GPP_E21/DPPC_CTRLDATA

<28> TS_I2C_RST# CP4

GPP_E22/DPPD_CTRLCLK CN4
GPP_E23/DPPD_CTRLDATA

GPP_H16/DDPF_CTRLCLK CR26
GPP_H17/DDPF_CTRLDATA CP26

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+1.05V_VCCST — RC8 1 — 2 1K 0402 5% — H_THERMTRIP#
RC10 2 — @ — 1 49.9 0402 1% — CATERR#

+1.05VS_VCCSTG — RC3 1K 0402 5% — H_PROCHOT#_R

<34> H_PROCHOT# — RC4 1 — 2 499 0402 1% — <34> H_PECI

If routed MS, PECI requires 18 mils spacing to other signals

UC1D

CATERR# AA4
PECI AR1
PROCHOT# Y4
THERMTRIP# BJ1

PROC_TCK T6 — CPU_XDP_TCK0
PROC_TDI U6 — SOC_XDP_TDI
PROC_TDO Y5 — SOC_XDP_TDO
PROC_TMS T5 — SOC_XDP_TMS
PROC_TRST# AB6 — SOC_XDP_TRST#

BPM#_0 U1
BPM#_1 U2
BPM#_2 U3
BPM#_3 U4

PCH_TCK W6 — PCH_JTAG_TCK1
PCH_TDI U5 — SOC_XDP_TDI
PCH_TDO W5 — SOC_XDP_TDO
PCH_TMS P5 — SOC_XDP_TMS
PCH_TRST# Y6 — SOC_XDP_TRST#
PCH_JTAG_TCK P6 — CPU_XDP_TCK0

GPP_E3/CPU_GP0 CE9
GPP_E7/CPU_GP1 CN3
GPP_B3/CPU_GP2 CB34
GPP_B4/CPU_GP3 CC35

PROC_PREQ# W2 — TP@ T1
PROC_PRDY# W1 — TP@ T2

RC11 2 — 1 49.9 0402 1% — CPU_POPIRCOMP — BP27
RC12 2 — 1 49.9 0402 1% — PCH_OPIRCOMP — BW25
RC14 2 — @ — 1 49.9 0402 1% — EDRAM_OPIO_RCOMP — L5
RC15 2 — @ — 1 49.9 0402 1% — EOPIO_RCOMP — N5

PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

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< PU/PD for CMC Debug >

+1.05VS_VCCSTG

SOC_XDP_TMS — RC5 1 — CMC@ 2 — 51 0402 5%
SOC_XDP_TDI — RC6 1 — CMC@ 2 — 51 0402 5%
SOC_XDP_TDO — RC7 1 — DCI@ 2 — 51 0402 5%
CPU_XDP_TCK0 — RC9 1 — DCI@ 2 — 51 0402 5%
PCH_JTAG_TCK1 — RC13 1 — @ 2 — 51 0402 5%
SOC_XDP_TRST# — RC16 1 — @ 2 — 51 0402 5%

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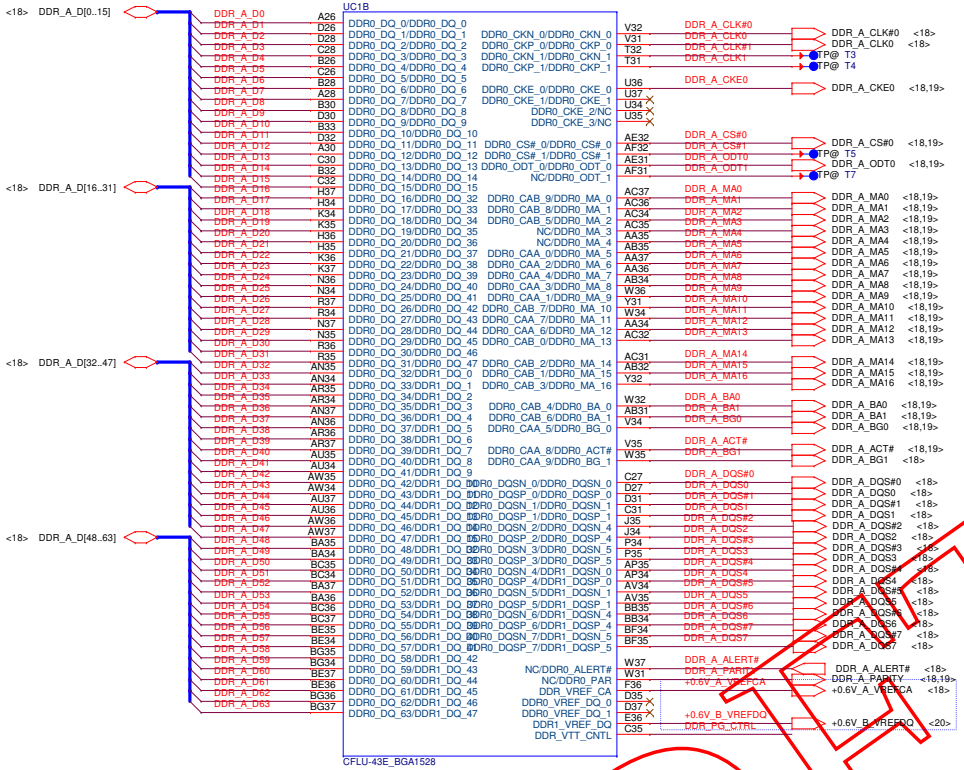
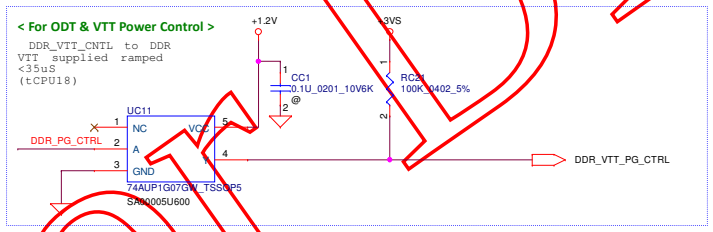
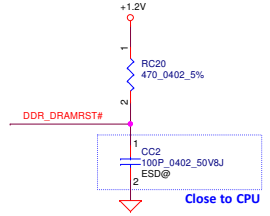
Interleaved Memory



Trace width/Spacing >= 20mils





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+3VALW

RC23 1 2 100K_0201_5% SOC_SPI_0_SI
RC24 1 2 100K_0201_5% SOC_SPI_0_IO2
RC25 1 2 100K_0201_5% SOC_SPI_0_IO3

Note: The internal pull-up is disabled when RSMRST# is asserted (during reset) and only enabled after RSMRST# de-assertion

SML1ALERT#/ PCHHOT#/GPP_B23	•If USB 3.1 Port 1 is used for 4-wire DCI.OOB (BSSB), and alternate functionality is also used on the pin, pull up to V3.3S with >100K resistor to avoid noise. •If USB 3.1 Port 1 is used for DCI.OOB (BSSB) 4-wire BSSB, and NO alternate functionality is used, leave float. •If DCI.OOB (BSSB) 2+2 functionality is used, pull up to V3.3S with a 4.7K resistor.

SML0ALERT# (Internal Pull Down):

eSPI or LPC

0 = LPC is selected for EC ==> Default

1 = eSPI is selected for EC

SPI ROM

UC1E

SOC_SPI_0_CLK CH37 — SPI0_CLK
SOC_SPI_0_SO CF37 — SPI0_MISO
SOC_SPI_0_SI CF36 — SPI0_MOSI
SOC_SPI_0_IO2 CF34 — SPI0_IO2
SOC_SPI_0_IO3 CG34 — SPI0_IO3
SOC_SPI_0_CS#0 CG36 — SPI0_CS0#
CG35 — SPI0_CS1#
CH34 — SPI0_CS2#

CF20 — GPP_D1/SPI1_CLK/BK1/SBK1
CG22 — GPP_D2/SPI1_MISO_IO1/BK2/SBK2
CF22 — GPP_D3/SPI1_MOSI_IO0/BK3/SBK3
CG23 — GPP_D21/SPI1_IO2
CH23 — GPP_D22/SPI1_IO3
CG20 — GPP_D0/SPI1_CS0#/BK0/SBK0

CH7 — CL_CLK
CH8 — CL_DATA
CH9 — CL_RST#

KB_RST# — SERIRQ — BV29 — GPP_A0/RCIN#/TIME_SYNC1
BV28 — GPP_A6/SERIRQ

<34> SERIRQ

GPP_C0/SMBCLK CK14 SOC_SMBCLK — SOC_SMBCLK <20>
GPP_C1/SMBDATA CH15 SOC_SMBDATA — SOC_SMBDATA <20>
GPP_C2/SMBALERT# CJ15 SOC_SMBALERT# — TP@ T8

GPP_C3/SML0CLK CH14 SOC_SML0CLK
GPP_C4/SML0DATA CF15 SOC_SML0DATA
GPP_C5/SML0ALERT# CG15 SOC_SML0ALERT# — TP@ T9

GPP_C6/SML1CLK CN15 — EC_SMB_CK2 <34>
GPP_C7/SML1DATA CM15 — EC_SMB_DA2 <34>
GPP_B23/SML1ALERT#/PCHHOT# CC34 SOC_SML1ALERT#

GPP_A1/LAD0/ESPI_IO0 CA29 LPC_AD0 — LPC_AD0 <34>
GPP_A2/LAD1/ESPI_IO1 BY29 LPC_AD1 — LPC_AD1 <34>
GPP_A3/LAD2/ESPI_IO2 BY27 LPC_AD2 — LPC_AD2 <34>
GPP_A4/LAD3/ESPI_IO3 BV27 LPC_AD3 — LPC_AD3 <34>
GPP_A5/LFRAME#/ESPI_CS# CA28 LPC_FRAME# — LPC_FRAME# <34>
GPP_A14/SUS_STAT#/ESPI_RESET# CA27

GPP_A9/CLKOUT_LPC0/ESPI_CLK BV32 LPC_CLK0 — RC27 1 EMI@ 2 22_0402_5% — CLK_LPC_EC <34>
GPP_A10/CLKOUT_LPC1 BV30
GPP_A8/CLKRUN# BY30 PM_CLKRUN# — PM_CLKRUN# <34>

CFLU-43E_BGA1528

SMB (Link to DAB)

SML1 (Link to EC, Thermal Sensor)

+3VS

RC26 1 2 10K_0402_5% KB_RST#

+3VS

RC28 1 2 8.2K_0402_5% SERIRQ

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close to SPI ROM

From SOC

SOC_SPI_0_SO RC29 1 2 33_0402_5% SOC_SPI_0_SO_R
SOC_SPI_0_CLK RC31 1 EMI@ 2 33_0402_5% SOC_SPI_0_CLK_R
SOC_SPI_0_SI RC32 1 2 33_0402_5% SOC_SPI_0_SI_R
SOC_SPI_0_IO3 RC34 1 2 33_0402_5% SOC_SPI_0_IO3_R

SOC_SPI_0_IO2 RC36 1 2 33_0402_5% SOC_SPI_0_IO2_R

From EC

<34> EC_SPI_CLK — EC_SPI_CLK RC41 1 EMI@ 2 33_0402_5% SOC_SPI_0_CLK_R
<34> EC_SPI_MOSI — EC_SPI_MOSI RC42 1 2 33_0402_5% SOC_SPI_0_SI_R
<34> EC_SPI_CS0# — EC_SPI_CS0# RC43 1 2 33_0402_5% SOC_SPI_0_CS#0
<34> EC_SPI_MISO — EC_SPI_MISO RC44 1 2 33_0402_5% SOC_SPI_0_SO_R

< SPI ROM - 16M >

+3VALW

UC12
SOC_SPI_0_CS#0 1 CS#
SOC_SPI_0_SO_R 2 DO(IO1)
SOC_SPI_0_IO2_R 3 IO2
4 GND
VCC 8
IO3 7 SOC_SPI_0_IO3_R
CLK 6 SOC_SPI_0_CLK_R
DI(IO0) 5 SOC_SPI_0_SI_R
XM25QH128AHIG SOP 8P

CC3 1 @ 2 0.1U_0201_10V K X5R

CC4 @EMI@ 1 2 10P_0402_50V8J

+3VS

EC_SMB_CK2 RC30 1 2 1K_0402_5%
EC_SMB_DA2 RC33 1 2 1K_0402_5%

SOC_SML1ALERT# RC35 1 @ 2 150K_0402_5%

SOC_SMBCLK RC37 1 2 1K_0402_5%
SOC_SMBDATA RC38 1 2 1K_0402_5%
SOC_SML0CLK RC39 1 2 1K_0402_5%
SOC_SML0DATA RC40 1 2 1K_0402_5%

PM_CLKRUN# RC45 1 2 8.2K_0402_5%

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Title: **WHL-U(3/12)SPI,SMB,LPC,ESPI**

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< HD AUDIO >

<33> HDA_BIT_CLK_R — RC46 1 EMI@ 2 33_0402_5% — HDA_BIT_CLK
<33> HDA_SYNC_R — RC48 1 2 33_0402_5% — HDA_SYNC
<33> HDA_SDOUT_R — RC47 1 2 33_0402_5% — HDA_SDOUT
HDA_SDOUT — RC49 499_0402_1% (1, @, 2)

< To Enable ME Override >

<34> ME_EN — RC51 1 @ 2 0_0402_5% — HDA_SDOUT

+3VS — RC55 1 @ 2 2.2K_0402_5% — HDA_SPKR

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode. ==> Default

1 = Enable TOP Swap Mode.

75K_0402_5% 1 CNVi@ 2 RC52 — CNV_RF_RESET#

Follow Jefferson Peak schematic check list.

RC164 1 @ 2 1K_0402_5% — WLBT_OFF#

UC1G

<33> HDA_SDIN0 — HDA_SYNC (BN34) / HDA_BIT_CLK (BN37) / HDA_SDOUT (BN36) / BN35 / BL36 / BL35 / CK23 / BL37 / BL34
HDA_SYNC/I2S0_SFRM
HDA_BCLK/I2S0_SCLK
HDA_SDO/I2S0_TXD
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD/SNDW1_DATA
HDA_RST#/I2S1_SCLK/SNDW1_CLK
GPP_D23/I2S_MCLK
I2S1_SFRM/SNDW2_CLK
I2S1_TXD/SNDW2_DATA

<31> CNV_RF_RESET# — CNV_RF_RESET# — CJ32
GPP_H1/I2S2_SFRM/CNV_BT_I2S_BCLK/CNV_RF_RESET#

<31> CLKREQ_CNV# — CH32
GPP_H0/I2S2_SCLK/CNV_BT_I2S_SCLK

CH29
GPP_H2/I2S2_TXD/CNV_BT_I2S_SDI/MODEM_CLKREQ

CH30
GPP_H3/I2S2_RXD/CNV_BT_I2S_SDO

CP24
GPP_D19/DMIC_CLK0/SNDW4_CLK

CN24
GPP_D20/DMIC_DATA0/SNDW4_DATA

CK25
GPP_D17/DMIC_CLK1/SNDW3_CLK

CJ25
GPP_D18/DMIC_DATA1/SNDW3_DATA1

<33> HDA_SPKR — HDA_SPKR — CF35
GPP_B14/SPKR

GPP_G0/SD_CMD CH36
GPP_G1/SD3_DATA0 CL35
GPP_G2/SD3_DATA1 CL36
GPP_G3/SD3_DATA2 CM35
GPP_G4/SD3_DATA3 CN35
GPP_G5/SD_CD# CH35
GPP_G6/SD_CLK CK36
GPP_G7/SD_WP CK34

GPP_A17/SD_VDD1_PWR_EN#/ISH_GP7 BW36
GPP_A16/SD_1P8_SEL BY31

SD_1P8_RCOMP CK33
SD_3P3_RCOMP CM34
SOC_SD_RCOMP — RC50 1 2 200_0402_1%

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GPP_H21 XTAL frequency select.
0: 38.4 / 19.2 MHz
1: 24MHz XTAL select.

UC1I

<31> CNV_CRX_DTX_N0 — CR30
<31> CNV_CRX_DTX_P0 — CP30
CNV_WR_D0N
CNV_WR_D0P

<31> CNV_CRX_DTX_N1 — CM30
<31> CNV_CRX_DTX_P1 — CN30
<31> CNV_CTX_DRX_N0 — CN32
<31> CNV_CTX_DRX_P0 — CM32
CNV_WR_D1N
CNV_WR_D1P
CNV_WT_D0N
CNV_WT_D0P

<31> CNV_CTX_DRX_N1 — CP33
<31> CNV_CTX_DRX_P1 — CN33
CNV_WT_D1N
CNV_WT_D1P

<31> CLK_CNV_CRX_DTX_N — CN31
<31> CLK_CNV_CRX_DTX_P — CP31
<31> CLK_CNV_CTX_DRX_N — CP34
<31> CLK_CNV_CTX_DRX_P — CN34
CNV_WR_CLKN
CNV_WR_CLKP
CNV_WT_CLKN
CNV_WT_CLKP

RC56 1 CNVi@ 2 150_0402_1% — CNV_WT_RCOMP — CP32
CNV_WT_RCOMP_0
CNV_WT_RCOMP_1
CR32
GPP_F0/CNV_PA_BLANKING CP20

CK19
GPP_F1
CG17
GPP_F2

<35> TP_INT# — CR14
GPP_C8/UART0_RXD

CP14
GPP_C9/UART0_TXD

<31> WLBT_OFF# — WLBT_OFF# — CN14
GPP_C10/UART0_RTS#

CM14
GPP_C11/UART0_CTS#

CJ17
GPP_F8/CNV_MFUART2_RXD

CH17
GPP_F9/CNV_MFUART2_TXD

RC57 1 2 10K_0402_5% — SOC_A4WP_PRESENT — CF17
GPP_F23/A4WP_PRESENT

GPP_H18/CPU_C10_GATE# CN27
GPP_H19/TIMESYNC_0 CM27
GPP_H21 CF25
GPP_H22 CN26
GPP_H23 CM26
GPP_F10 CK17
GPD7 BV35
GPP_F3 CN20
GPP_D4/IMGCLKOUT0/BK4/SBK4 CG25
GPP_H20/IMGCLKOUT_1 CH25

GPP_F12/EMMC_DATA0 CR20
GPP_F13/EMMC_DATA1 CM20
GPP_F14/EMMC_DATA2 CN19
GPP_F15/EMMC_DATA3 CM19
GPP_F16/EMMC_DATA4 CN18
GPP_F17/EMMC_DATA5 CR18
GPP_F18/EMMC_DATA6 CP18
GPP_F19/EMMC_DATA7 CM18

GPP_F20/EMMC_RCLK CM16
GPP_F21/EMMC_CLK CP16
GPP_F11/EMMC_CMD CR16
GPP_F22/EMMC_RESET# CN16
EMMC_RCOMP
CK15

SOC_C10_GATE# — TP@ T10
SOC_GPP_H21 — RC53 1 2 4.7K_0201_5%
SOC_GPD7 — RC54 1 2 100K_0201_5%
+3VALW

XTAL INPUT MODE (HVM ONLY)
LOW: XTAL INPUT IS SINGLE ENDED
HIGH: XTAL IS ATTACHED

SOC_SD_RCOMP

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Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Compal Electronics, Inc.

Title: WHL-U(4/12)HDA,EMMC,SDIO,CSI2

Size	Document Number	Rev
Custom	LA-H102P	0.1

Date: Thursday, October 18, 2018 Sheet 9 of 51

SRCCLKREQ#[5:0].

Any used, enabled, and mapped SRCCLKREQ# signal should connect to a PCIe* connector pin or a device down ball with a 10K Ohm ±10% external pull-up resistor to core rail..

Any un-used, disabled, and non-mapped SRCCLKREQ# signal must be left as no connects at the PCH side on the platform..

Note: The SRCCLKREQ# signals can be configured to map to any of the PCH PCI Express* Root Ports while using any of the CLKOUT_PCIE_P/N differential pairs. Refer to latest version of the Cannon Lake PCH External Design Specification (EDS) and Intel® FW Bring-Up Guide for details on how to assign the SRCCLKREQ# signals..

5/9 Naming Rule

+3VS

RC61 10K_0402_5% CLKREQ_PCIE#1
RC63 10K_0402_5% CLKREQ_PCIE#3
RC64 10K_0402_5% CLKREQ_PCIE#4
RC68 @ 10K_0402_5%

SSD <32> CLK_PCIE_N1 / <32> CLK_PCIE_P1 / <32> CLKREQ_PCIE#1
WLAN <31> CLK_PCIE_N3 / <31> CLK_PCIE_P3 / <31> CLKREQ_PCIE#3
Card Reader <37> CLK_PCIE_N4 / <37> CLK_PCIE_P4 / <37> CLKREQ_PCIE#4

UC1J

AW2	CLKOUT_PCIE_N_0	CLKOUT_ITPXDP_N	AU1
AY3	CLKOUT_PCIE_P_0	CLKOUT_ITPXDP_P	AU2
CF32	GPP_B5/SRCCLKREQ0#		
		GPD8/SUSCLK	BT32 → SUSCLK <31>
BC1	CLKOUT_PCIE_N_1	XTAL_IN	CK3 ← 33E_SOC_XTAL24_IN_R
BC2	CLKOUT_PCIE_P_1	XTAL_OUT	CK2 → 33E_SOC_XTAL24_OUT_R
CE32	GPP_B6/SRCCLKREQ1#		
		CLK_BIASREF	CJ1 ← XCLK_BIASREF
BD3	CLKOUT_PCIE_N_2	CLKIN_XTAL	CM3 ← CLKIN_XTAL → CLKIN_XTAL <31>
BC3	CLKOUT_PCIE_P_2		
CF30	GPP_B7/SRCCLKREQ2#		
		RTCX1	BN31 ↔ SOC_RTCX1
BH3	CLKOUT_PCIE_N_3	RTCX2	BN32 ↔ SOC_RTCX2
BH4	CLKOUT_PCIE_P_3		
CE31	GPP_B8/SRCCLKREQ3#	SRTCRST#	BR37 ↔ SOC_SRTCRST#
		RTCRST#	BR34 ↔ SOC_RTCRST#
BA1	CLKOUT_PCIE_N_4		
BA2	CLKOUT_PCIE_P_4		
CE30	GPP_B9/SRCCLKREQ4#		
BE1	CLKOUT_PCIE_N_5		
BE2	CLKOUT_PCIE_P_5		
CF31	GPP_B10/SRCCLKREQ5#		

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CLKREQ_PCIE#1 / CLKREQ_PCIE#3 / CLKREQ_PCIE#4

XCLK_BIASREF — RC60 1 2 60.4_0402_1%
CLKIN_XTAL — RC65 1 2 10K_0402_5%

Follow CFL-U PDG_Rev_0.7
Stuff 60.4 ohm(RC110) PD for CNL-U, WHL-U and CFL-U

33E_SOC_XTAL24_IN_R — RC66 EMI@ 33_0201_5% — 33E_SOC_XTAL24_IN
LC1 @EMI@ DLM0NSN900HY2D 4P
33E_SOC_XTAL24_OUT_R — RC73 EMI@ 33_0201_5% — 33E_SOC_XTAL24_OUT

+3VL_RTC

RC70 20K_0402_5% SOC_SRTCRST#
CC5 1U_0201_6.3V6M SE00000UC00
RC71 20K_0402_5% SOC_RTCRST#
RC72 @ 0_0402_5% EC_CLEAR_CMOS# <34>
CC6 1U_0201_6.3V6M SE00000UC00
CLRP1 SHORT PADS CLR_CMOS
RC75 1M_0402_5% SM_INTRUDER#

RC74 200K_0402_1%

YC1 24MHZ_18PF_XRCGB24M000F2P51R0 SJ10000UJ00
NC NC
CC7 27P_0402_50V8J
CC8 27P_0402_50V8J

+3VALW

RC77 10K_0402_5% SYS_RESET#
RC78 10K_0402_5% PCH_PWROK
RC79 10K_0402_5% EC_RSMRST#

< PCH PLTRST Buffer >

SOC_PLTRST# — RC76 0_0402_5% — PCI_RST# <21,22,34,37>
RC80 100K_0402_5%
CC9 ESD@ 100P_0402_50V8J

SOC_RTCX2
SOC_RTCX1
RC81 10M_0402_5%
YC2 32.768KHZ_9PF_X1A000141000200 SJ10000PW00
CC13 8.2P_0402_50V8B
CC14 8.2P_0402_50V8B

ESD@ CC10 100P_0402_50V8J SYS_RESET#
ESD@ CC11 100P_0402_50V8J EC_RSMRST#
ESD@ CC12 100P_0402_50V8J SYS_PWROK

+3VALW

RC82 1K_0402_5% WAKE#

UC1K

SOC_PLTRST#	BJ35	GPP_B12/SLP_S0#	BJ37 → PM_SLP_S0# → TP@T12
SYS_RESET#	CN1	GPD4/SLP_S3#	BU36 → PM_SLP_S3# → PM_SLP_S3# <34>
EC_RSMRST#	BR36	GPD5/SLP_S4#	BU27 → PM_SLP_S4# → PM_SLP_S4# <34,42,45>
		GPD10/SLP_S5#	BT29 → PM_SLP_S5# → TP@T13
H_CPUPWRGD	AR2	SLP_SUS#	BU29
EC_VCCST_PG	BJ2	SLP_LAN#	BT31
PROCPWRGD		GPD9/SLP_WLAN#	BT30 → SLP_WLAN# → TP@T14
VCCST_PWRGOOD		GPD6/SLP_A#	BU37 → PM_SLP_A# → TP@T15
SYS_PWROK	CR10		
PCH_PWROK	BP31	GPD3/PWRBTN#	BU28 → PBTN_OUT#
EC_RSMRST#	BP30	GPD1/ACPRESENT	BU35 ← AC_PRESENT_R ← RC83 1 @ 2 0_0402_5% ← PBTN_OUT# <34> / AC_PRESENT <34>
DSW_PWROK		GPD0/BATLOW#	BV36 ← PM_BATLOW#
GPP_A13/SUSWARN#/SUSPWRDACK	BV34		
GPP_A15/SUSACK#	BY32	INTRUDER#	BR35 → SM_INTRUDER#
WAKE#	BU30	GPP_B11/EXT_PWR_GATE#	CC37
GPD2/LAN_WAKE#	BU32	GPP_B2/VRALERT#	CC36 → SOC_VRALERT#
GPD11/LANPHYPC	BU34	INPUT3VSEL	BT27 → SOC_INPUT3VSEL

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<34> EC_RSMRST# — T111 TP@ — H_CPUPWRGD
<34> SYS_PWROK
<34> PCH_PWROK
WAKE#

+3VALW

PM_BATLOW# — RC84 8.2K_0402_5%
AC_PRESENT — RC85 @ 10K_0402_5%
SOC_VRALERT# — RC86 @ 10K_0402_5%
SOC_INPUT3VSEL — RC87 @ 4.7K_0402_5%
RC88 4.7K_0402_5%

From EC (Open-Drain)

+1.05V_VCCST
RC89 1K_0402_5%
<34> VCCST_PWRGD — RC90 1 2 0_0402_5% — EC_VCCST_PG
CC15 100P_0402_50V8J ESD@

INPUT3VSEL	I	Strapped high if PCH's VCCDSW_3P3 rail is 3.0V +/-5%; else PCH's VCCDSW_3P3 rail is 3.3V +/- 5%. This pin is in the VCCPRIM_3P3 well. **Note:** When strapped for 3.0V operation, it is expected that the rest of the platform's 3.3V rails are at 3.0V (e.g. the battery is a 1S configured battery) and that components can function properly at 3.0V.

Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Compal Electronics, Inc.

Title: WHL-U(5/12)CLK,PM,GPIO

Size	Document Number	Rev
Custom	LA-H102P	0.1

Date: Thursday, October 18, 2018 Sheet 10 of 51

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This funct i oni s usef ul when running ITP/XDP.

GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode ==> Default

1 = LPC Mode

Capacity	Description	X76	PART NUMBER (R1)
4GB	WITHOUT ON-BOARD RAM	NO_MD@	N/A
	HYNIX 2666MHz (H5AN8G6NCJR-VKC) S340	X7680438L81	SA0000BMN00
	HYNIX 2666MHz (H5AN8G6NCJR-VKC) C340	X7680538LA1	
	MICRON 2666MHz (MT40A512M16LY-075:E) S340	X7680438L82	SA0000ARD20
	MICRON 2666MHz (MT40A512M16LY-075:E) C340	X7680538LA2	
	SAMSUNG 2666MHz (K4A8G165WC-BCTD) S340	X7680438L83	SA0000B6F00
	SAMSUNG 2666MHz (K4A8G165WC-BCTD) C340	X7680538LA3	
	N/A	N/A	N/A

Capacity	Description	GPP_B19	GPP_B20	GPP_B21
		OBRAM_ID0	OBRAM_ID1	OBRAM_ID2
4GB	WITHOUT ON-BOARD RAM	0	0	0
	SAMSUNG 2666MHz (K4A8G165WC-BCTD)	0	0	1
	HYNIX 2666MHz (H5AN8G6NCJR-VKC)	0	1	0
	MICRON 2666MHz (MT40A512M16LY-075:E)	0	1	1
	N/A	1	0	0
	N/A	1	0	1
	N/A	1	1	0
	N/A	1	1	1

Function	MODEL_SETTING2 (GPP_D10)
Array MIC	1
Single MIC	0

Function	MODEL_SETTING1 (GPP_D12)	MODEL_SETTING0 (GPP_D11)
C340-15	0	0
S340-15	0	1
S340-14	1	0

Function	DGPU_PRSNT (GPP_C15)
DIS	0
UMA Only	1

Table 1-26. Miscellaneous Signals on the Processor Checklist

Pin Name	System Pull-up / Pull-down	Schematics Notes	✓
RCIN#/GPP_A0	Pull-up to V3.3S with 10 KΩ resistor.	Driven by discrete glue logic or SIO which act as keyboard controller to generate INIT# to the processor.	
PROCPWRGD		This signal is indication of PROCPWRGOOD.	
PIRQA#/GPP_A7	Pull-up to V3.3S with 8.2 KΩ ~10 KΩ resistor.		

Place close to PCH

for RMT test

6 Layer / 8 Layer PCB

for DVT review

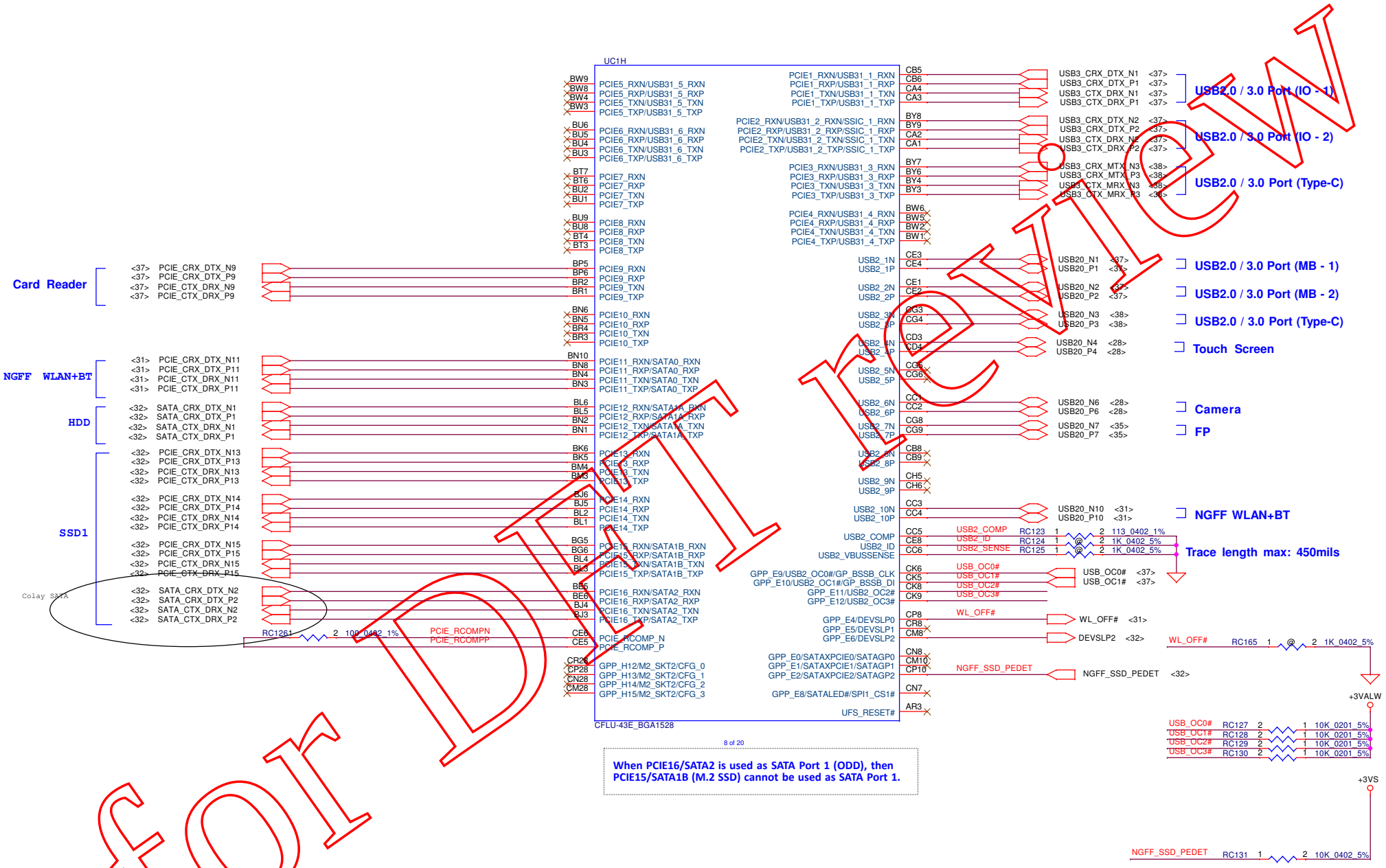
Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Compal Electronics, Inc.

Title: WHL-U(6/12)GPIO,I2C,GSPI

Size: Custom | Document Number: LA-H102P | Rev: 0.1

Date: Thursday, October 18, 2018 | Sheet 11 of 51



Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

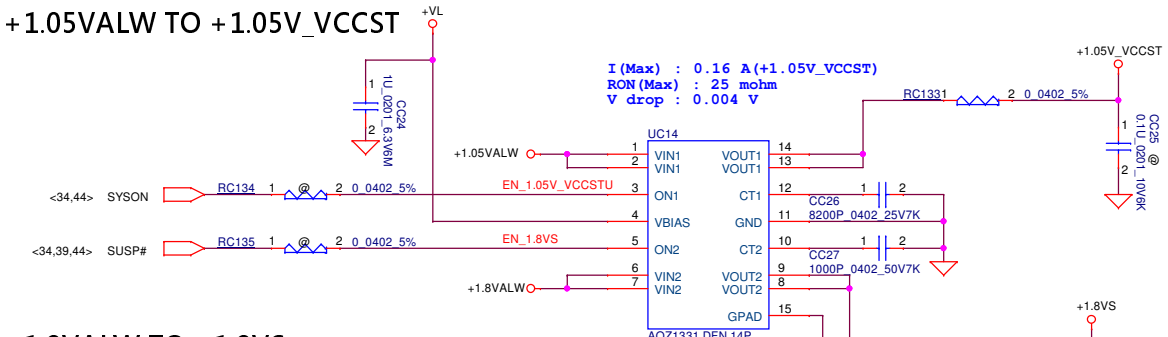
Compal Electronics, Inc.

Title: **WHL-U(7/12)PCIE,USB,SATA**

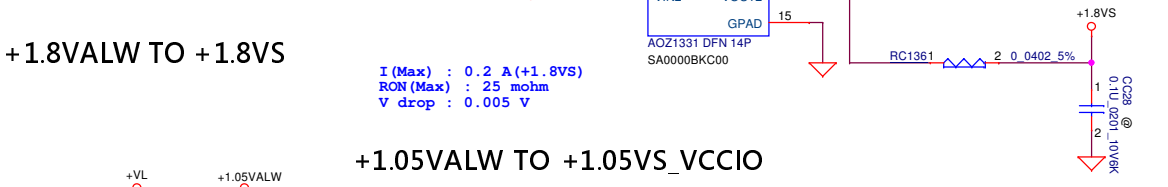
Size	Document Number	Rev
Custom	LA-H102P	0.1

Date: Thursday, October 18, 2018 Sheet 12 of 51

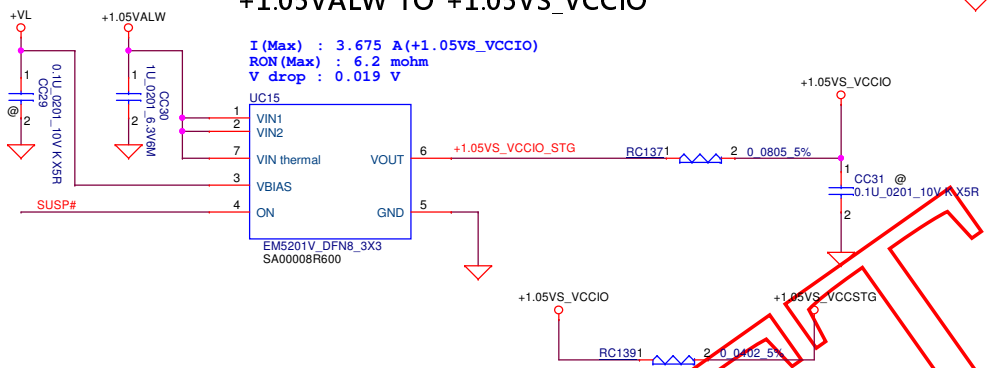
+1.05VALW TO +1.05V_VCCST

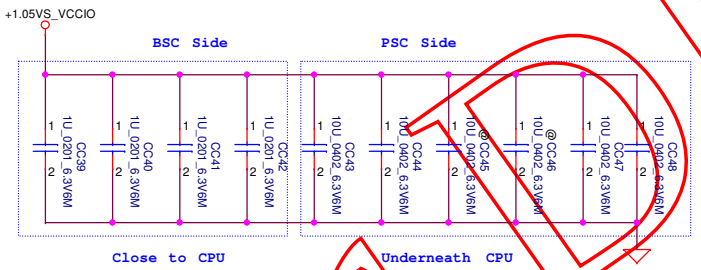


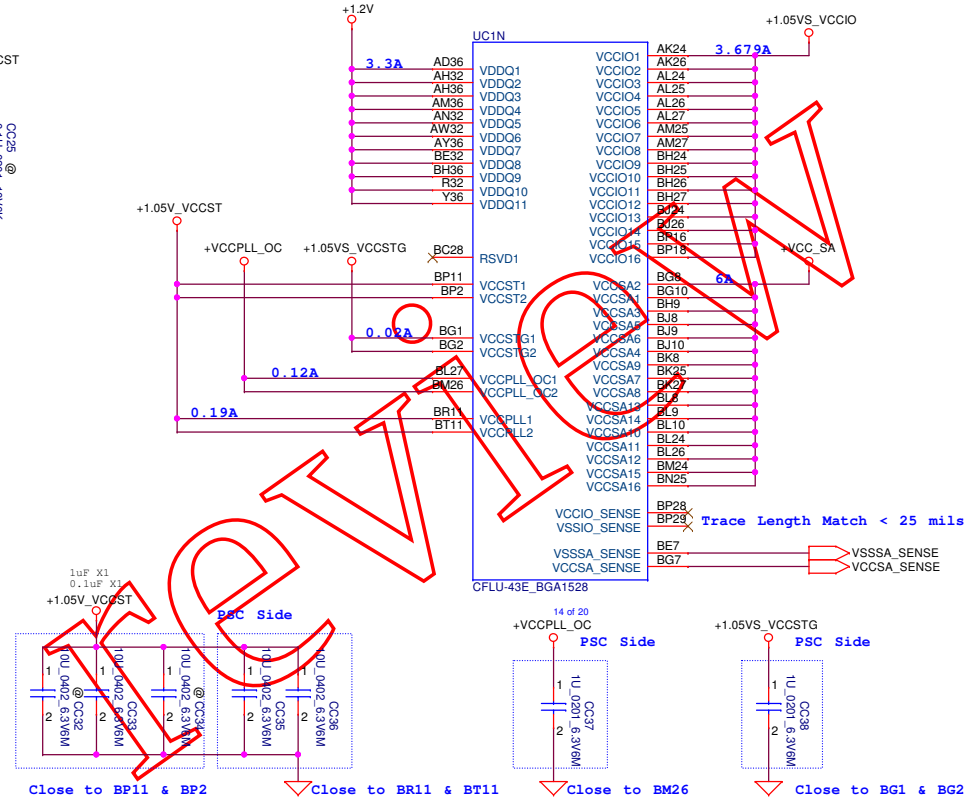
+1.8VALW TO +1.8VS

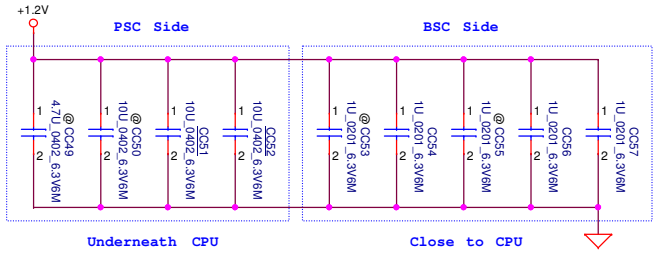


+1.05VALW TO +1.05VS_VCCIO

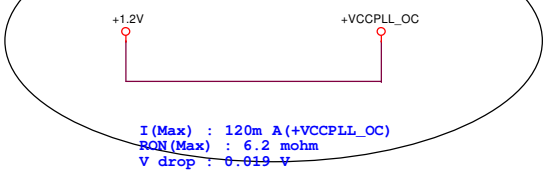






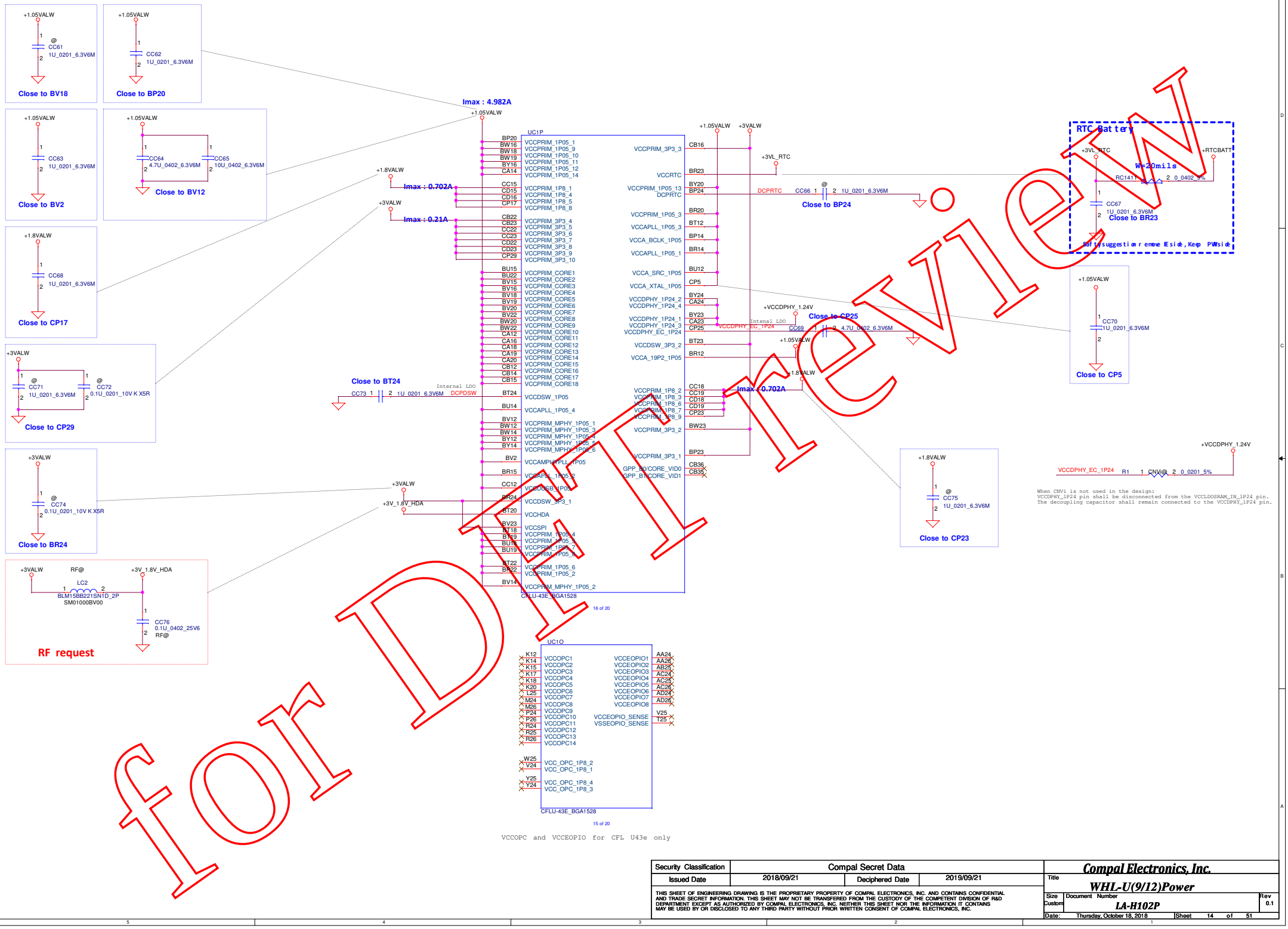


+1.2V TO +VCCPLL_OC



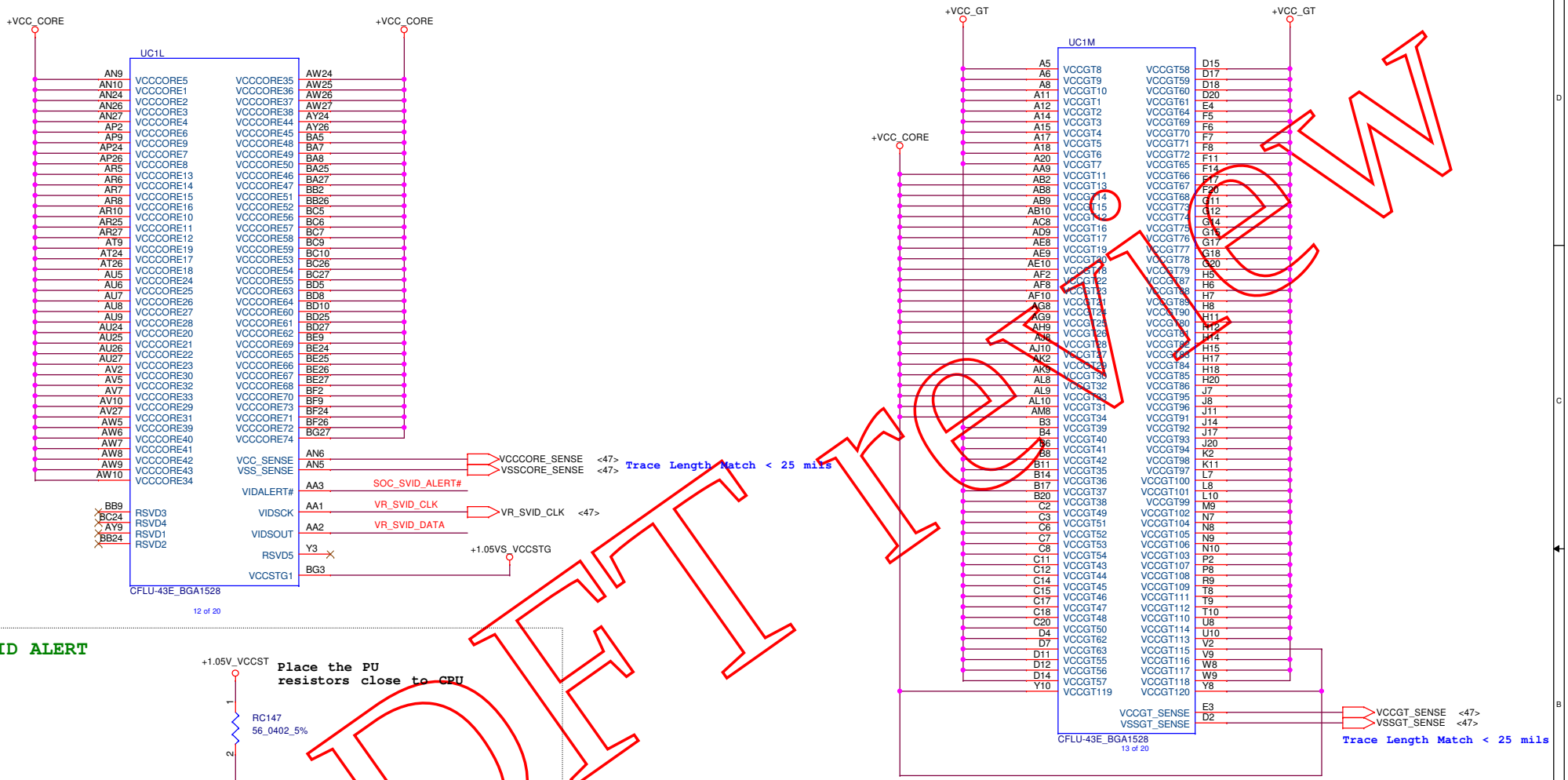
Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Compal Electronics, Inc.			
Title: WHL-U(8/12)Power			
Size: Custom	Document Number: LA-H102P		Rev: 0.1
Date: Thursday, October 18, 2018	Sheet 13 of 51		



Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Compal Electronics, Inc.			
Title: WHL-U(9/12)Power			
Size: Custom	Document Number: LA-H102P		Rev: 0.1
Date: Thursday, October 18, 2018	Sheet 14 of 51		



Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Compal Electronics, Inc.

Title: **WHL-U(10/12)Power,SVID**

Size	Document Number	Rev
Custom	LA-H102P	0.1

Date: Thursday, October 18, 2018 Sheet 15 of 51

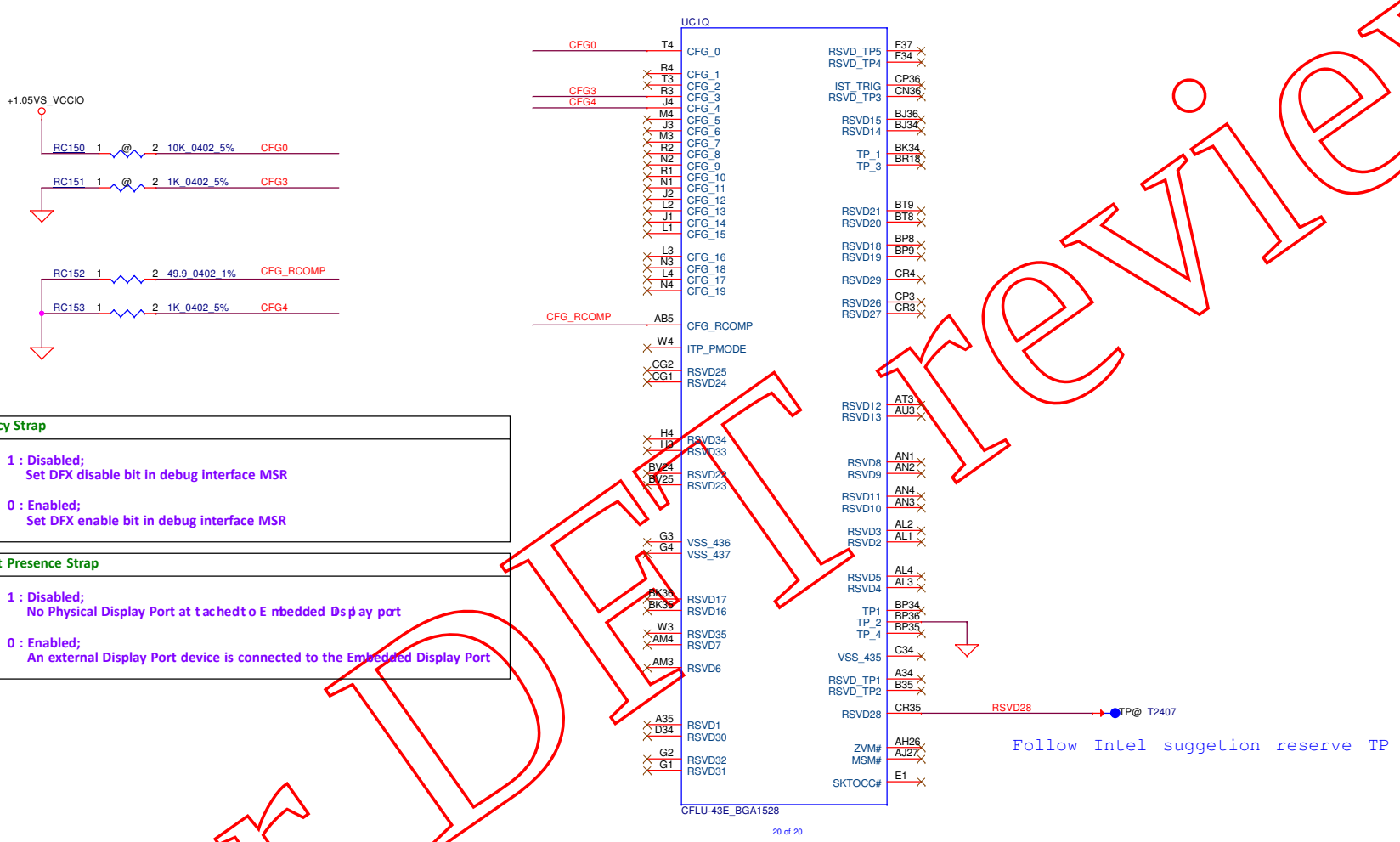
Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Compal Electronics, Inc.

Title: **WHL-U(11/12)GND**

Size	Document Number	Rev
Custom	LA-H102P	0.1

Date: Thursday, October 18, 2018 | Sheet 16 of 51



Follow Intel suggetion reserve TP

DFX Privacy Strap	
CFG3	1 : Disabled; Set DFX disable bit in debug interface MSR 0 : Enabled; Set DFX enable bit in debug interface MSR

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port at t achedt o E mbedded D sp ay port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

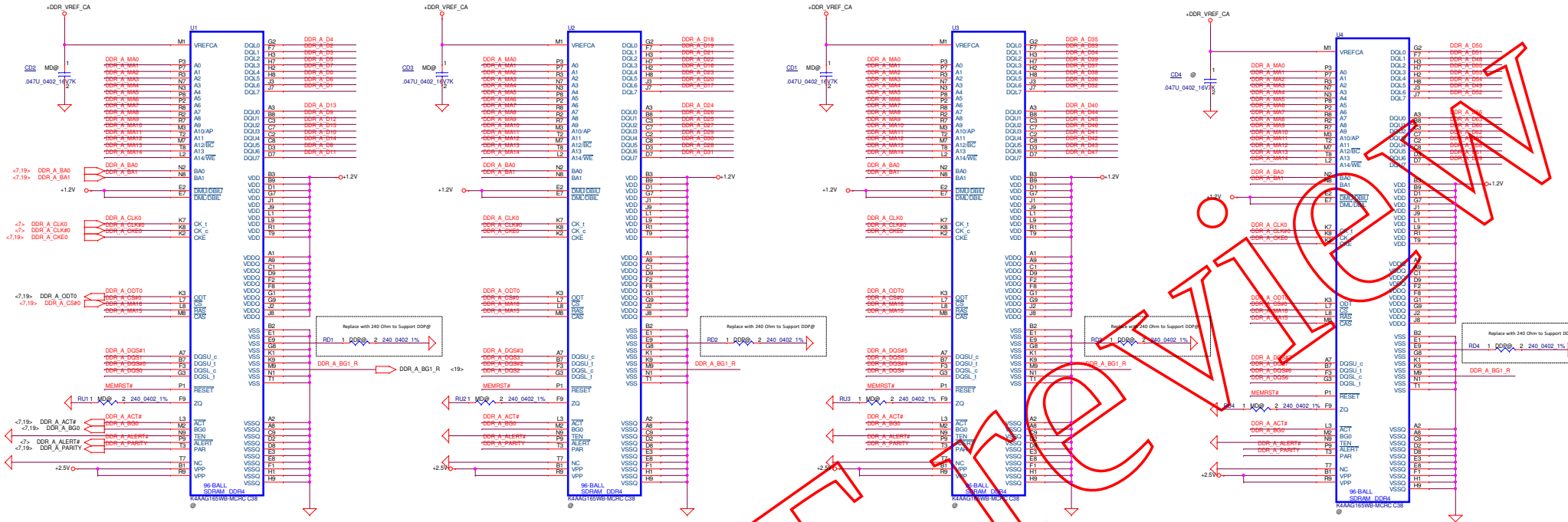
Compal Electronics, Inc.

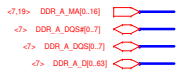
Title: WHL-U(12/12)CFG,RSVD

Size	Document Number	Rev
Custom	LA-H102P	0.1

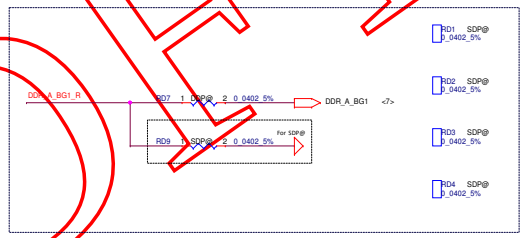
Date: Thursday, October 18, 2018 Sheet 17 of 51

Interleaved Memory





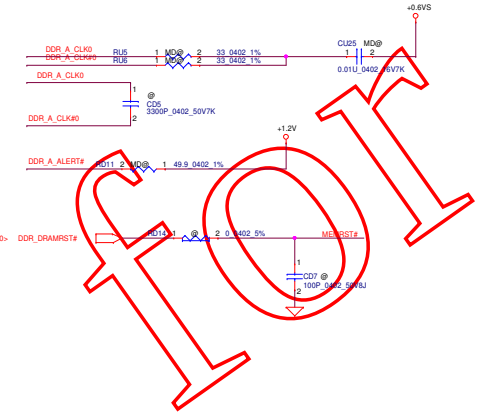
Co-lay for SDP / DDP Memory DIE

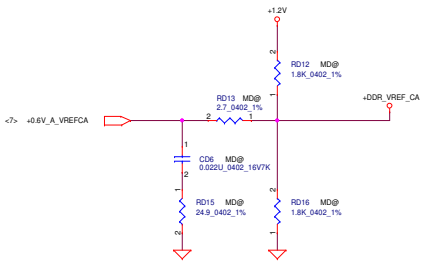


On Board RAM - Data Mapping

U4	DQ	U2	DQ	U3	DQ	U1	DQ
DQL0	D13	DQL0	D29	DQL0	D43	DQL0	D60
DQL1	D12	DQL1	D25	DQL1	D40	DQL1	D61
DQL2	D11	DQL2	D27	DQL2	D42	DQL2	D62
DQL3	D8	DQL3	D24	DQL3	D41	DQL3	D57
DQL4	D10	DQL4	D30	DQL4	D47	DQL4	D58
DQL5	D9	DQL5	D28	DQL5	D45	DQL5	D56
DQL6	D14	DQL6	D31	DQL6	D46	DQL6	D59
DQL7	D15	DQL7	D26	DQL7	D44	DQL7	D63
DQU0	D6	DQU0	D22	DQU0	D38	DQU0	D50
DQU1	D1	DQU1	D17	DQU1	D37	DQU1	D52
DQU2	D7	DQU2	D23	DQU2	D35	DQU2	D51
DQU3	D5	DQU3	D20	DQU3	D32	DQU3	D48
DQU4	D3	DQU4	D19	DQU4	D33	DQU4	D54
DQU5	D4	DQU5	D16	DQU5	D36	DQU5	D53
DQU6	D2	DQU6	D18	DQU6	D39	DQU6	D55
DQU7	D0	DQU7	D21	DQU7	D34	DQU7	D49

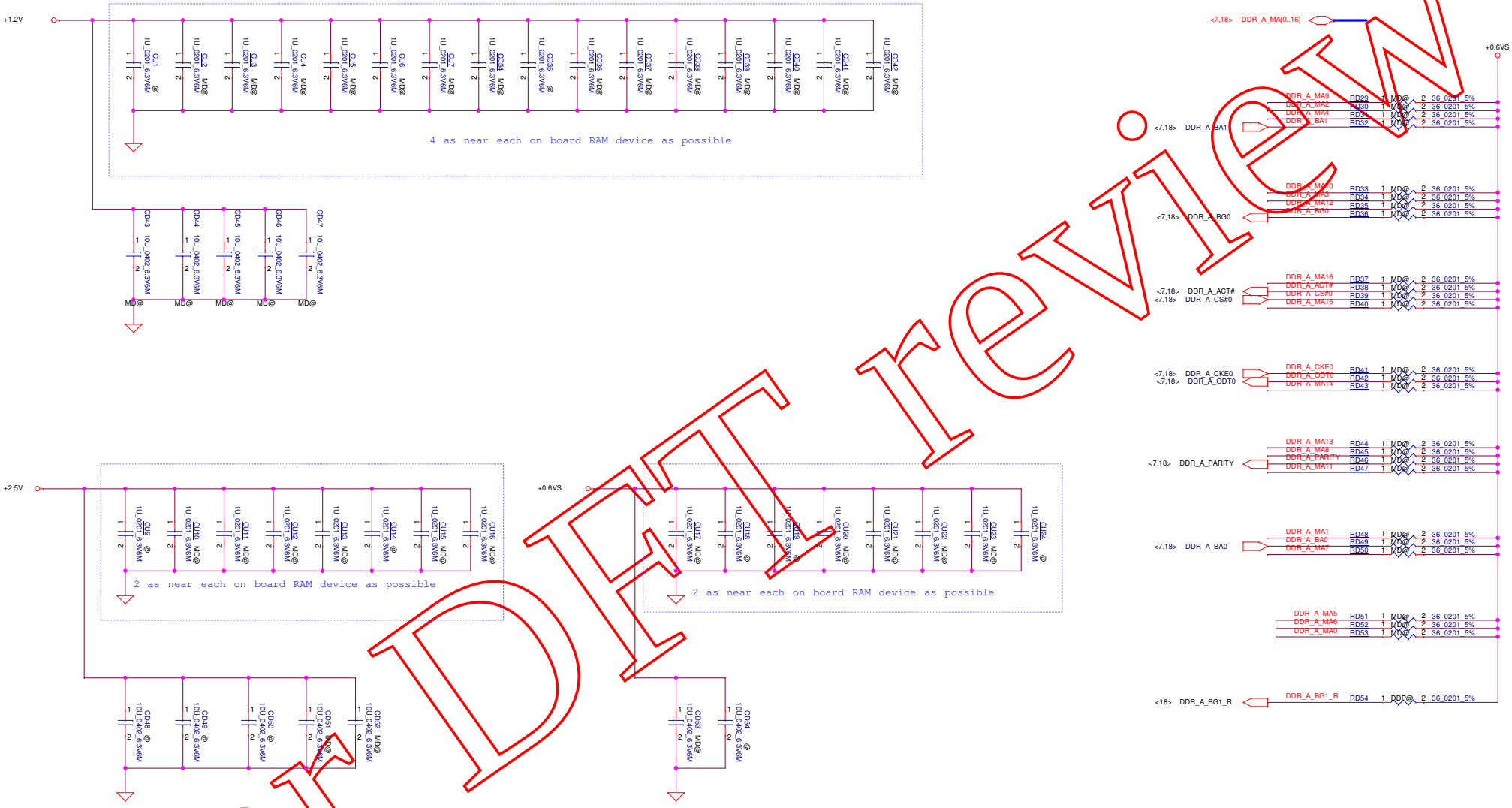
CLOCK TERMINATION





Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Title	DDR4 ON BOARD CHIPS		
Size: Custom	Document Number: LA-H102P		Rev: 0.1
Date: Thursday, October 18, 2018	Sheet 18 of 51		

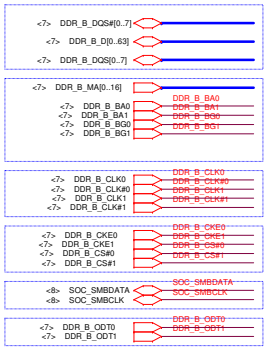


Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Title	DDR4 MISC		
Size: Custom	Document Number		Rev: 0.1
Date: Thursday, October 18, 2018	Sheet 19 of 51		

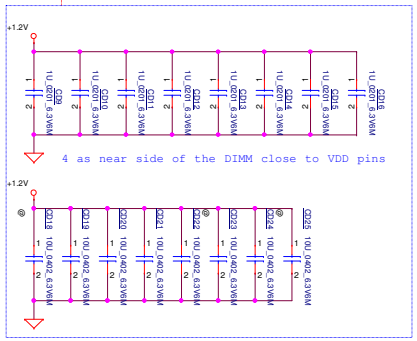
Standard Type

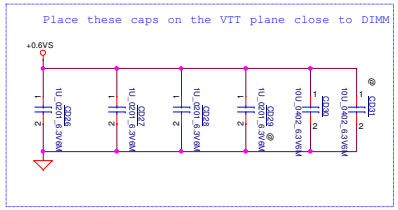
2-3A to 1 DIMMs/channel

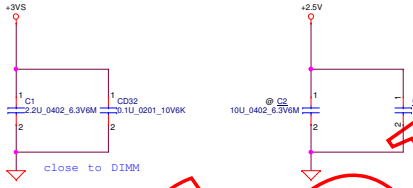


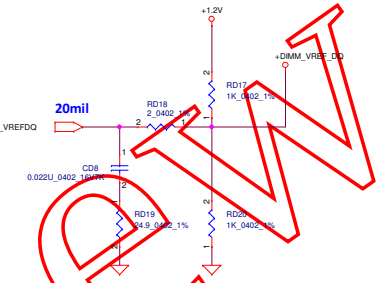
Layout Note:
Place near JDIMM1

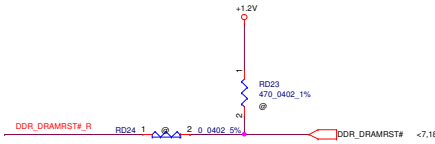
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket



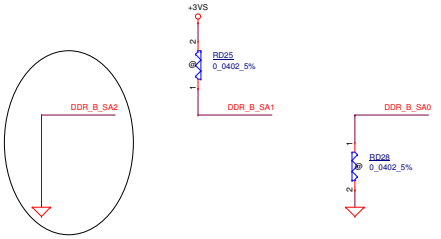








JDIMM1 ADDRESS (PLACE CLOSE TO DIMM)



Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Compal Electronics, Inc.

Title: **DDR4 DIMM**

Size	Document Number	Rev
Custom	LA-H102P	0.1

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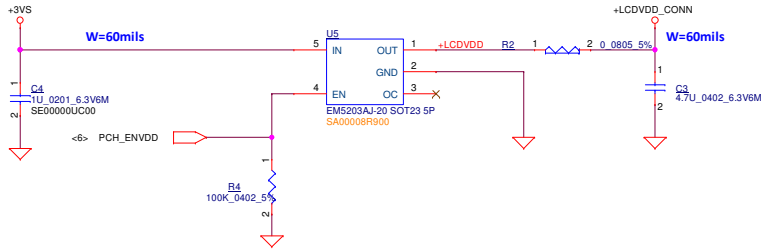
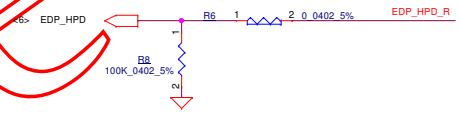
LCD POWER SWITCH



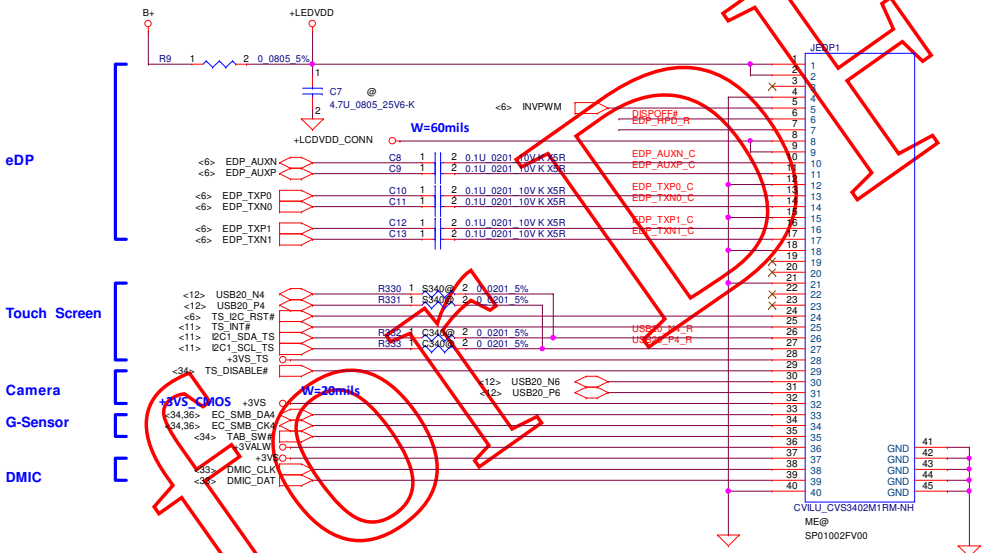
CAMERA POWER CIRCUIT

DISPLAY OFF

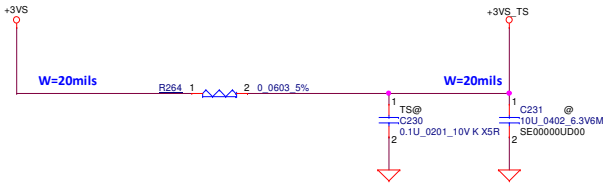
HOT PLUG DETECT



eDP CONNECTOR

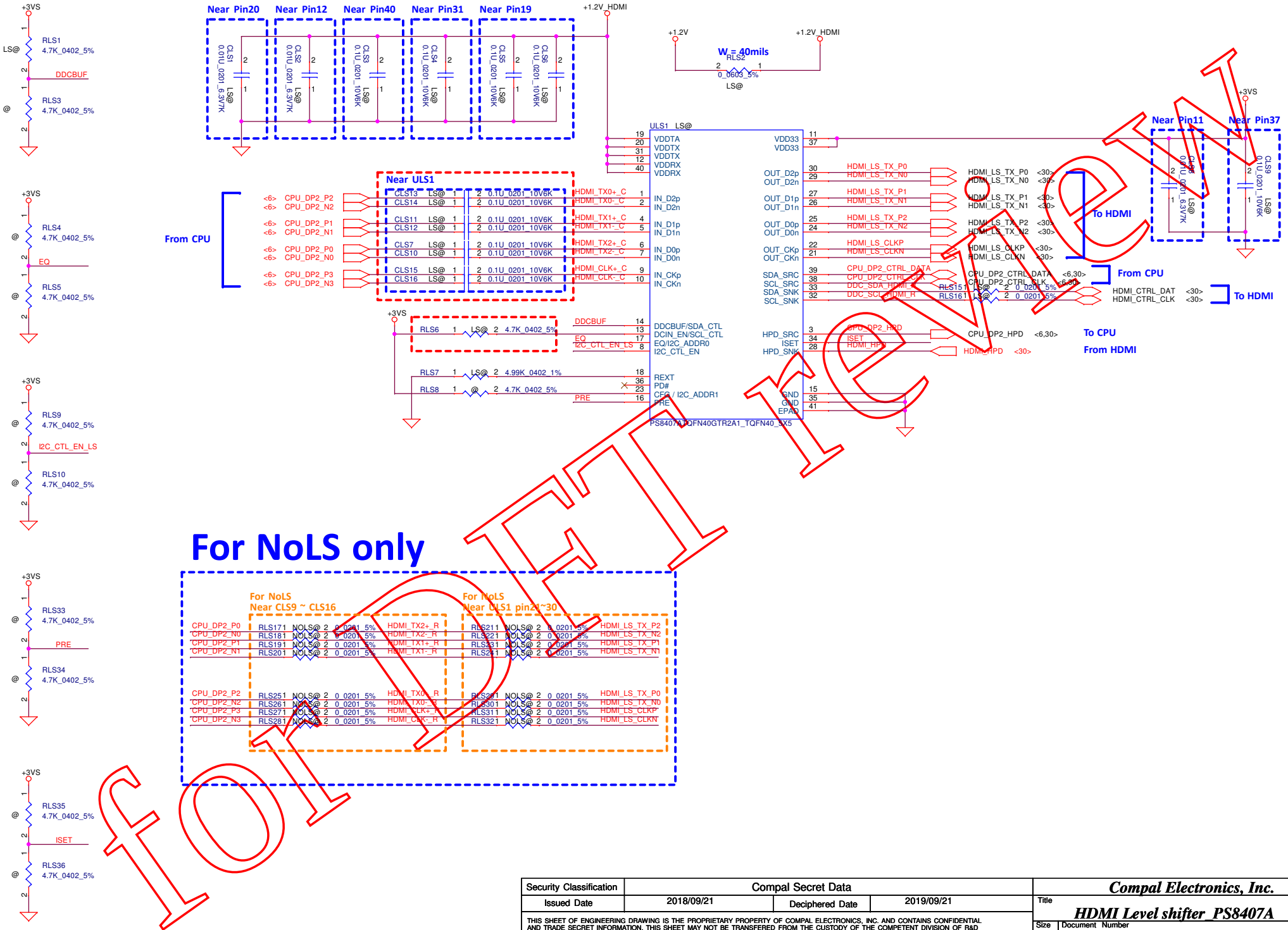


Touch Screen POWER CIRCUIT



Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

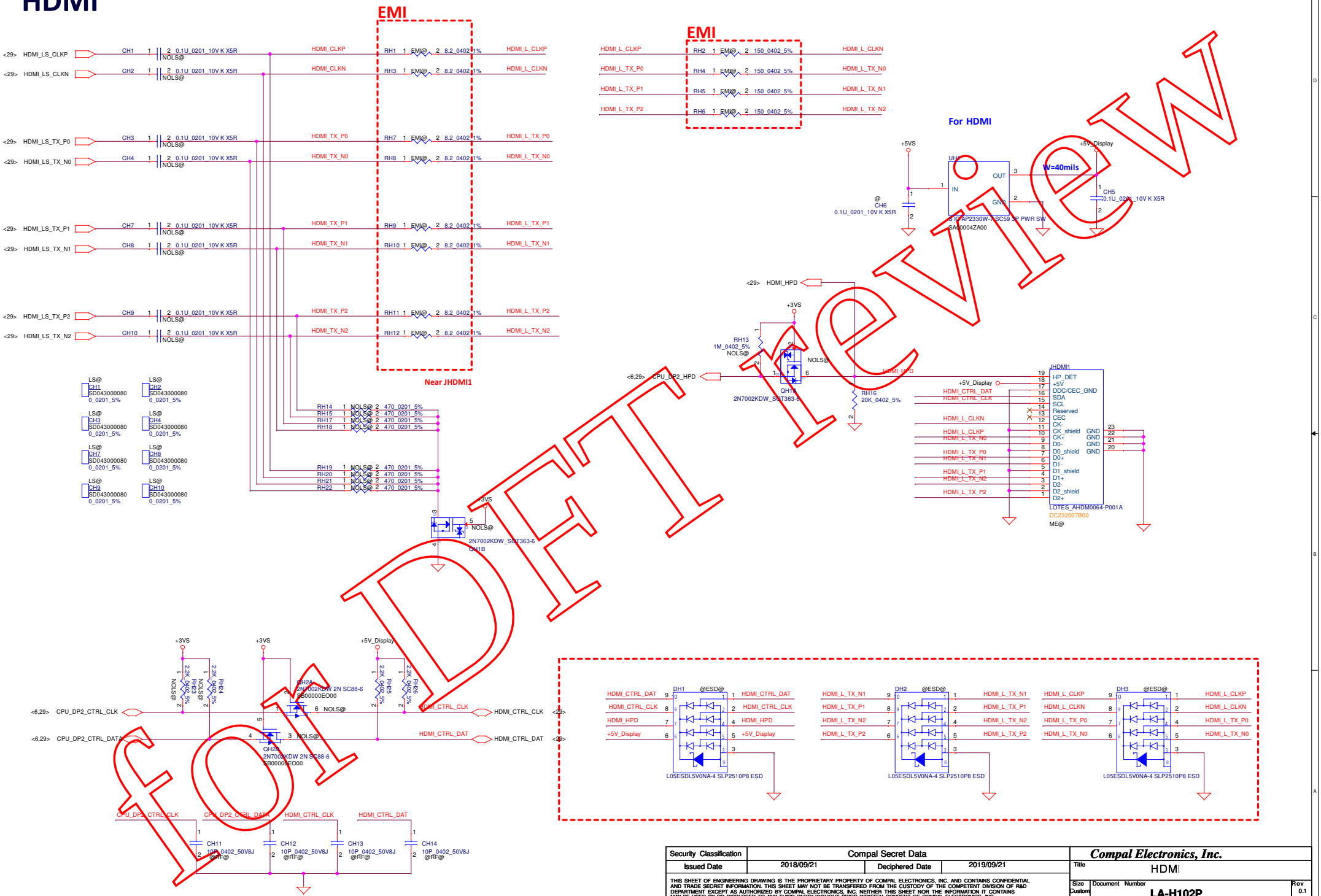
Compal Electronics, Inc.			
Title	eDP / Camera / MIC		
Size	Document Number		Rev
Custom	LA-H102P		0.1
Date:	Thursday, October 18, 2018	Sheet	28 of 51



Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Compal Electronics, Inc.			
Title: HDMI Level shifter_PS8407A			
Size	Document Number: LA-H102P		Rev: 0.1
Date: Thursday, October 18, 2018	Sheet 29 of 51		

HDMI



Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Compal Electronics, Inc.

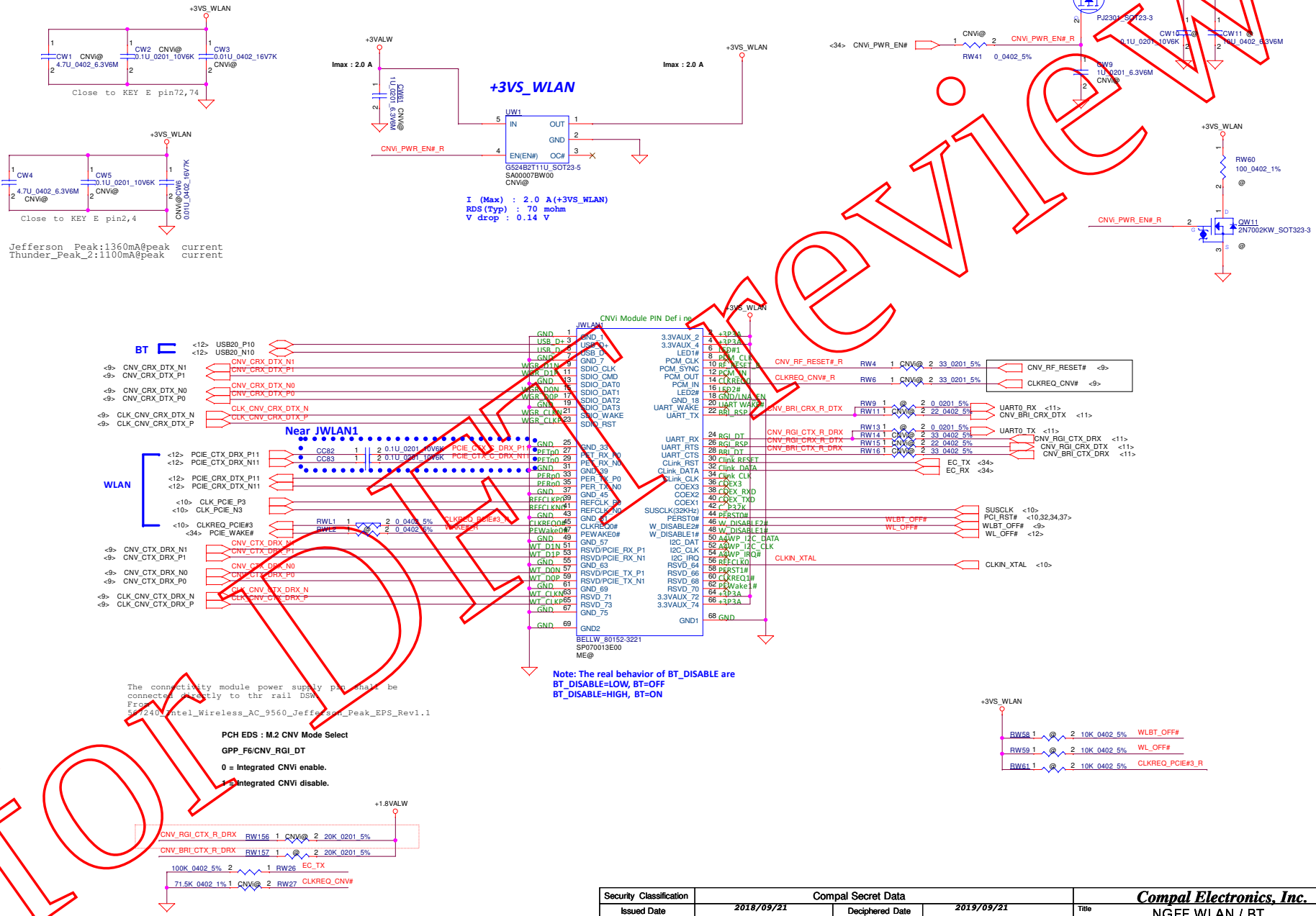
Title: HDMI

Size: Custom | Document Number: LA-H102P | Rev: 0.1

Date: Thursday, October 18, 2018 | Sheet 30 of 51

NGFF WLAN /BT(Key E)

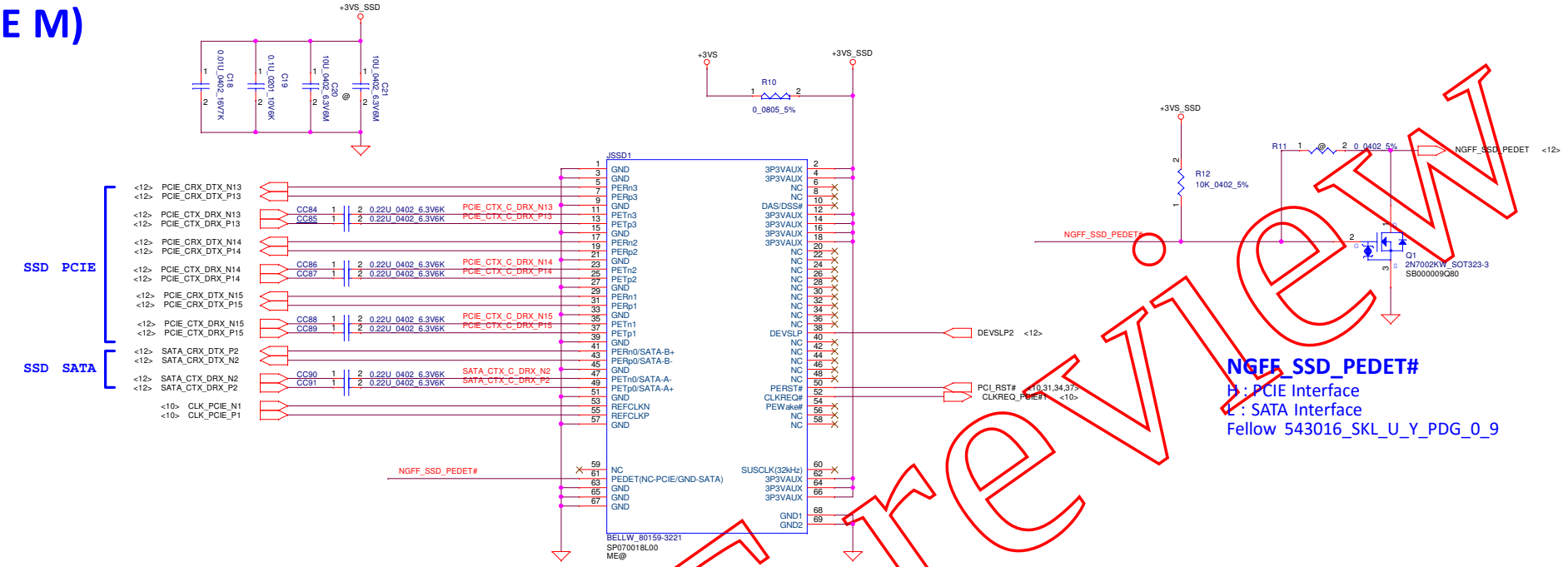
NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]



Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

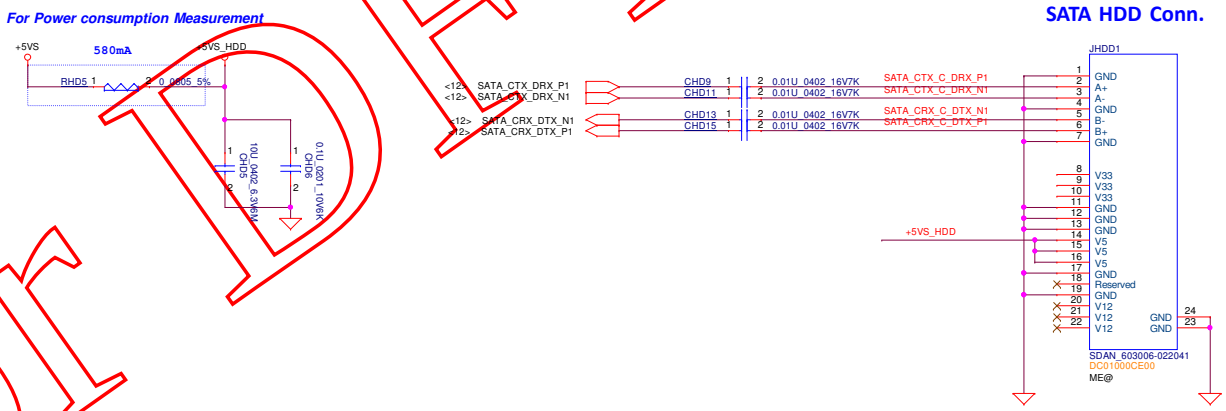
Compal Electronics, Inc.			
Title	NGFF WLAN / BT		
Size	Document Number		Rev
	LA-H102P		0.1
Date: Thursday, October 18, 2018	Sheet 31 of 51		

SSD(TYPE M)



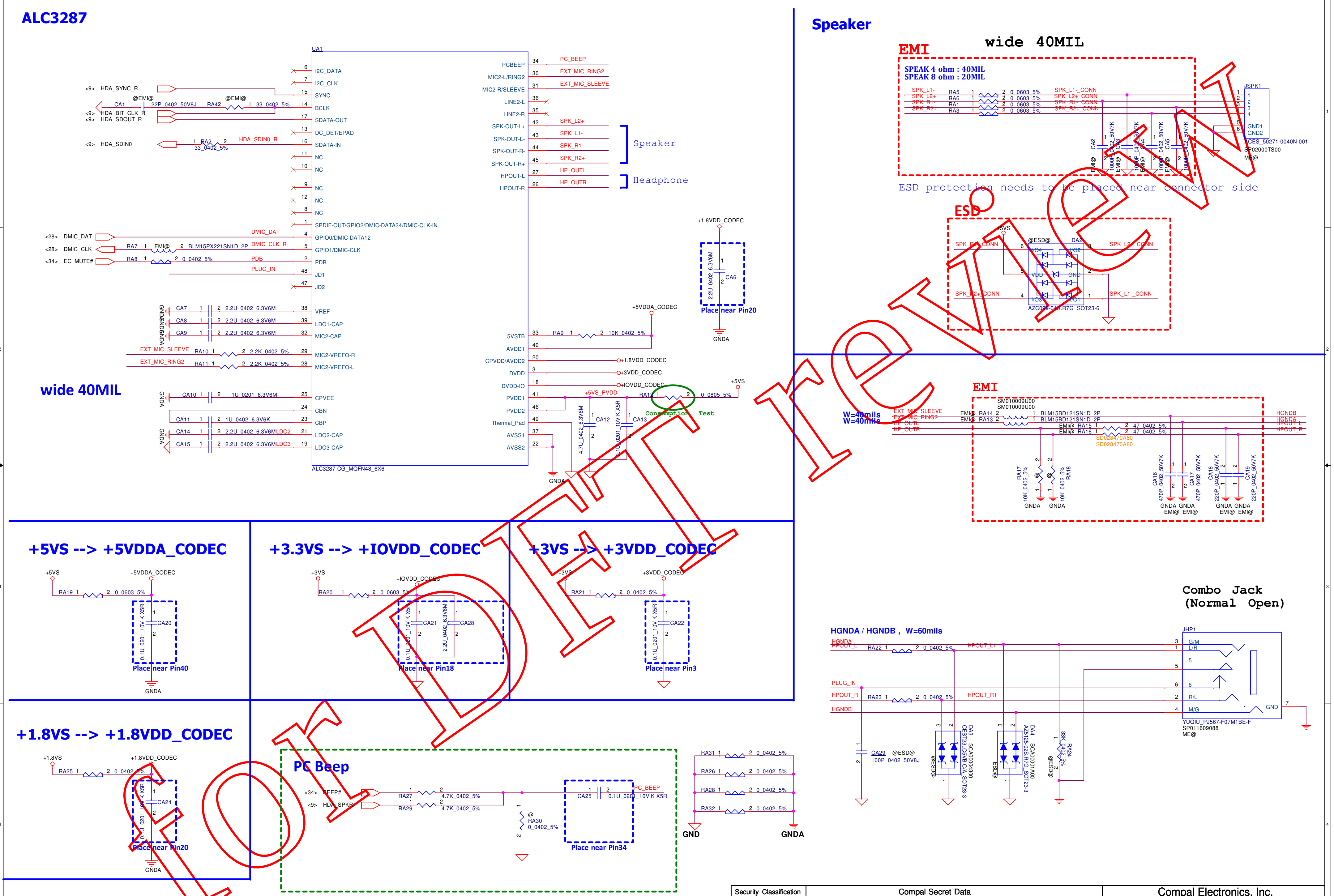
NGFF_SSD_PEDET#
H : PCIE Interface
L : SATA Interface
Fellow 543016_SKL_U_Y_PDG_0_9

SATA HDD

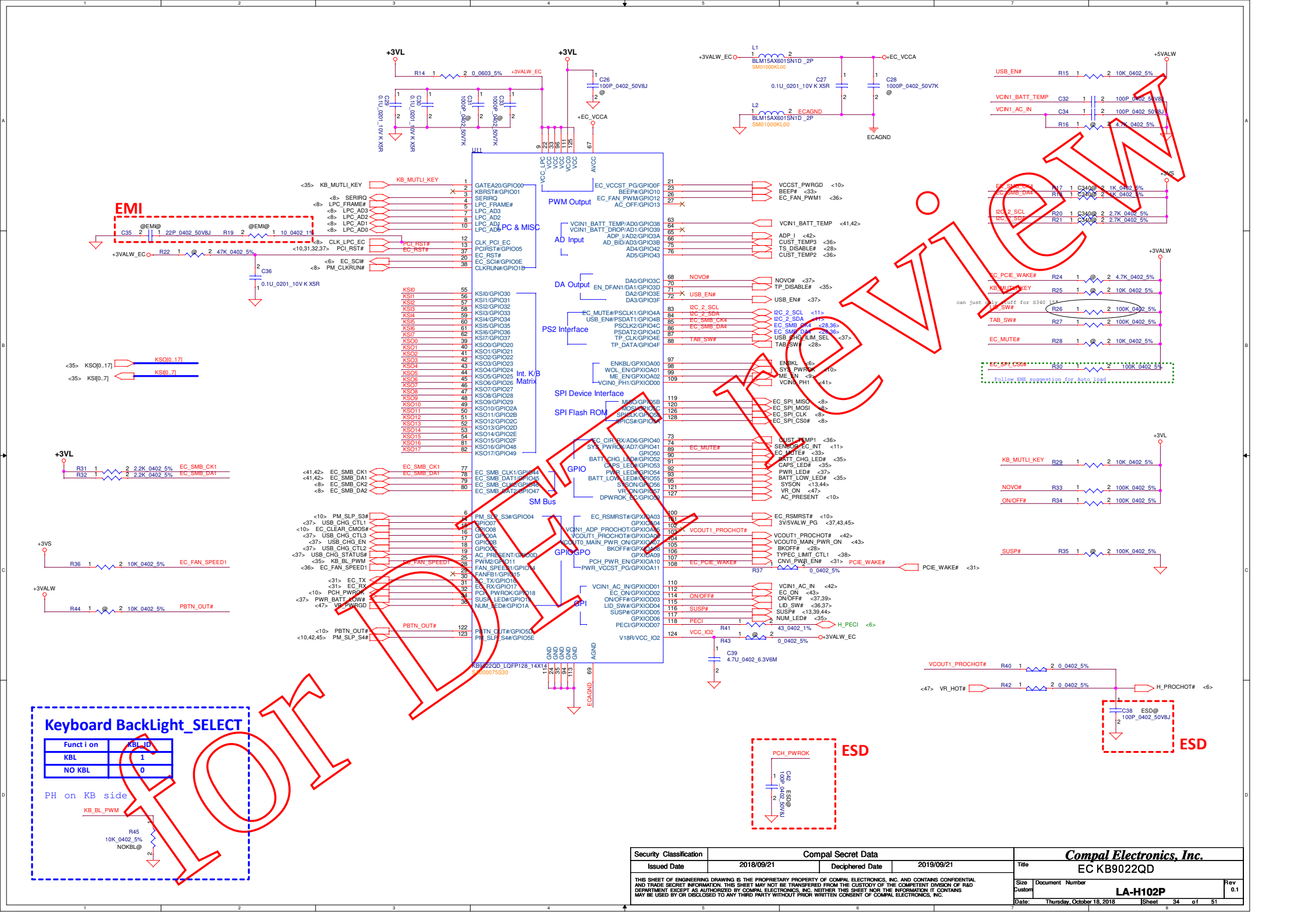


Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Compal Electronics, Inc.			
Title	SSD/HDD		
Size Custom	Document Number LA-H102P		Rev 0.1
Date: Thursday, October 18, 2018	Sheet 32 of 51		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/09/21	Deciphered Date 2019/09/21	Title: HD Audio Codec_ALC3287
			Size: Custom; Document Number: LA-H102P; Rev: 0.1
			Date: Thursday, October 18, 2018; Sheet 33 of 51


EMI
PC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPIO/GPO
GPI
ESD
ESD
Keyboard BackLight_SELECT
Funct i on
KBL_ID
KBL
1
NO KBL
0
PH on KB side
KB_BL_PWM
R45
10K_0402_5%
NOKBL@
Security Classification
Compal Secret Data
Issued Date
2018/09/21
Deciphered Date
2019/09/21
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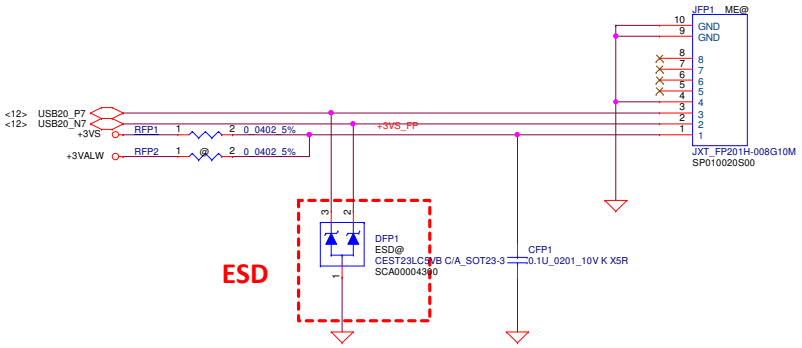
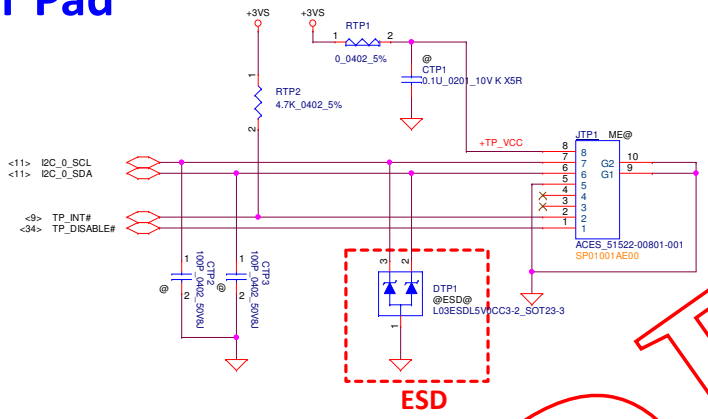
Size
Custom
Document Number
LA-H102P
Rev
0.1
Date:
Thursday, October 18, 2018
Sheet
34
of
51

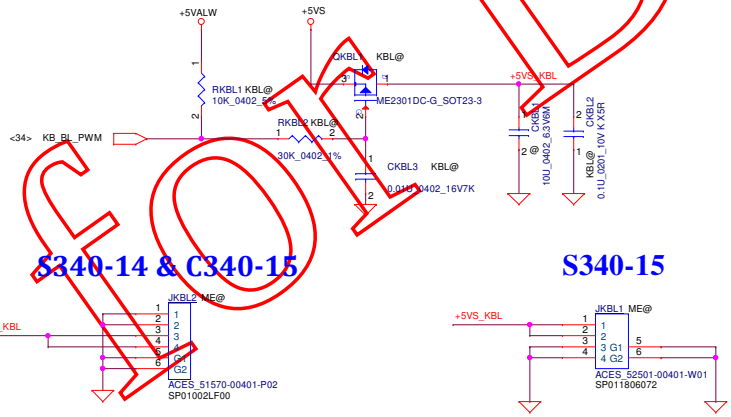
Finger printer



Touch Pad



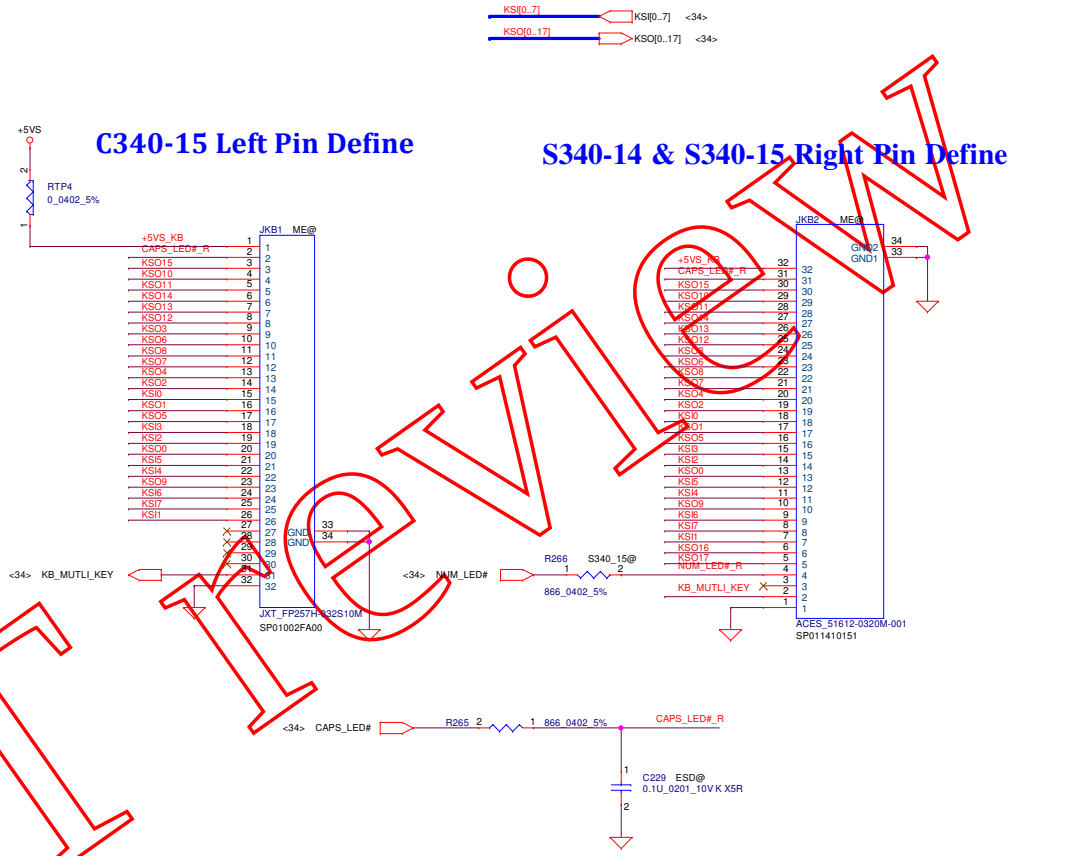
Keyboard Backlight



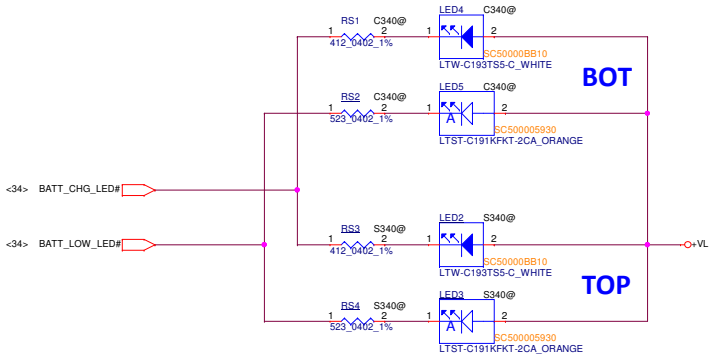
S340-14 & C340-15

S340-15

Keyboard



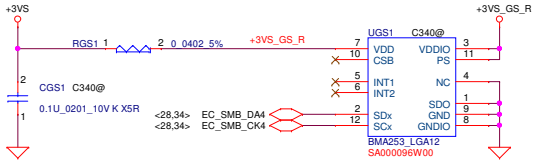
BATT LED



Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Compal Electronics, Inc.	
Title	KBL/KBD/LED/TP/HS Conn.
Size: Custom	Document Number: LA-H102P
Rev	0.1
Date: Thursday, October 18, 2018	Sheet 35 of 51

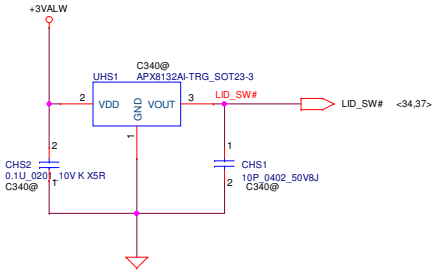
G-Sensor



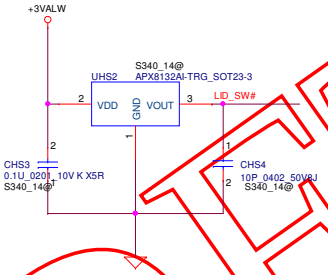
SMB Address: 0X18

Hall Sensor

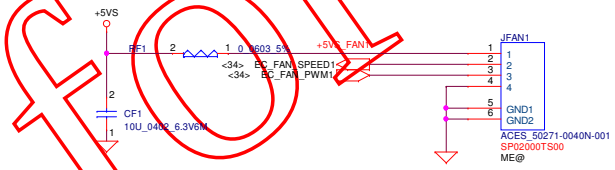
for C340



for S340 14"

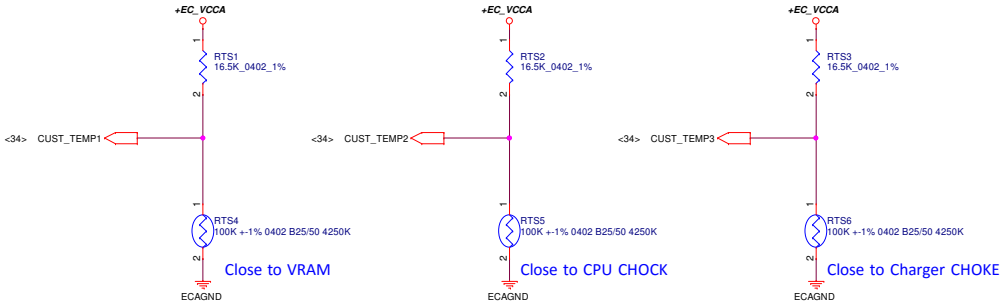


FAN



Thermal Sensor

THERMISTOR



Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

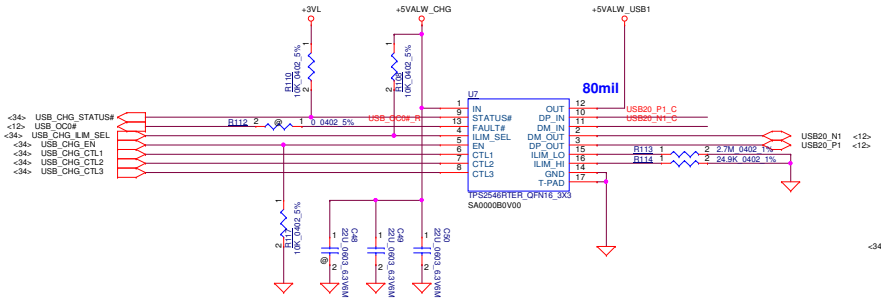
Compal Electronics, Inc.

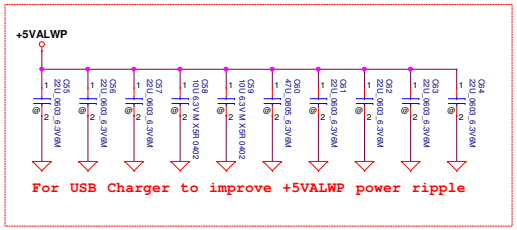
Title: FAN / Thermal Senser

Size	Document Number	Rev
Custom	LA-H102P	0.1

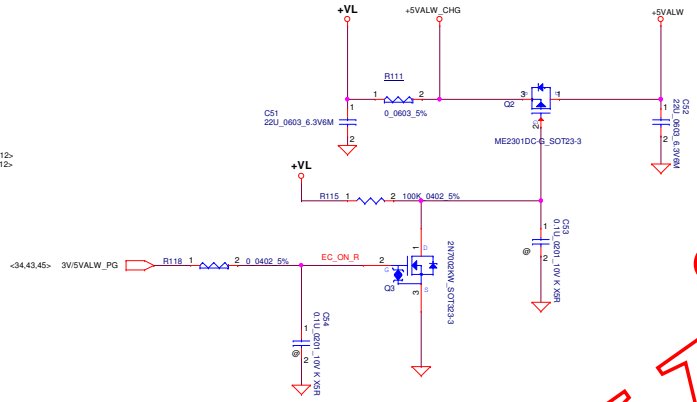
Date: Thursday, October 18, 2018 | Sheet 36 of 51

USB3.0_Port (AOU_Port)

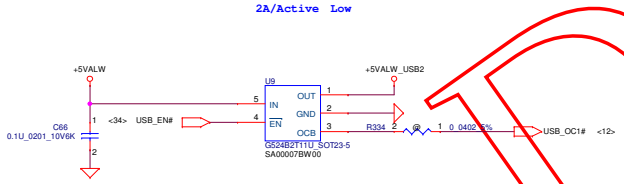


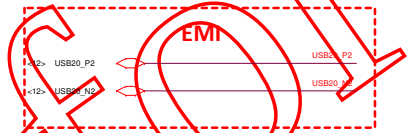


USB Charge switch

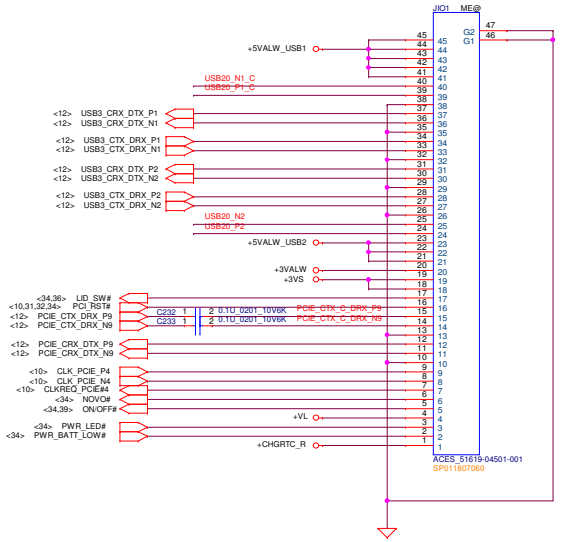


USB3.0_Port (Non-AOU_Port)





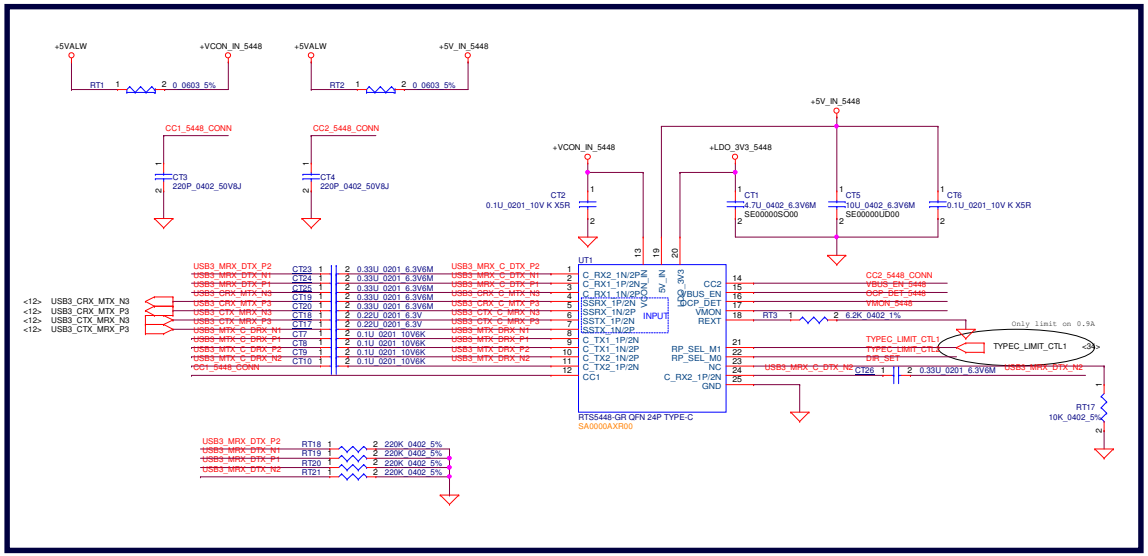
I/O CONN



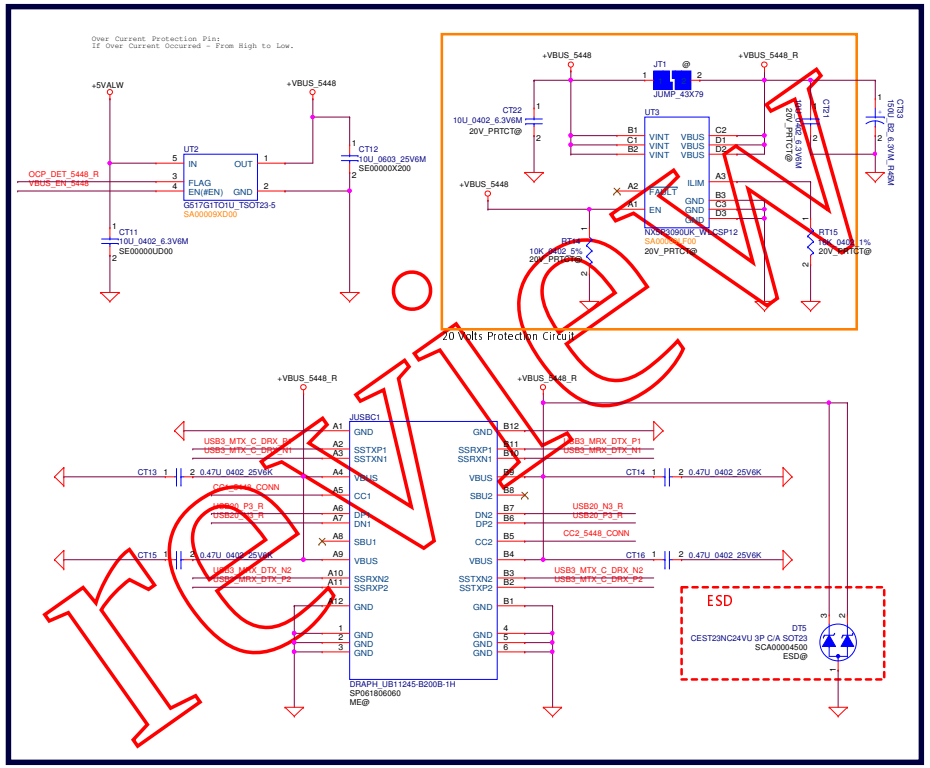
Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Compal Electronics, Inc.			
Title: IO board			
Size: Custom	Document Number: LA-H102P		Rev: 0.1
Date: Thursday, October 18, 2018	Sheet 37 of 51		

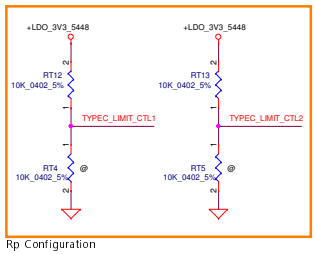
TYPE-C - CC+MUX (RTS5448-GR)



TYPE-C CONNECTOR

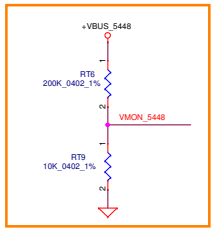


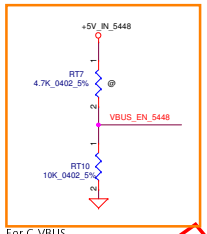
MUX MISC.



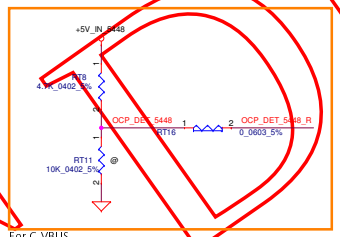
Rp Configuration

	M1	M0	Note
Rp:900mA	0	1	RT4/RT13 mount,RT12/RT5don't mount
Rp:1.5A	1	0	RT12/RT5 mount,RT4/RT13don't mount
Rp:3.0A	1	1	RT12/RT13mount,RT4/RT5 don't mount





For C_VBUS
(Power Switch Enable Pin)

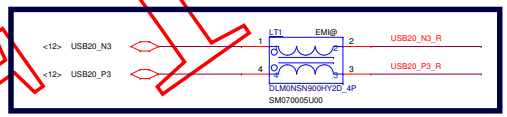


For C_VBUS
(Power Switch OCP Pin)

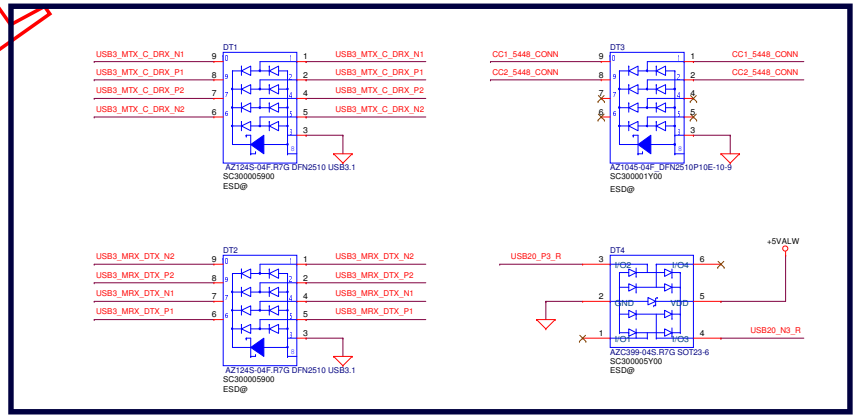
Power switch enable pin	Note
Low Active	RT7/RT10 mount
High Active	RT10 mount, RT7 don't mount

Power switch OCP pin	Note
Low Active	RT8/RT11 mount
High Active	RT11 mount, RT8 don't mount

USB2.0



ESD COMPONENTS



Security Classification	Compal Secret Data	
Issued Date	2018/09/21	Deciphered Date 2019/09/21

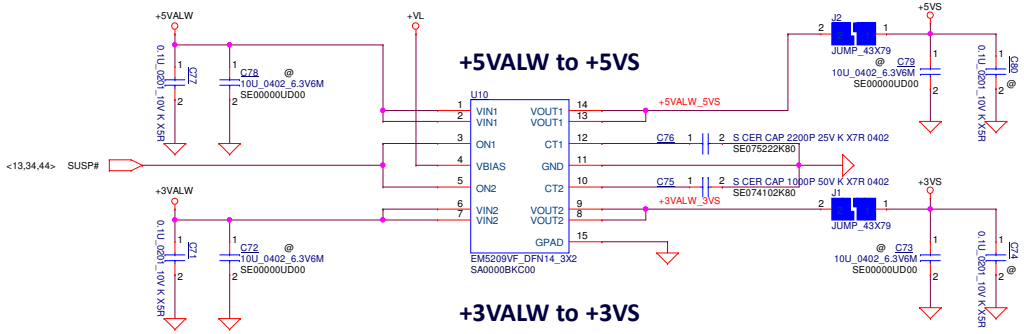
Compal Electronics, Inc.

Title: Type-C

Size: Custom | Document Number: LA-H102P | Rev: 0.1

Date: Thursday, October 18, 2018 | Sheet 38 of 51

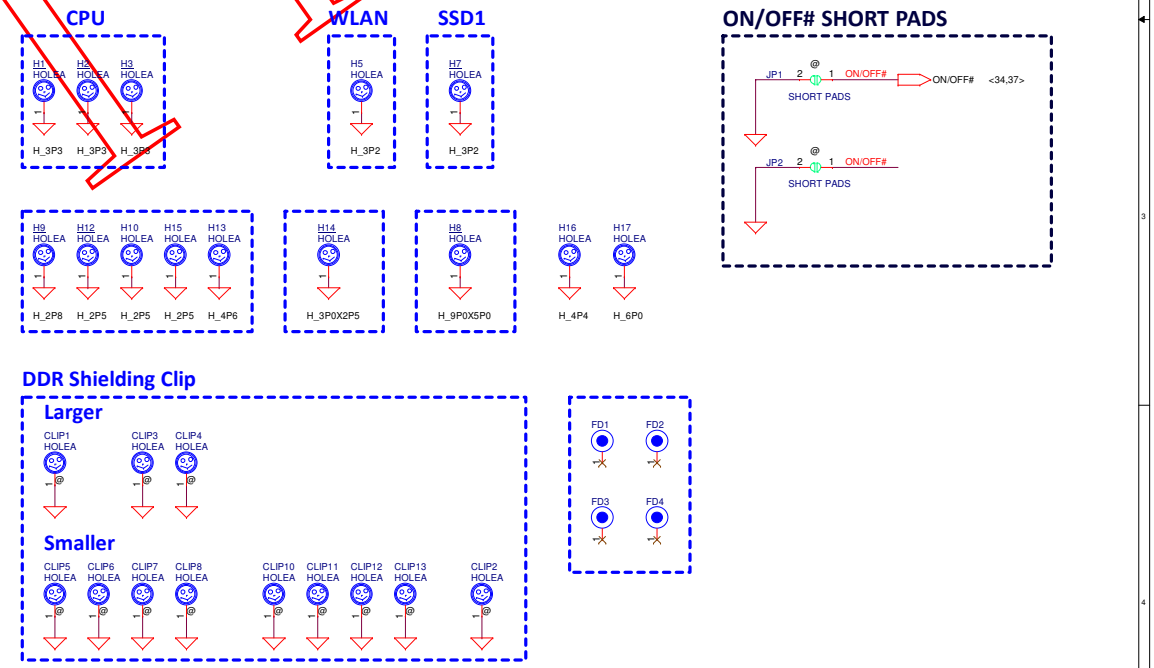
DC to DC



DISCHARGE CIRCUIT

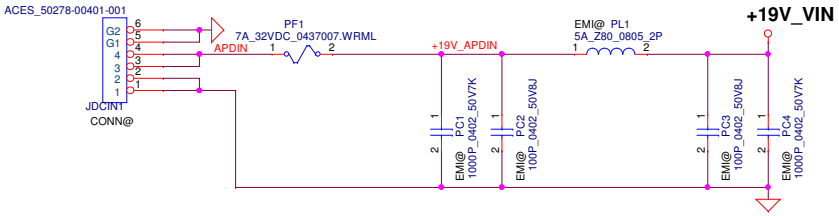
For +1.8VALW Discharge

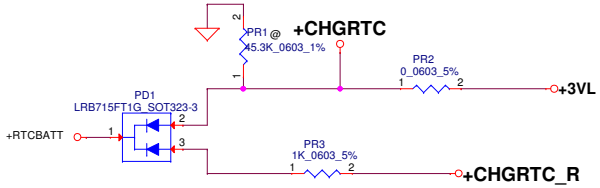
MISC.



Security Classification	Compal Secret Data		
Issued Date	2018/09/21	Deciphered Date	2019/09/21

Compal Electronics, Inc.			
Title	DC to DC / Discharge / MISC		
Size	Document Number		Rev
Custom	LA-H102P		0.1
Date:	Thursday, October 18, 2018	Sheet	39 of 51





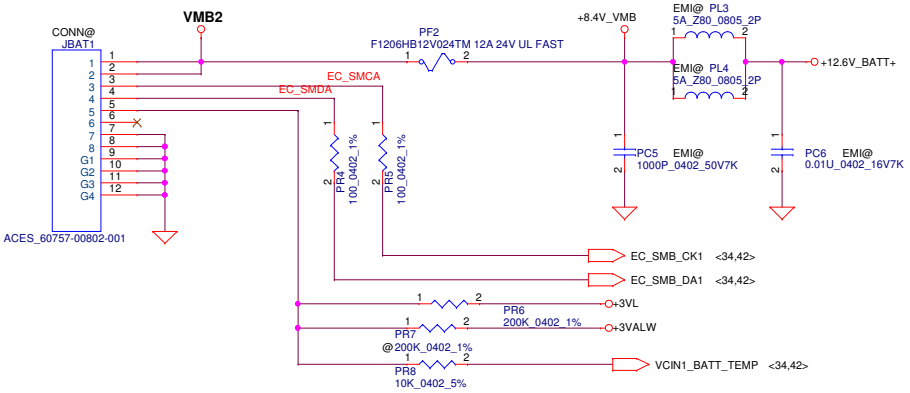
Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

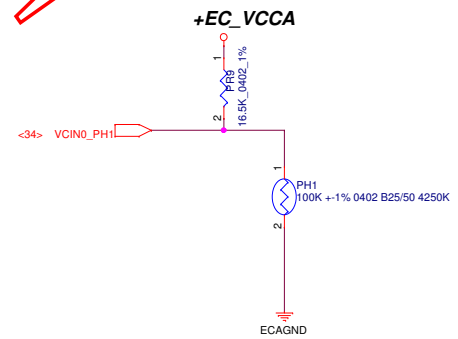
Title: **PWR- DCIN / Vin Detector**

Size	Document Number	Rev
Custom	KBL	0.1

Date: Thursday, October 18, 2018 Sheet 40 of 54



PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

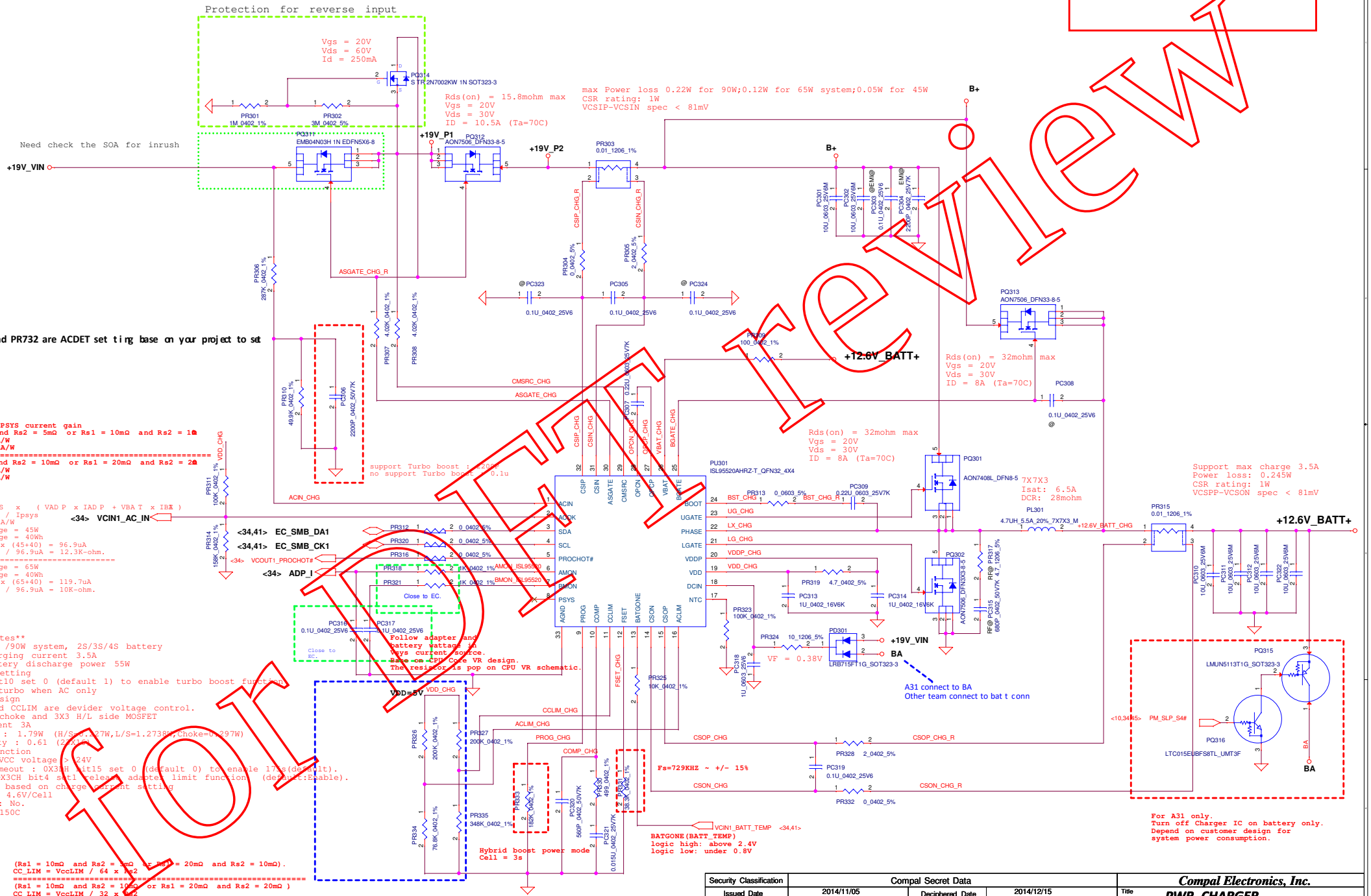
Title: **PWR- BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	KBL	0.1

Date: Thursday, October 18, 2018 Sheet 41 of 54

Module model information

ISL95520A_Hybrid_Boost_V2.mdd

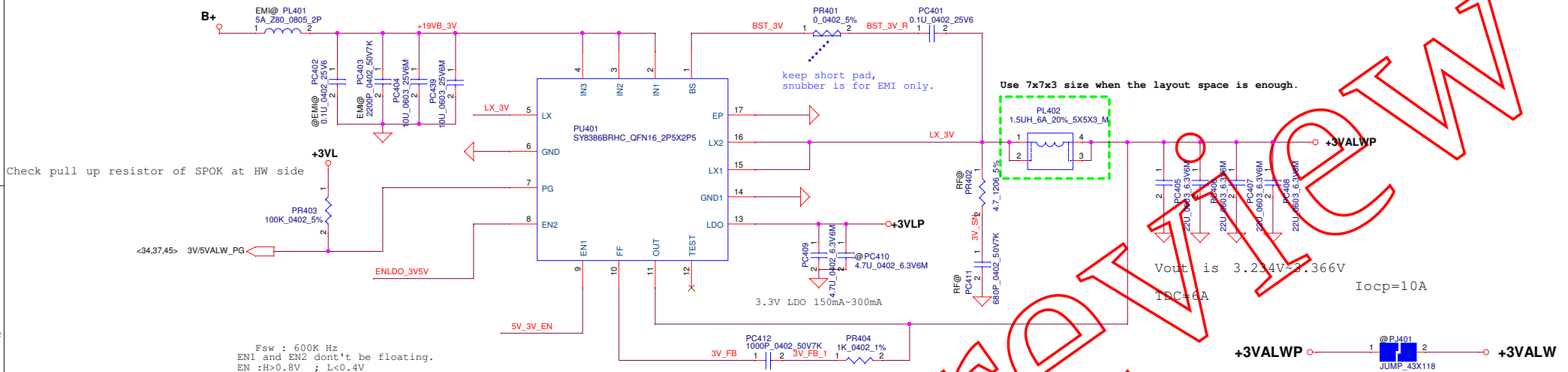


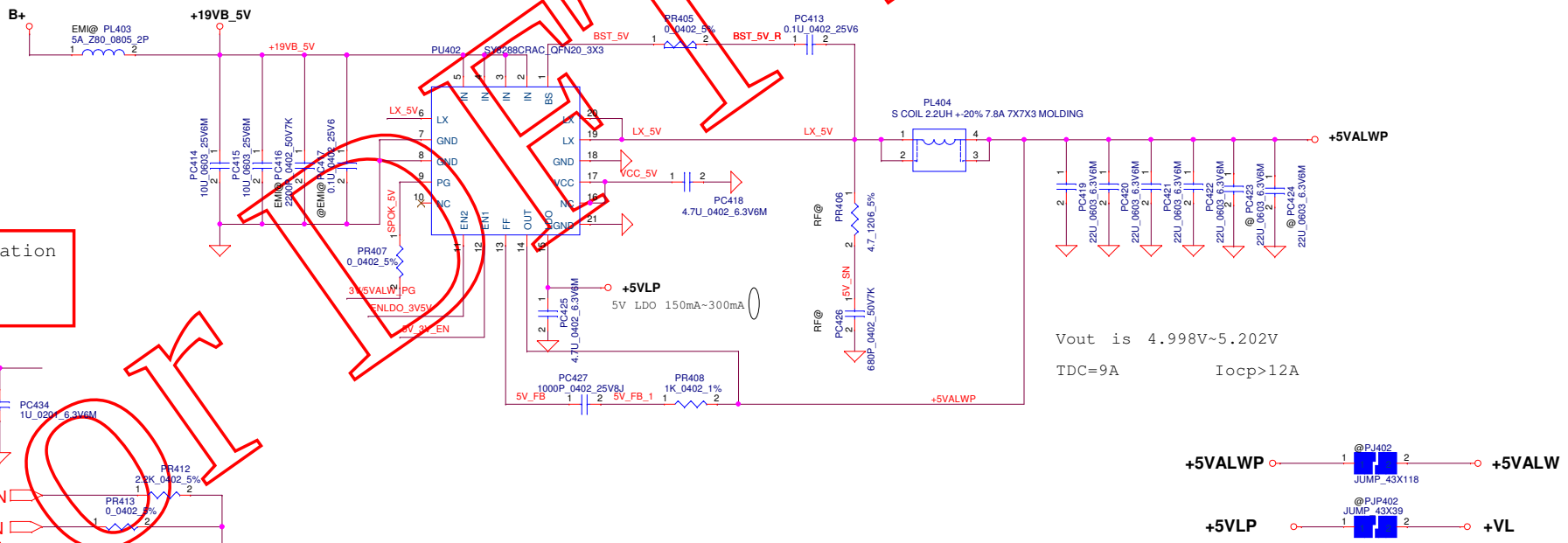
Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

Compal Electronics, Inc.			
Title	PWR_CHARGER		
Size	Document Number		Rev 0.1
Date: Thursday, October 18, 2018		Sheet 42 of 54	

Module model information

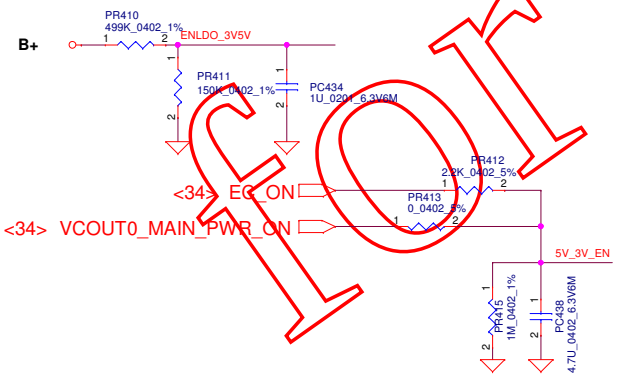
SY8286B_V3_single.mdd
SY8286B_V3_dual.mdd





Module model information

SY8286C_V3_single.mdd
SY8286C_V3_dual.mdd



Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size: Custom | Document Number | Rev: 0.1

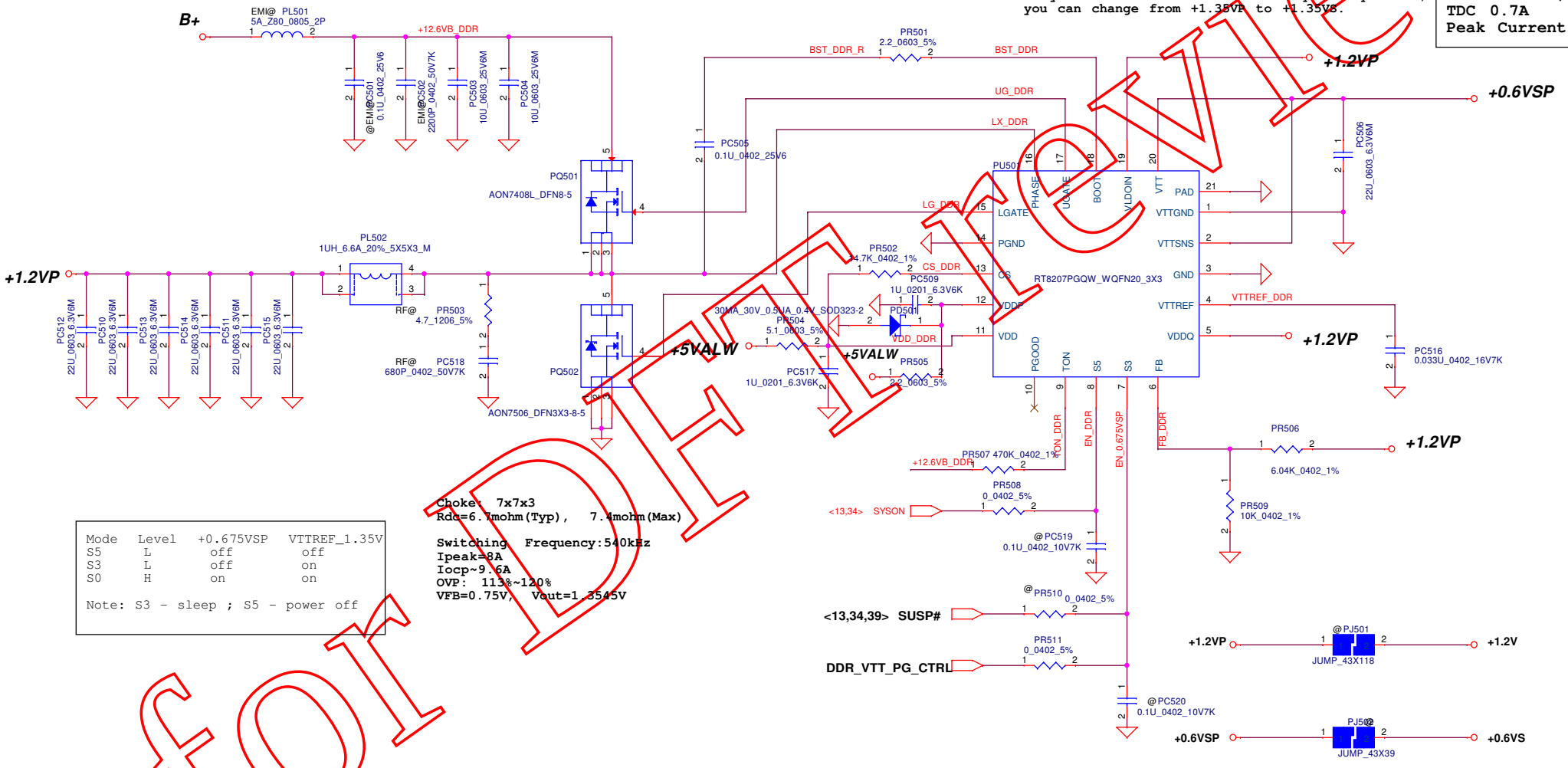
Date: Thursday, October 18, 2018 | Sheet 43 of 54

Module model information

RT8207P_single_V3.mdd For Single layer
RT8207P_dual_V3.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Choke: 7x7x3
Rdc=6.7mohm(Typ), 7.4mohm(Max)

Switching Frequency:540kHz
Ipeak=8A
Iocp~9.6A
OVP: 113%~120%
VFB=0.75V, Vout=1.3545V

Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

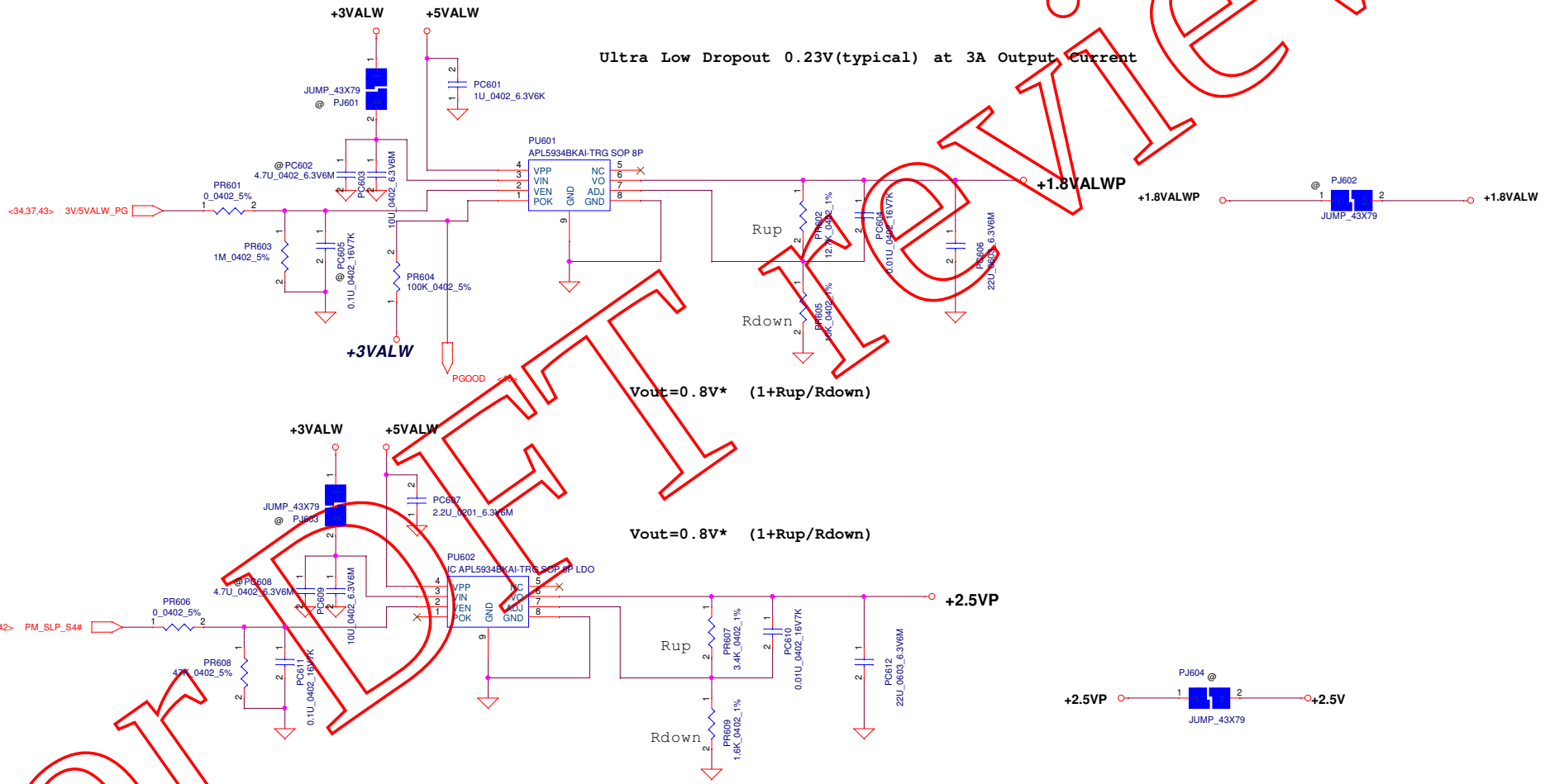
Title: RT8207P

Size: Custom | Document Number | Rev: 0.1

Date: Thursday, October 18, 2018 | Sheet 44 of 54

Module model information

APL5930_V2.mdd



Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

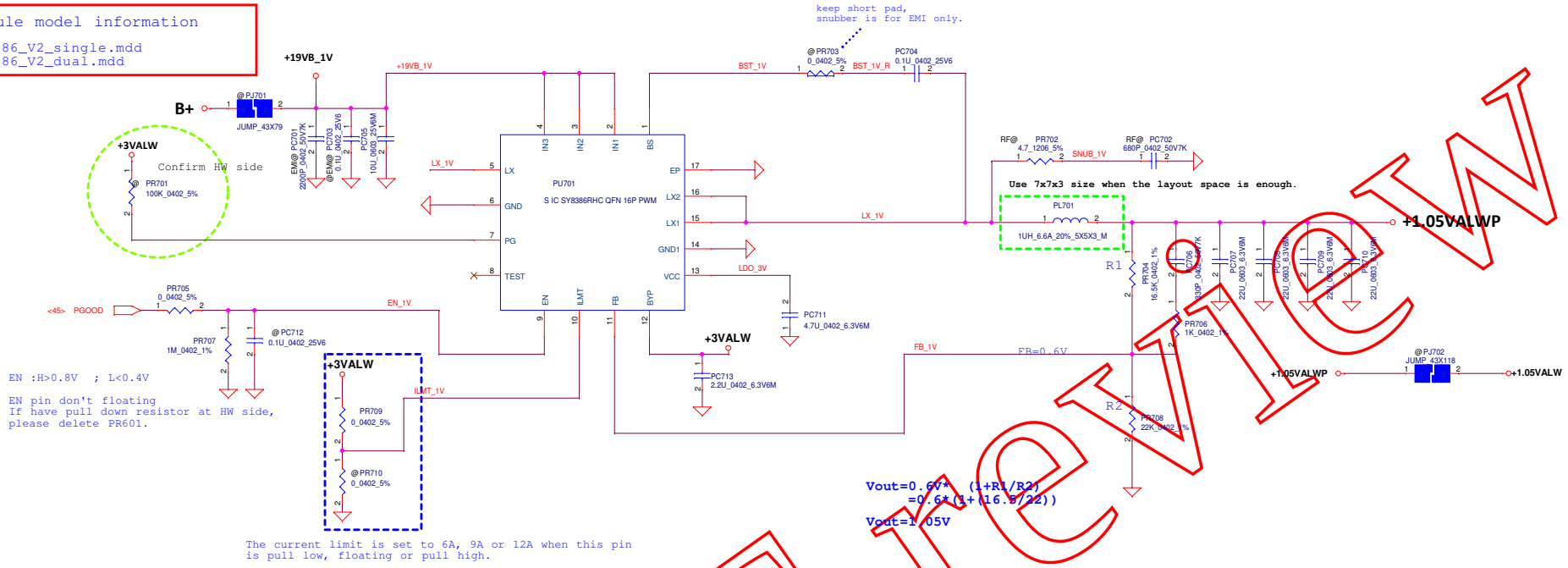
Title: APL5930

Size: Custom | Document Number: KBL | Rev: 0.1

Date: Thursday, October 18, 2018 | Sheet 45 of 54

Module model information

SY8286_V2_single.mdd
SY8286_V2_dual.mdd



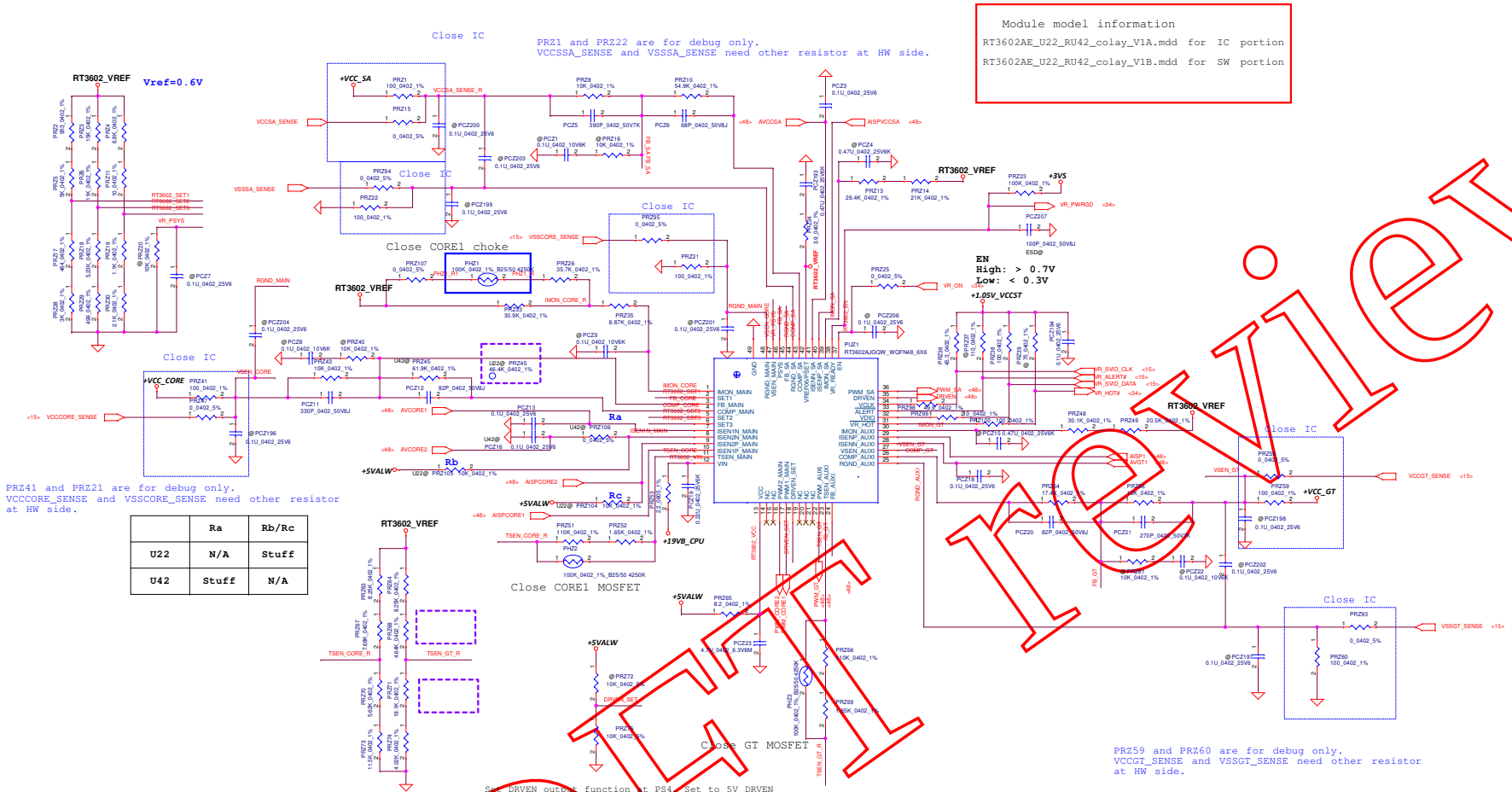
Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.

Title: SY8286

Size	Document Number	Rev
C		0.1

Date: Thursday, October 18, 2018 | Sheet 46 of 54



	Ra	Rb/Rc
U22	N/A	Stuff
U42	Stuff	N/A

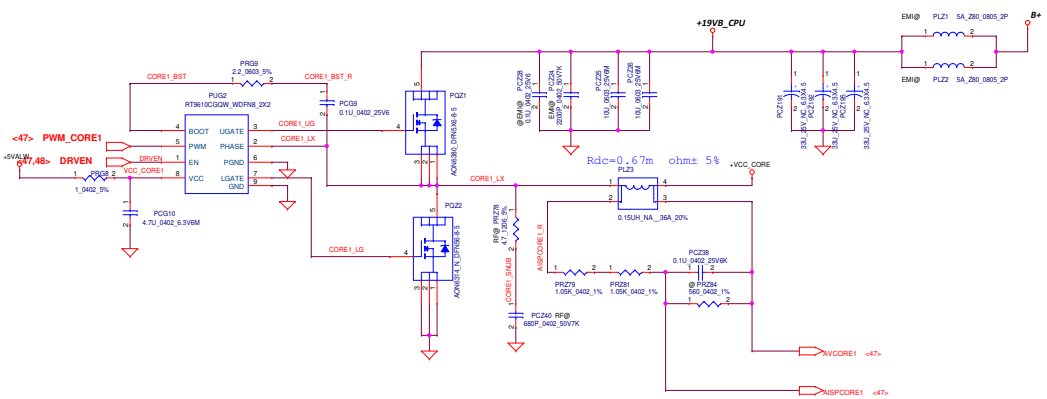
Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

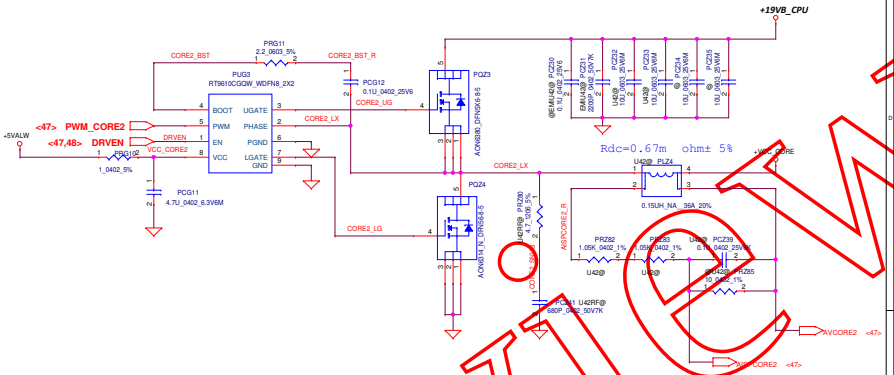
Compal Electronics, Inc.

Title: CPU_CORE

Size: | Document Number: | Rev: 0.2

Date: Thursday, October 18, 2018 | Sheet 47 of 54





H/S AON6280:
R DS(ON) (at V GS =10V) < 6.8m
R DS(ON) (at V GS =4.5V) < 10.5m

L/S AON6214:
R DS(ON) (at V GS =10V) < 2.8m
R DS(ON) (at V GS =4.5V) < 3.5m

VCC_CORE
FSW=450kHz
Choke=0.15uH
DCR=0.67 mohm +/- 5%

U22
LL=2.4 mohm
TDC=21A
ICCMAX=32A
OCP=40A

U42
LL=2.4 mohm
TDC=42A
ICCMAX=64A
OCP=70A

VCC_GT
FSW=450kHz
Choke=0.15uH
DCR=0.67 mohm +/- 5%

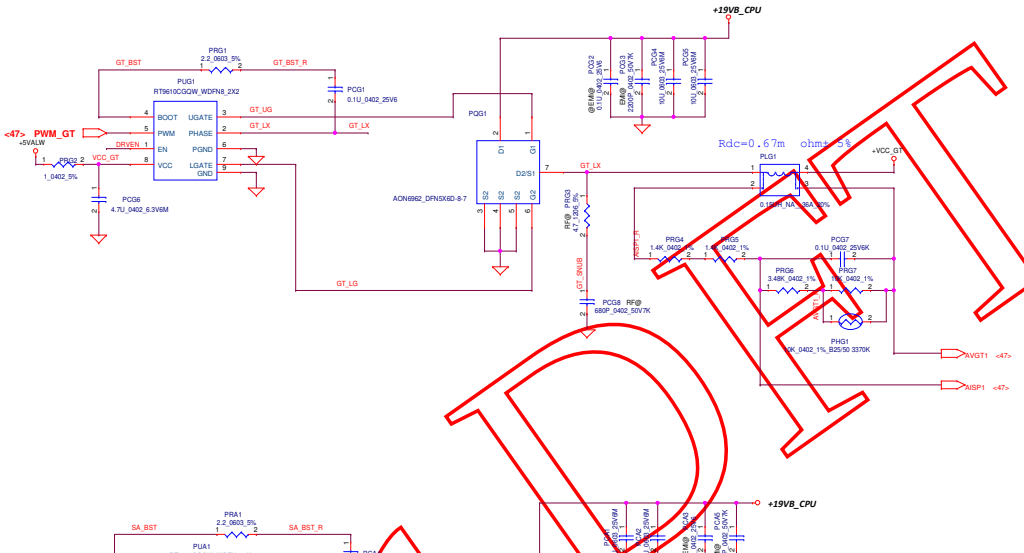
U22
LL=3.1 mohm
TDC=18A
ICCMAX=31A
OCP=39A

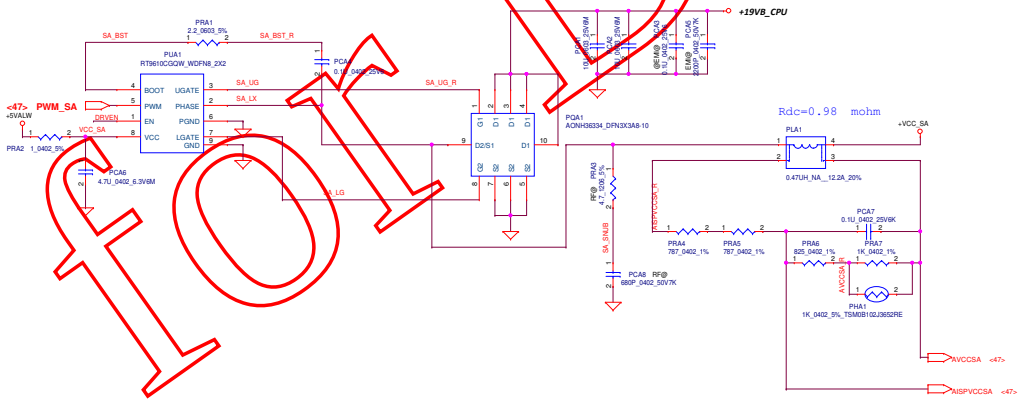
U42
LL=3.1 mohm
TDC=12A
ICCMAX=28A
OCP=39A

VCC_SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

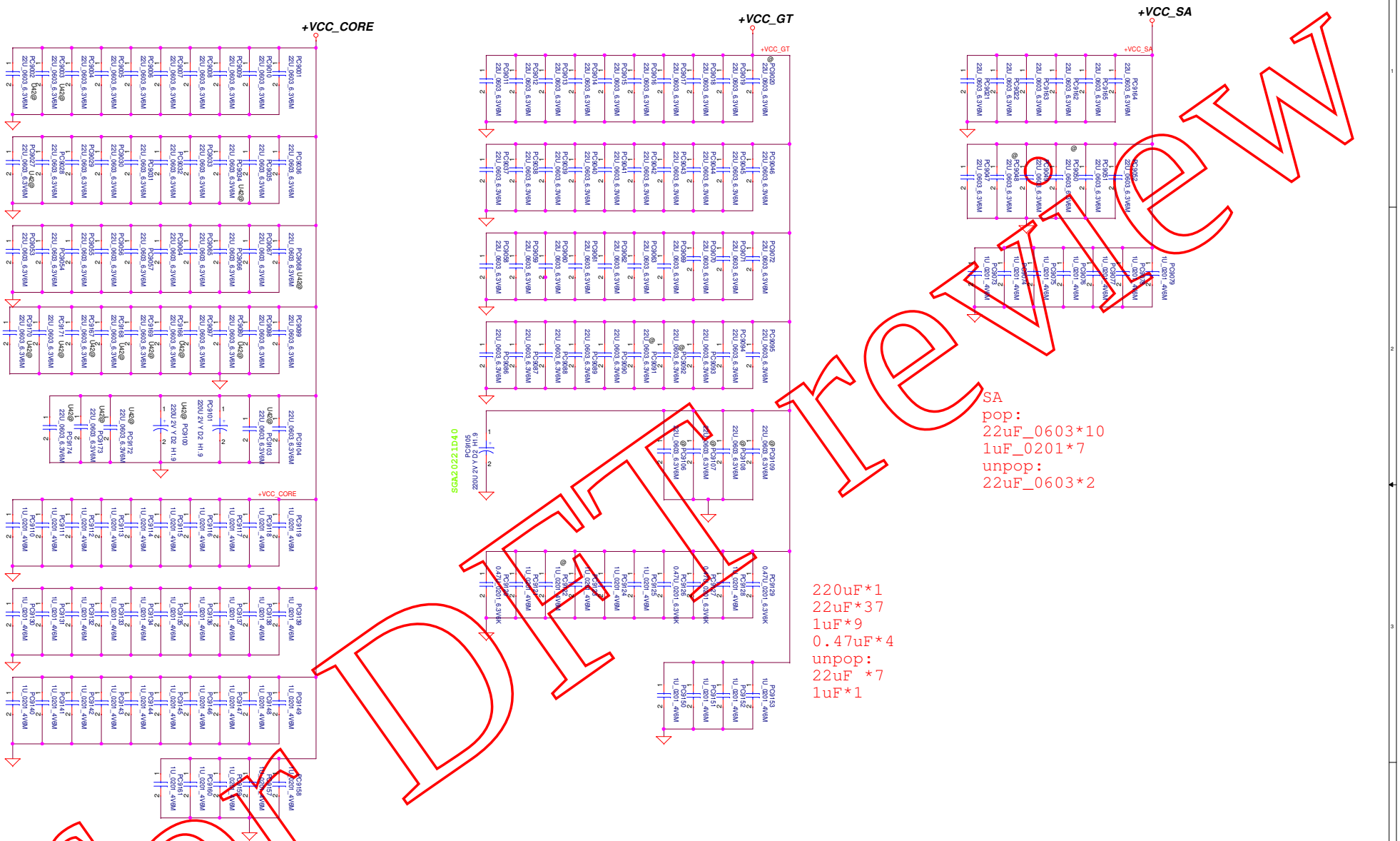
U22
LL=10.3 mohm
TDC=4A
ICCMAX=5A
OCP=10A

U42
LL=10.3 mohm
TDC=4A
ICCMAX=5A
OCP=10A





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/04/09	Deciphered Date	2019/04/09
Title	CPU Power stage		
Size	Document Number		Rev 0.1
Date: Thursday, October 18, 2018	Sheet 48 of 54		



Security Classification	Compal Secret Data		
Issued Date	2018/10/10	Deciphered Date	2018/11/04

Compal Electronics, Inc.			
Title: Power Train			
Size: C	Document Number: EH5AW M/B LA-G521P		Rev: 0.1
Date: Thursday, October 18, 2018	Sheet 49 of 54		

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	change 3V,5V BS 0 ohm to short pad		change PPR401 and PR405 to 0 ohm	0814	SIV
2	change DDR choke size from 7X7X3 to 5X5X3		change PL502 size to 5X5X3	0814	SIV
3	change VTT cap size to 0603		change PC506 to 22uF 0603	0820	SIV
4	change 1.8V and 2.5V to APL5934BKAI		change PU601and PU602 to APL5934BKAI	0820	SIV
5	Remove +0.6VSP cap PC507 PC508		Remove +0.6VSP cap PC507 PC508	0821	SIV
6	thermal test result		PU702 change from LDO to converter	0823	SIV
7	sourcer requirement		PC846 PC847 PC848 PC849 PC850 change to 0201	0824	SIV
8				0824	SIV
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					

Security Classification	Compal Secret Data		
Issued Date	2018/04/09	Deciphered Date	2019/04/09

Compal Electronics, Inc.		
Title	PIR (PWR)	
Size: Custom	Document Number: Z_BDW	Rev: 0.1
Date: Thursday, October 18, 2018	Sheet 52 of 54	

Version change list
(P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	ME request	0	Modify Hole to correct type	2018/03/23	EVT
2	Intel request		Reserve RC164, RC165 for CNVi		
3	ME request		Change smail Clip footprint		
4	Layout impact		Delete RF By-Pass / Cross Moat Caps		
5	Not support one-key battery function on USB		Delete USB_DETECT#		
6	Common design		Swap PCIE between WALN and HDD		
7	Intel DDR request		Add CU25		
8	Follow FAN SPEC		Change FAN connector pin define		
9	EMI request		CA23,CA27 change to RA31,RA32		
10	EMI request		RA7 change PN to SM01000NY00		
11	NV request		UV20.5 change to +1.8VGS_+3VGS_AON		
12	Customer request		Add P29-HDMI Level shifter_PS8407A		
13	ME request		Add UHS1,CHS1,CHS2 and modify JIO1 pin define		
14	Layout request		Swap DDR pin define		
15	Intel request		Modify RC17 value		
16	ME request		Add LED2,RS4		
17	SW request		WL_OFF# change to GPP_E4		
18	Common request		Modify JIO1,JEDP1 pin define for S/B layout, add R330~R3332 and delete D2		
19	HW request		Modify R113,R114 value		
20	Layout request		Delete H16		
21	ME request		Add LED3 and change LED2		
22					
23					
24					
25					
26					
27					
28					
29					
30					
31					

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/09/21	Deciphered Date	2019/09/21
Title	PIR (HW)		
Size: Custom	Document Number: LA-H102P		Rev: 0.1
Date: Thursday, October 18, 2018	Sheet 53 of 51		