

LV530 KBL/ SKL Schematics

Kabylake-U U22 / U2+3e / U42

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
 For the value, it can be read by the number before R. (R means resistor)
 For the tolerance, it can be read from the last letter.
 For the rating, we don't show on the symbol name.
 For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

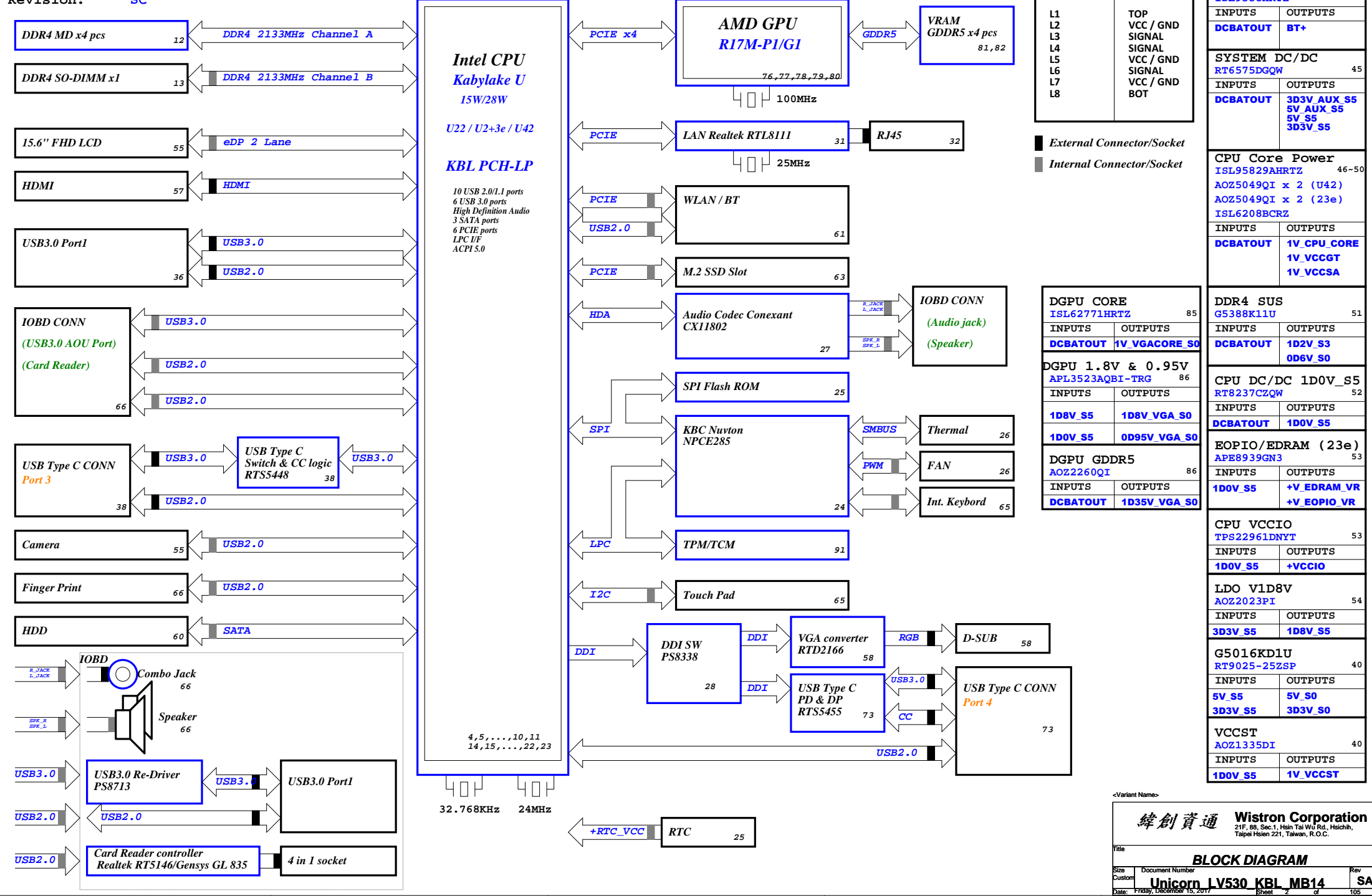
The naming rule is
 Capacitor type + value + rating + size + tolerance + material
 SCD1U10V2MX-1
 SC=> SMT Ceremic, TC=> POS cap or SP cap
 D1U => 0.1uF
 10V => the voltage rating is 10V
 2=> 0402, 3=>0603, 5=>0805
 M=>tolerance M, K, Z
 X=> X7R/X5R, Y=> Y5V
 -1 => symbol version, nonsense to EE characteristic

DY	DUMMY
DY-EMC	Follow EMC team request (SDV DY)
EMC-TVS	SDV : ASM FVT&SIT : By SKU (SKU1 DY / SKU2 ASM)
EMC-TEST	For EMC team SDV test (SDV : ASM)
23e	U2+3e only
U42	U42 only
NON-U42	U22 or U2+3e
UMA	UMA only
PX	Discrete only

<Variant Name>

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COVER PAGE	
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LV315 KBL-U Block Diagram



PCB LAYER	
L1	TOP
L2	VCC / GND
L3	SIGNAL
L4	SIGNAL
L5	VCC / GND
L6	SIGNAL
L7	VCC / GND
L8	BOT

External Connector/Socket
 Internal Connector/Socket

CHARGER	
ISL9538HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC	
RT6575DGQW 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

CPU Core Power	
ISL95829AHRTZ 46-50	
AOZ5049QI x 2 (U42) AOZ5049QI x 2 (23e) ISL6208BCRZ	
INPUTS	OUTPUTS
DCBATOUT	1V_CPU_CORE 1V_VCCGT 1V_VCCSA

DDR4 SUS	
G5388K11U 51	
INPUTS	OUTPUTS
DCBATOUT	1D2V_S3 0D6V_S0

CPU DC/DC 1D0V_S5	
RT8237CZQW 52	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

EOPPIO/EDRAM (23e)	
APE8939GN3 53	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5 +V_EDRAM_VR +V_EOPPIO_VR

CPU VCCIO	
TPS22961DNYT 53	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5 +VCCIO

LDO V1D8V	
AOZ2023PI 54	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 1D8V_S5

G5016KD1U	
RT9025-25ZSP 40	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 5V_S0 3D3V_S0

VCCST	
AOZ1335DI 40	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5 1V_VCCST

DGPU CORE	
ISL62771HRTZ 85	
INPUTS	OUTPUTS
DCBATOUT	1V_VGACORE_S0

DGPU 1.8V & 0.95V	
APL3523AQBI-TRG 86	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S5 1D8V_VGA_S0 1D0V_S5 0D95V_VGA_S0

DGPU GDDR5	
AOZ2260QI 86	
INPUTS	OUTPUTS
DCBATOUT	1D35V_VGA_S0

Main Func = CPU

(Blank)

<Variant Name>

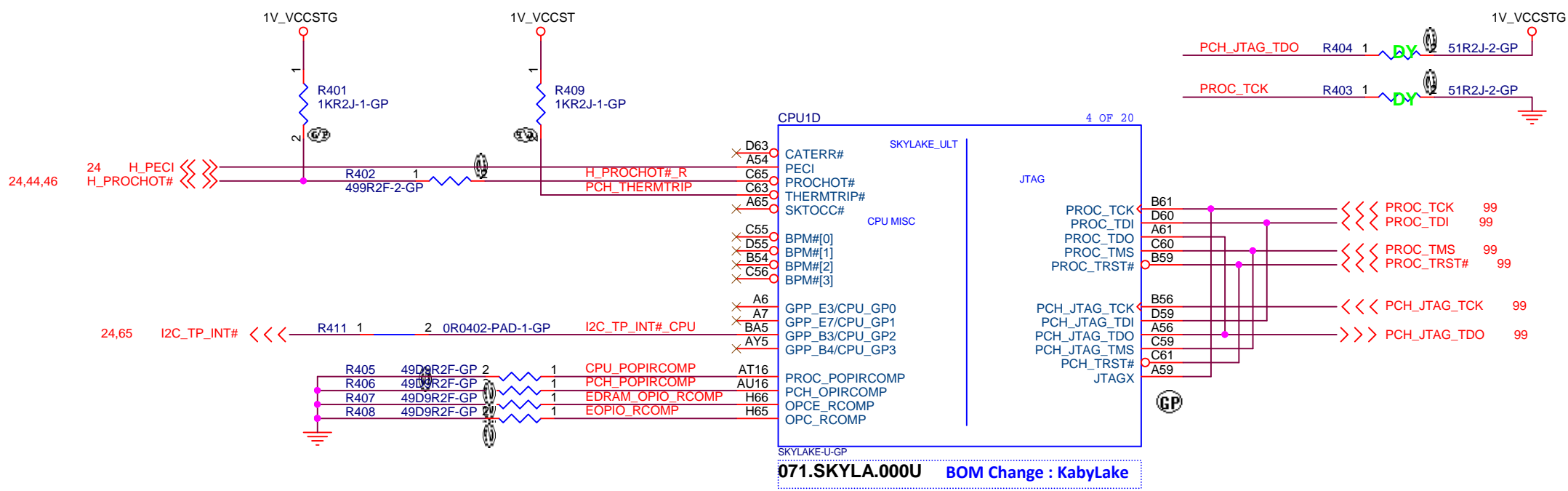
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RESERVED		
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Size A4	Document Number Unicorn LV530 KBL MB GA	Rev GA
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Main Func = CPU



<Variant Name>

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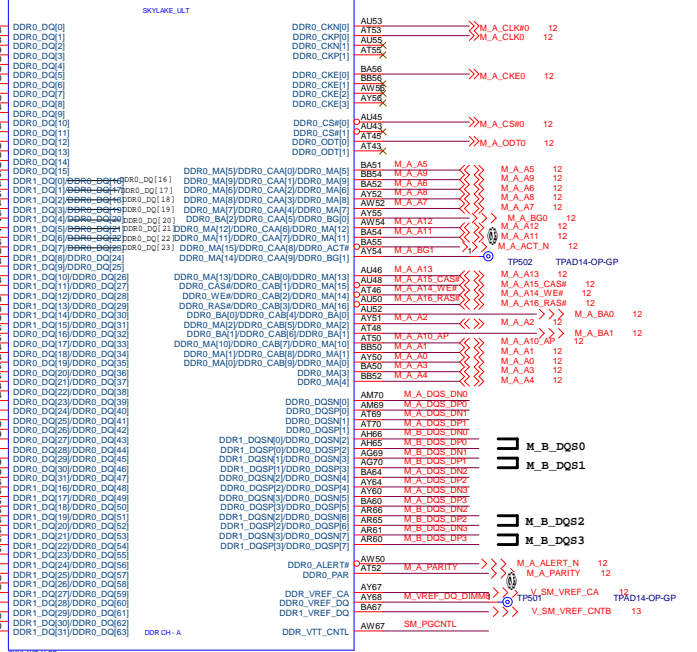
Title: **CPU (JTAG/CPU SIDE BAND)**

Size: A4 Document Number: **Unicorn LV530_KBL_MB14** Rev: SA

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M_A_BGL, M_VREF_DQ_DIMMO Reserve Testpoint only

CPUHB 2 OF 33



CPUHC 3 OF 33

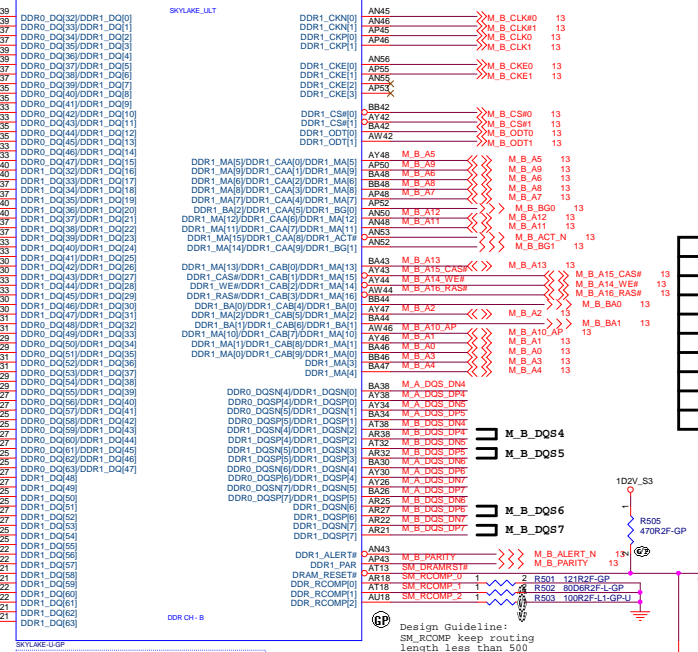
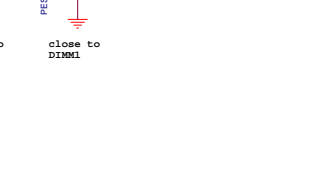
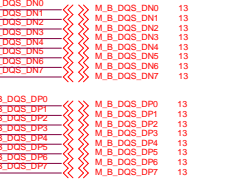
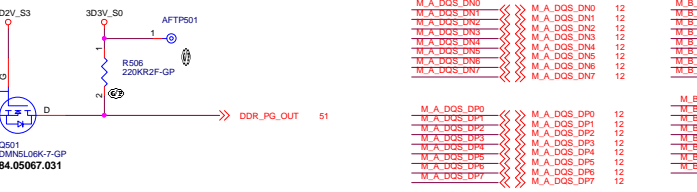


Table with 2 columns: Pin Name, Pin Number. Rows include M_B_A14, M_B_A15, M_B_A16, M_B_A17, M_B_A18, M_B_A19, M_B_A20, M_B_A21, M_B_A22, M_B_A23, M_B_A24, M_B_A25, M_B_A26, M_B_A27, M_B_A28, M_B_A29, M_B_A30, M_B_A31, M_B_A32, M_B_A33, M_B_A34, M_B_A35, M_B_A36, M_B_A37, M_B_A38, M_B_A39, M_B_A40, M_B_A41, M_B_A42, M_B_A43, M_B_A44, M_B_A45, M_B_A46, M_B_A47, M_B_A48, M_B_A49, M_B_A50, M_B_A51, M_B_A52, M_B_A53, M_B_A54, M_B_A55, M_B_A56, M_B_A57, M_B_A58, M_B_A59, M_B_A60, M_B_A61, M_B_A62, M_B_A63, M_B_A64, M_B_A65, M_B_A66, M_B_A67, M_B_A68, M_B_A69, M_B_A70, M_B_A71, M_B_A72, M_B_A73, M_B_A74, M_B_A75, M_B_A76, M_B_A77, M_B_A78, M_B_A79, M_B_A80, M_B_A81, M_B_A82, M_B_A83, M_B_A84, M_B_A85, M_B_A86, M_B_A87, M_B_A88, M_B_A89, M_B_A90, M_B_A91, M_B_A92, M_B_A93, M_B_A94, M_B_A95, M_B_A96, M_B_A97, M_B_A98, M_B_A99, M_B_A100.

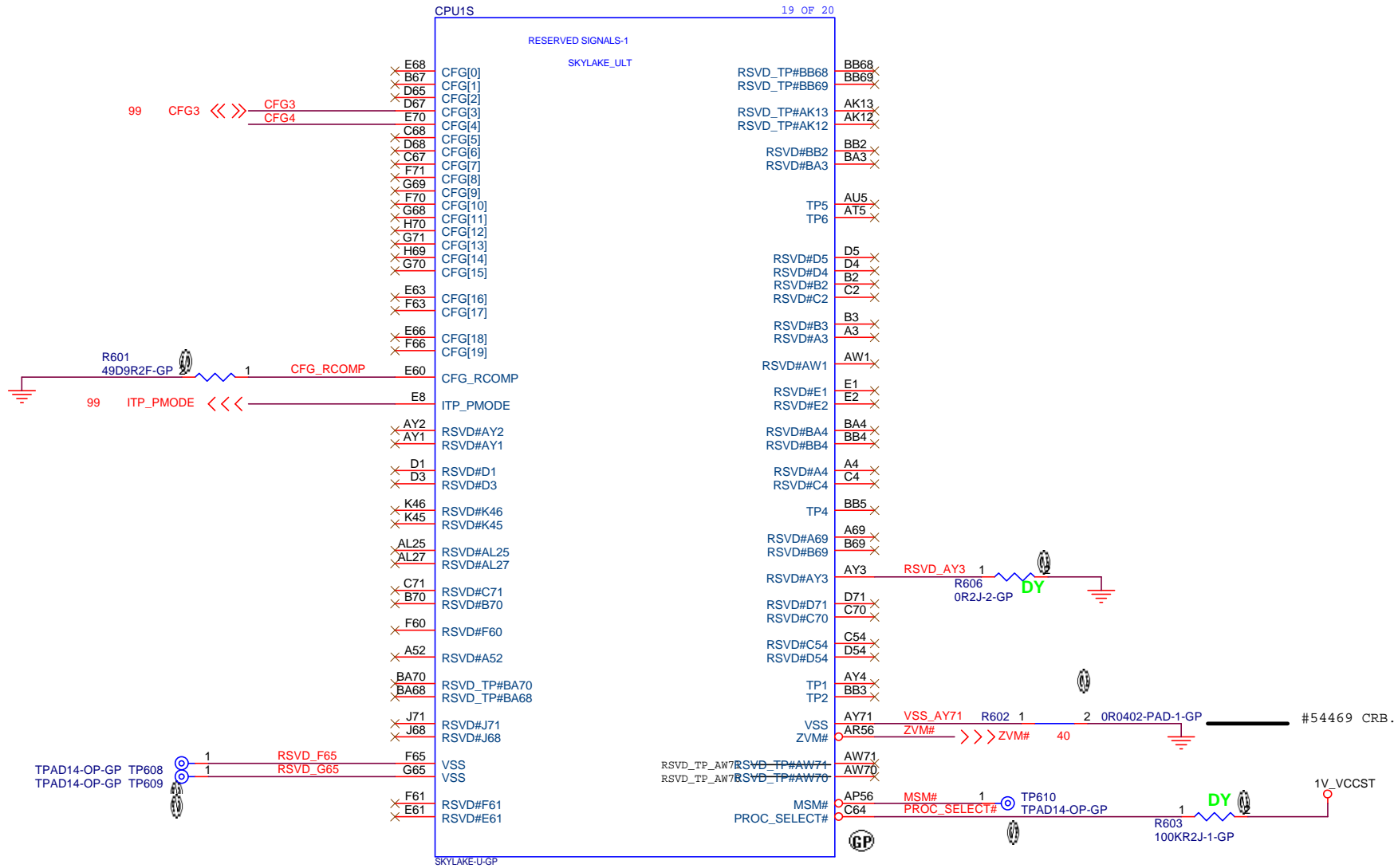
071.SKYLA.000 BOM Change : KabyLake

071.SKYLA.000 BOM Change : KabyLake



Wistron Corporation logo and address: 21F, 8F, Sec. 1, Hsinchu, Taipei Hsein 221, Taiwan, R.O.C. Product name: CPU (DDR). Customer: Unicorn_LV530_KBL_MB14. Date: Friday, December 15, 2017. Sheet 5 of 105.

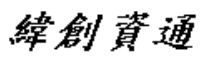
Main Func = CPU

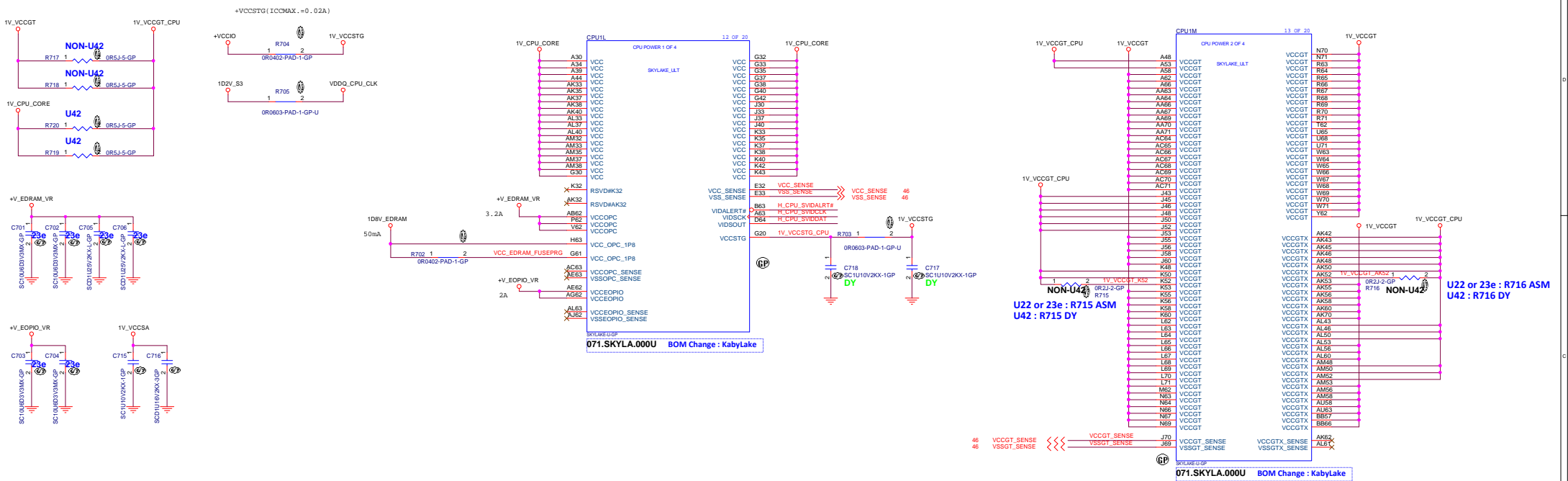


071.SKYLA.000U BOM Change : KabyLake

[559100]
 CFG[3]: Reserved configuration lane.
 CFG[4]: eDP enable:
 1 = Disabled.
 0 = Enabled.

<Variant Name>

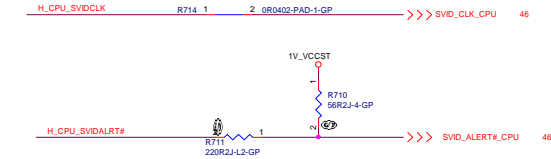
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CPU (CFG)	
Size	Document Number
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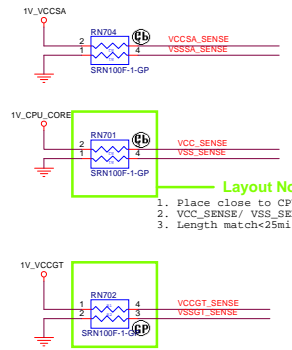
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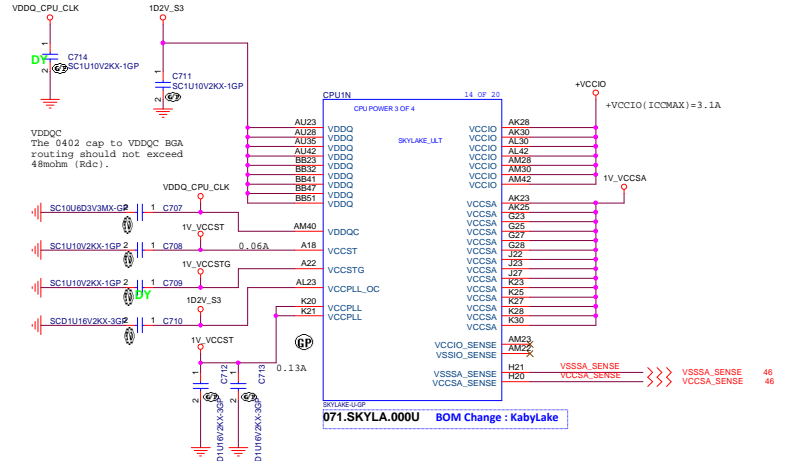
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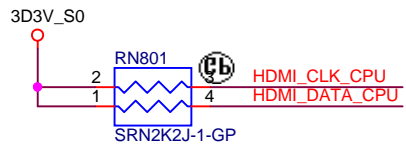
Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.



Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil



Main Func = CPU



HDMI

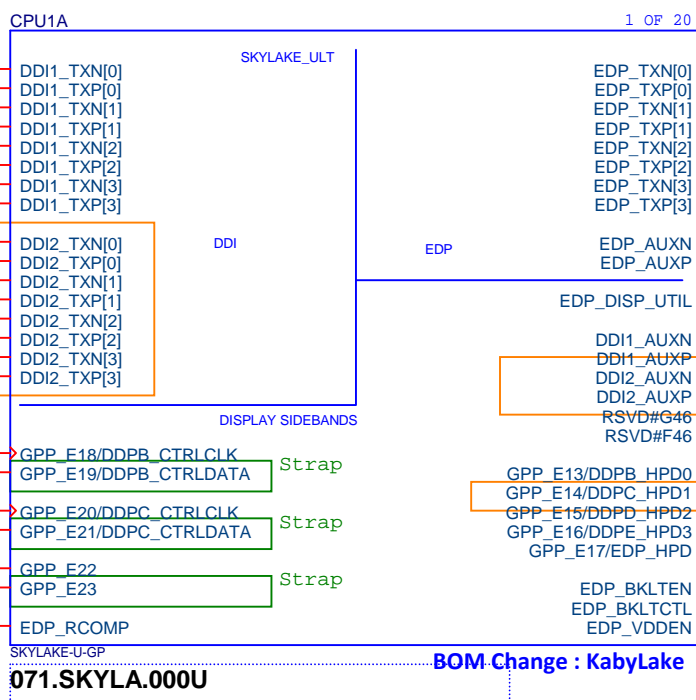
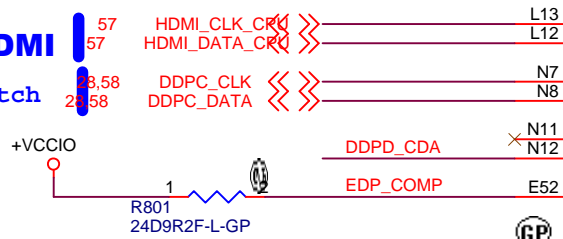
20170413
different with BOHO

DDI Switch Type C PD, DSUB



HDMI

DDI Switch



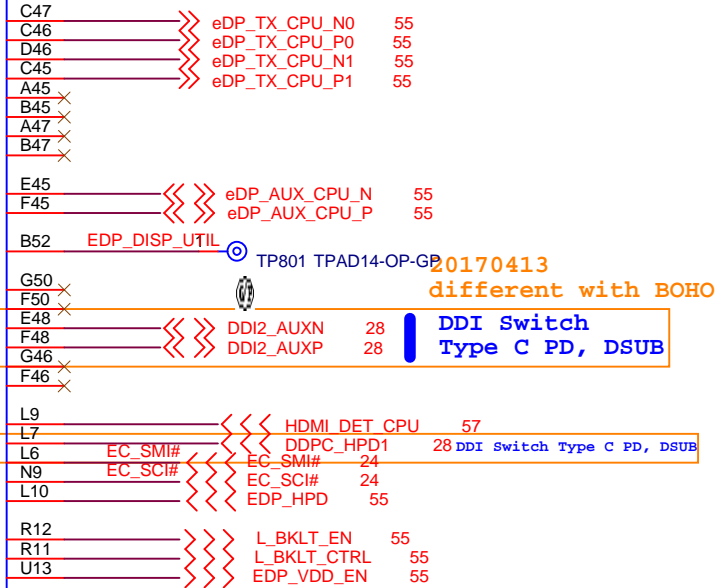
BOM Change : KabyLake

[561280] eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	5 mils	25 mils	24.9 Ω ±1%	Max = 600 mils

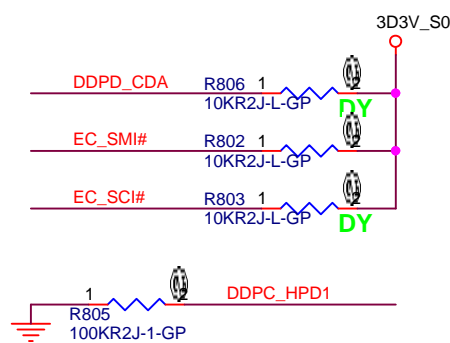
[561280] DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC



20170413
different with BOHO

DDI Switch Type C PD, DSUB



<Variant Name>

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Title: **CPU (DDI/EDP)**

Size A4 Document Number: **Unicorn LV530_KBL_MB14** Rev: **SA**

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Main Func = CPU

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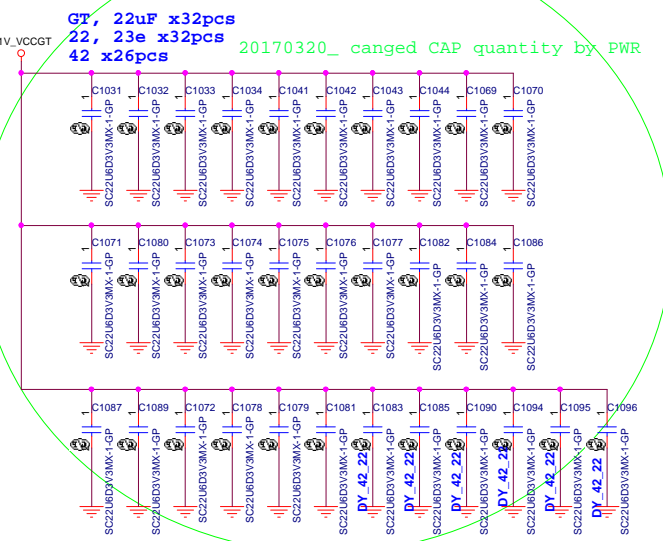
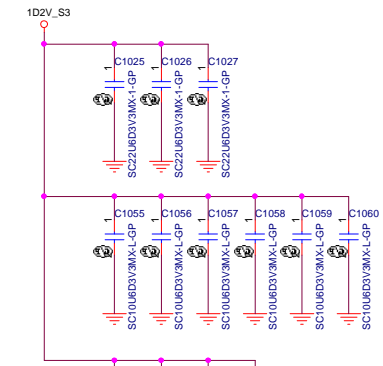
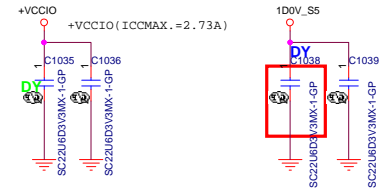
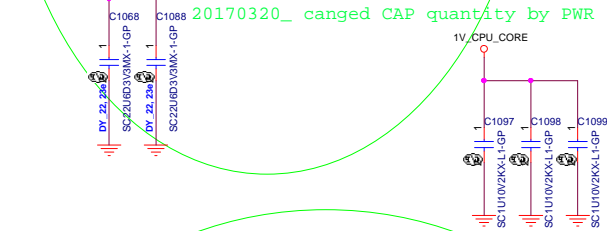
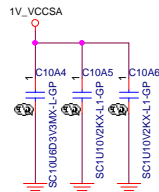
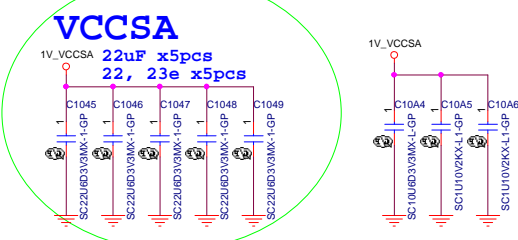
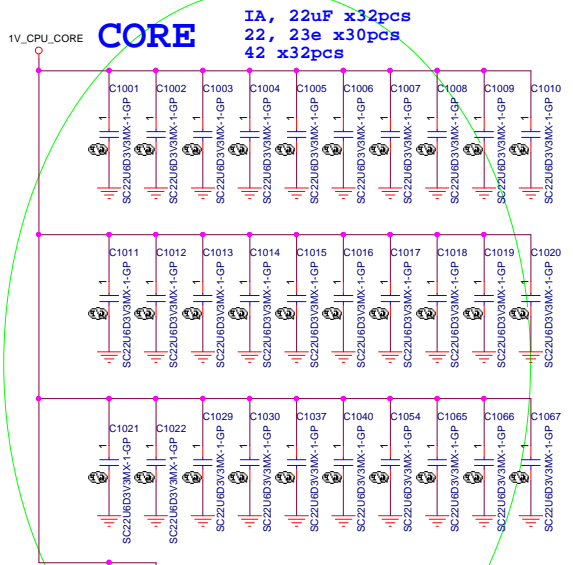
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Title
CPU (RESERVED)

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20170320 changed CAP quantity by PWR



GT:

U-Line_22/23e

U-line 22/23e 15W/28W
 IccMax current-10ms max[A] = 64 A

22uF	PCS	Cap
Suggestion	32	330uF*1 (U22)
Suggestion	32	330uF*2 (U23e)
OPP	26	330uF*1 (U22)

U-Line_42

U-line 22/42 15W/28W
 IccMax current-10ms max[A] = 32 A

22uF	PCS	Cap
Suggestion	26	330uF*1

IA:

U-Line_22/23e

U-line 22/23e 15W/28W
 IccMax current-10ms max = 32 A

22uF	PCS	Cap
Suggestion	30	330uF*1
OPP	22	330uF*1

U-Line_42

U-line 42
 IccMax current-10ms max = 64 A

22uF	PCS	Cap
Suggestion	32	330uF*2

VCCSA:

U-Line

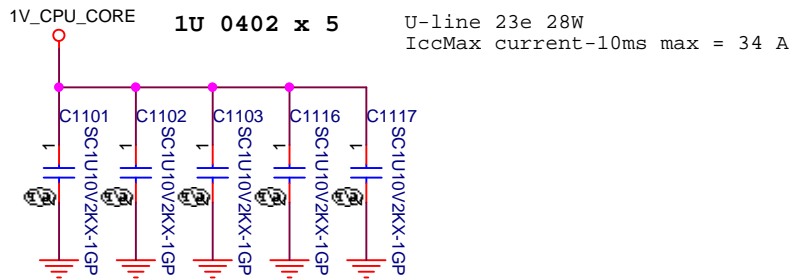
U-line 22/23e 15W/28W
 IccMax current-10ms max[A] = 5.1 A

22uF	PCS
Suggestion	5
OPP	5

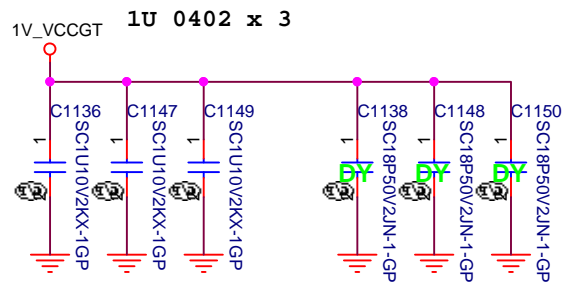
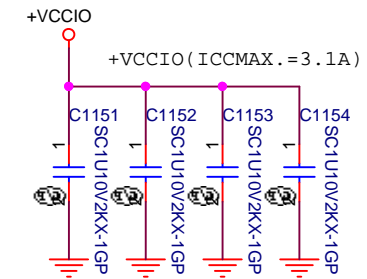
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緯創資通 Wistron Corporation	
<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
CPU (POWER CAP1)	
Size Custom	Document Number Unicorn_LV530_KBL_MB15A
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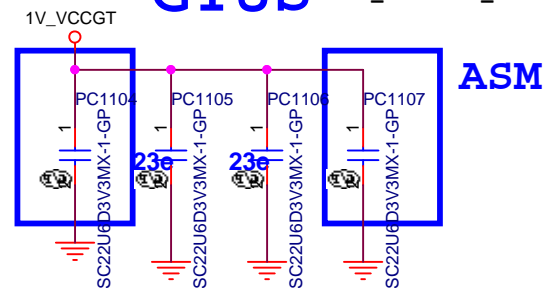
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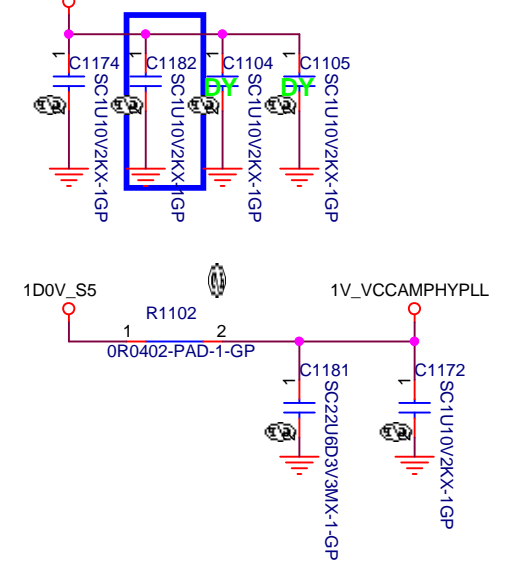
VCCIO



GTUS +V_VCCGTUS_VR can merge to +VCCGT

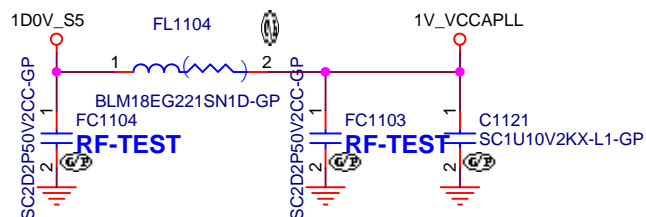
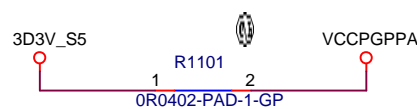
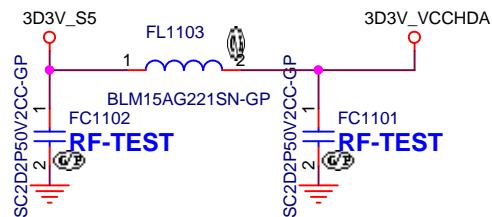


1D0V_S5 ASM 1UF



PCH DERIVED RAILS

VCCPGPPA(ICCMAX.=0.05A)



<Variant Name>

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Title			
CPU (POWER CAP2)			
Size A4	Document Number Unicorn_LV530_KBL_MB14		Rev SA
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<Variant Name>

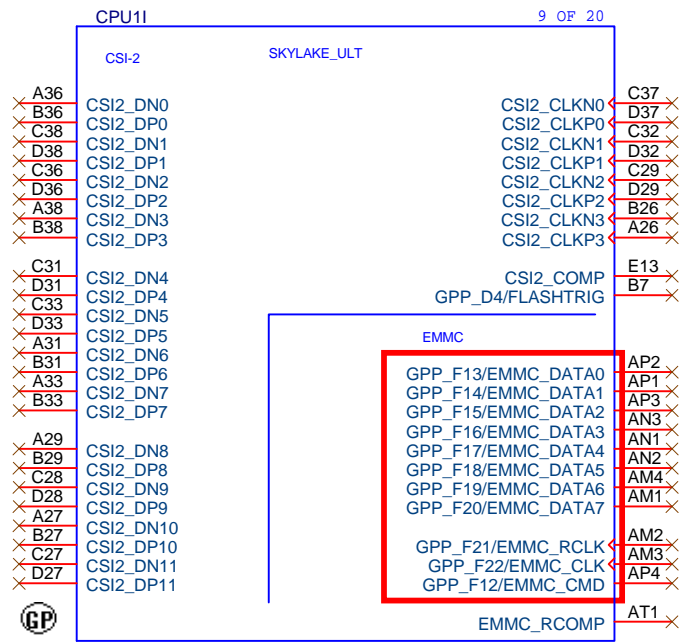
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Title **RESERVED**

Size A4	Document Number Unicorn LV530 KBL MB GA	Rev GA
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Main Func = PCH



GPP_F: VCCPGPPF = 1.8V Only

SKYLAKE-U-GP
071.SKYLA.000U BOM Change : KabyLake

<Variant Name>

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CPU (CSI2/EMMC)	
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[561280]
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.

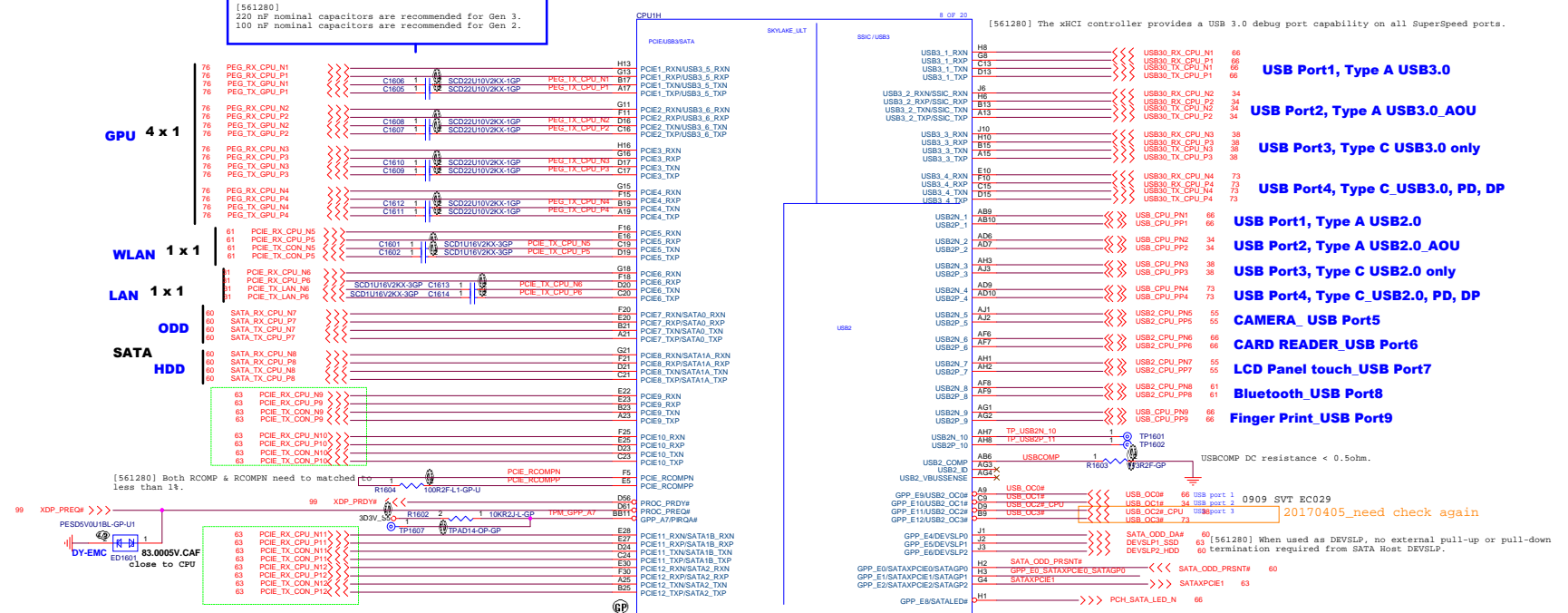
GPU 4 x 1
WLAN 1 x 1
LAN 1 x 1
SATA ODD
SATA HDD

M.2 SSD Optane
PCIe only

M.2 SSD Optane
PCIe/ SATA

4 x 1

Share SATA



PCIe Table

Port	PCIe Device	Share BUS
1	GPU L0	
2	GPU L1	
3	GPU L2	
4	GPU L3	
5	M.2 SSD	
6	M.2 SSD	
7	M.2 SSD	SATA0
8	M.2 SSD	SATA1A
9	LAN	
10	WLAN	
11	ODD	SATA1B
12	HDD	SATA2

SATA Table

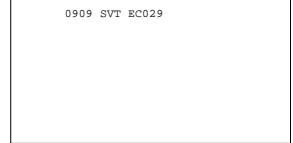
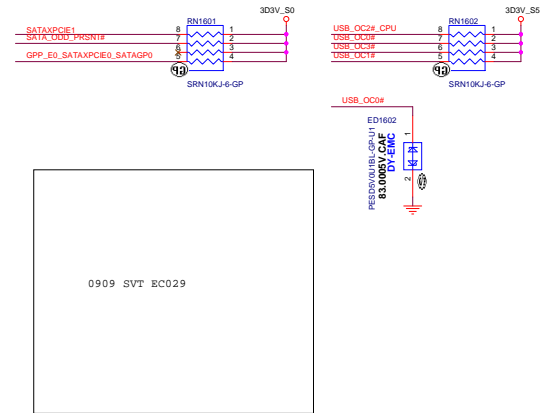
Pair	SATA Device	Share BUS
0	ODD	PCIe7
1A	HDD	PCIe8
1B	M.2 SSD	PCIe11
2	M.2 SSD	PCIe12

USB 3.0 Table

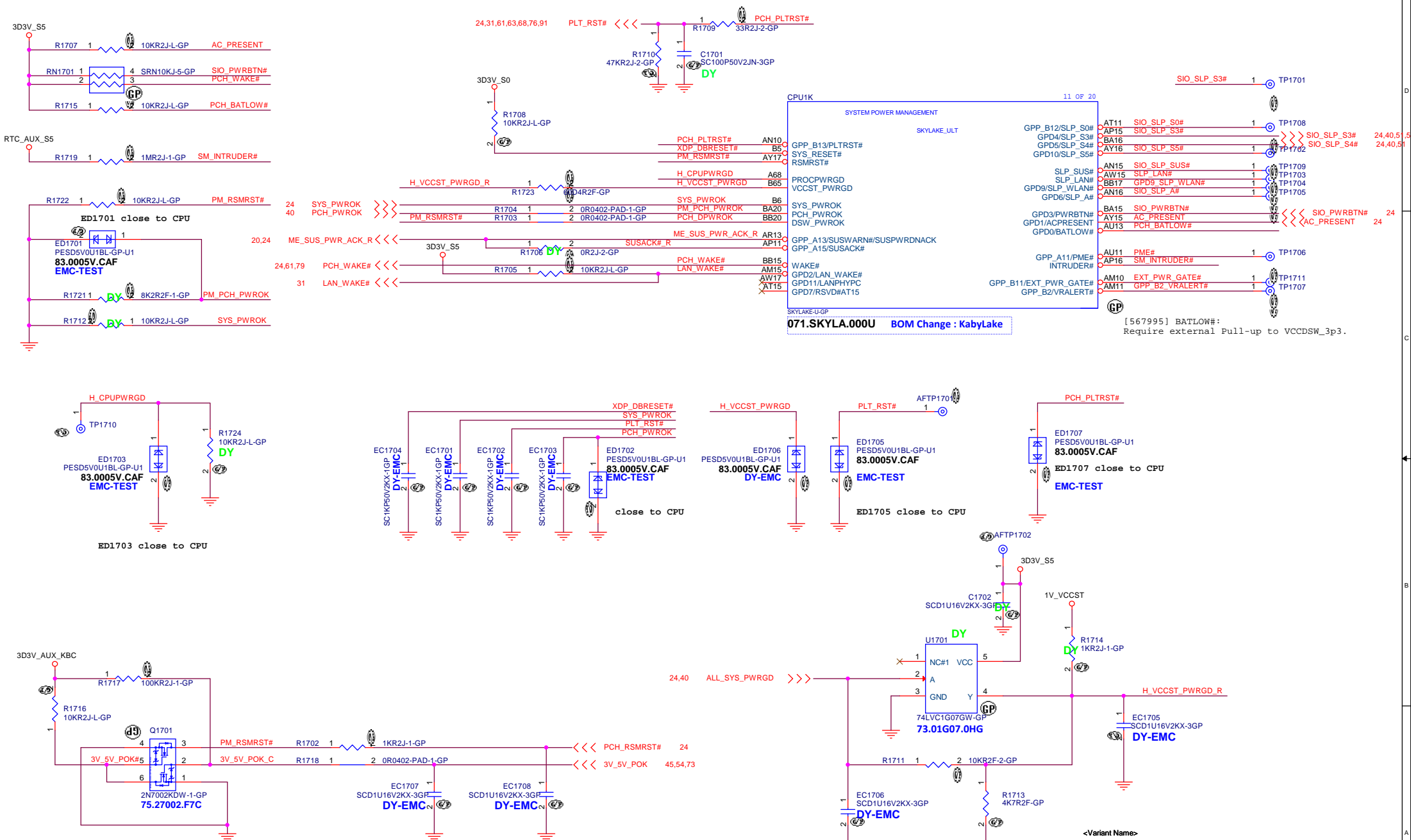
Pair	USB3.0 Device	Share BUS
1	USB3.0 port1 (Type A USB3.0)	
2	USB3.0 Port2 (Type A USB3.0_AOU)	
3	USB Port3, Type C USB3.0 only	
4	USB Port4, Type C, USB3.0, PD, DP	
5	N/A	PCIe1 (GPU)
6	N/A	PCIe2 (GPU)

USB 2.0 Table

Pair	USB2.0 Device
1	USB Port1, Type A USB2.0
2	USB Port2, Type A USB2.0_AOU
3	USB Port3, Type C USB2.0 only
4	USB Port4, Type C, USB2.0, PD, DP
5	CAMERA_USB Port5
6	CARD READER_USB Port6
7	LCD Panel touch_USB Port7
8	Bluetooth_USB Port8
9	Finger Print_USB Port9
10	Ultray bay_USB Port10



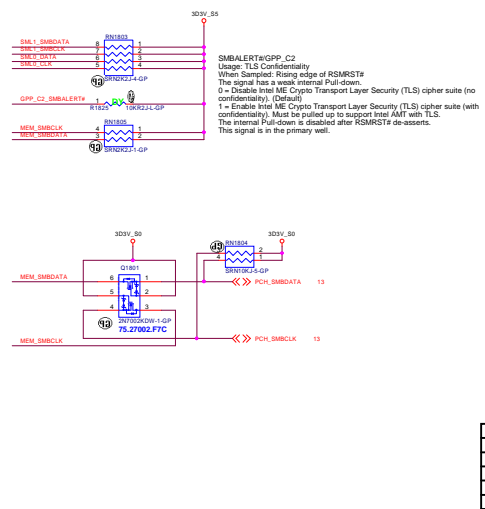
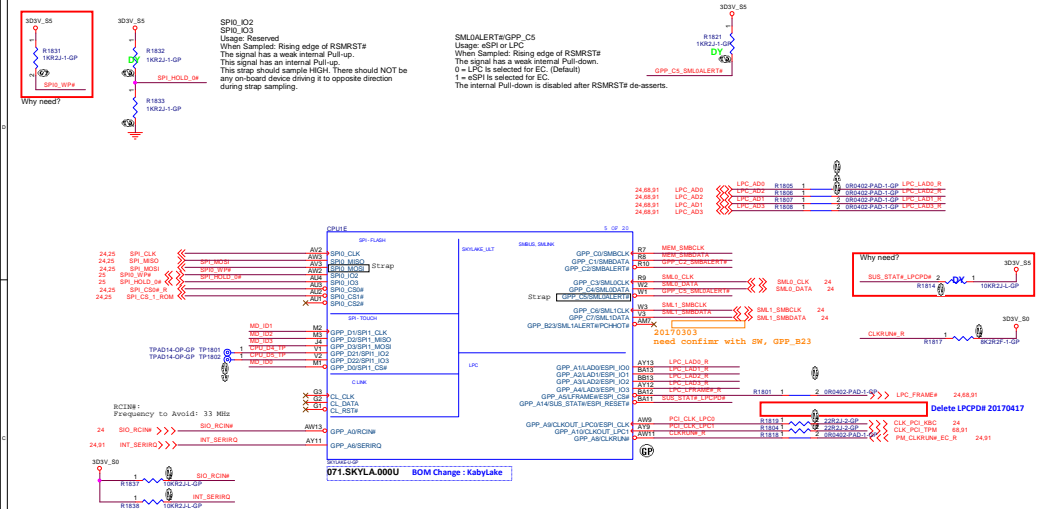
Main Func = PCH



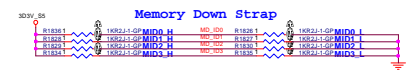
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Document Number		
UC1730		
Rev		
1.0		
Date		Sheet
Friday, December 15, 2017		17 of 105

Main PC = PCH

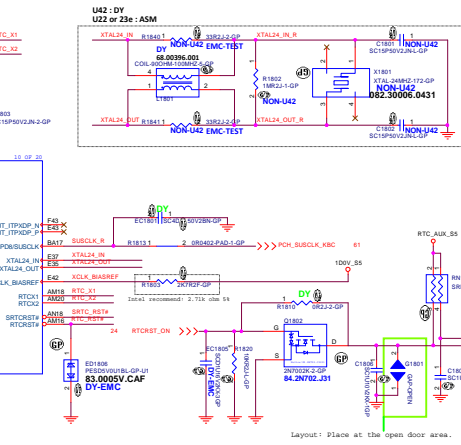
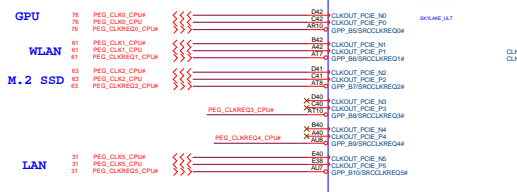


66A PIN	66B PIN	66C PIN	Location
SV20L77464	SV20L77465	SV20L77466	RAM1, RAM2, RAM3 RAM4
63 10534 L1L (1.0 MQ)	63 10234 L0L (1.0 KQ)	63 10534 L1L (1.0 MQ)	R1836
63 10234 L0L (1.0 KQ)	63 10534 L1L (1.0 MQ)	63 10234 L0L (1.0 KQ)	R1826
63 12534 1DL (1.2 MQ)	63 12534 1DL (1.2 MQ)	63 12234 1DL (1.2 KQ)	R1827
63 12234 1DL (1.2 KQ)	63 12234 1DL (1.2 KQ)	63 12234 1DL (1.2 KQ)	R1828
63 20534 1DL (2.0 MQ)	63 20534 1DL (2.0 MQ)	63 20534 1DL (2.0 MQ)	R1829
63 20234 1DL (2.0 KQ)	63 20234 1DL (2.0 KQ)	63 20234 1DL (2.0 KQ)	R1830
63 22534 1DL (2.2 MQ)	63 22534 1DL (2.2 MQ)	63 22534 1DL (2.2 MQ)	R1834
63 22234 L0L (2.2 KQ)	63 22234 L0L (2.2 KQ)	63 22234 L0L (2.2 KQ)	R1835
SAMSUNG 8GB	HYUNX 8GB	MICRON 8GB	
Memory ID : 0000	Memory ID : 0001	Memory ID : 0010	

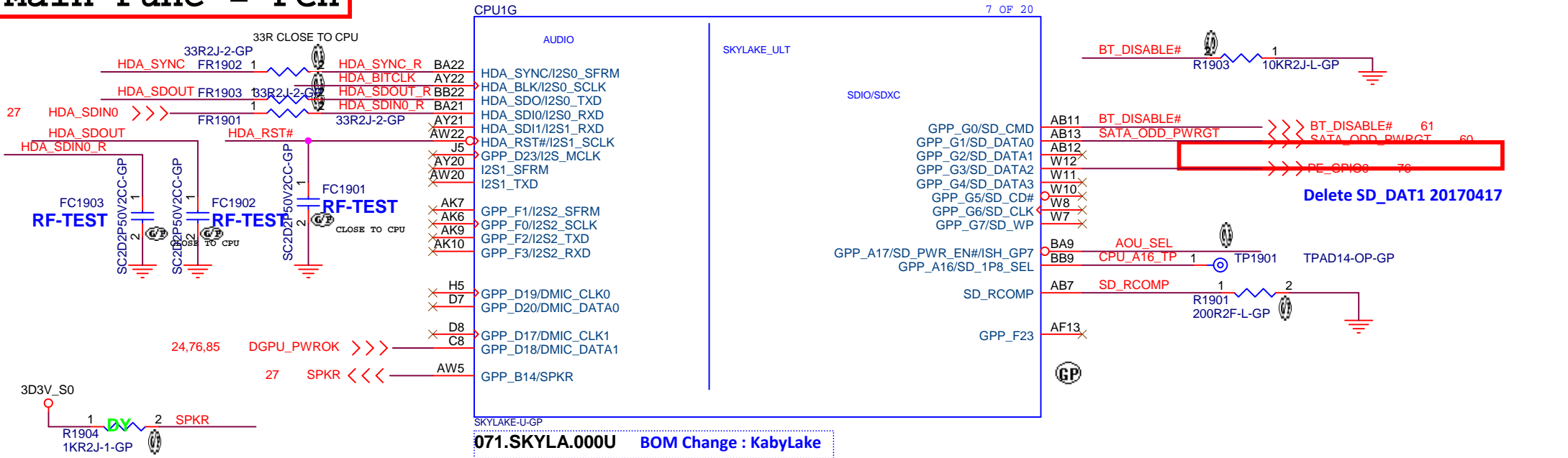


RAM ID	MD_ID0	MD_ID1	MD_ID2	MD_ID3	MD_ID4	MD_ID5	MD_ID6	MD_ID7	MD_ID8	MD_ID9	MD_ID10	MD_ID11	MD_ID12	MD_ID13	MD_ID14	MD_ID15
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1										
2	0	0	0	1	0											
3	0	0	0	1	1											
4	0	0	1	0	0											
5	0	1	0	0	1											
6	0	1	1	1	0											
7	0	1	1	1	1											
8	1	0	0	0	0											
9	1	0	0	0	1											
10	1	0	0	1	0											
11	1	0	1	1	1											
12	1	1	1	0	0											
13	1	1	1	0	1											
14	1	1	1	1	0											
15	1	1	1	1	1											

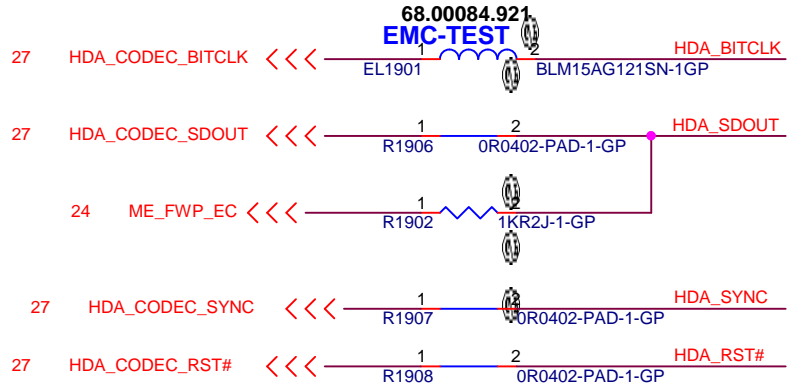
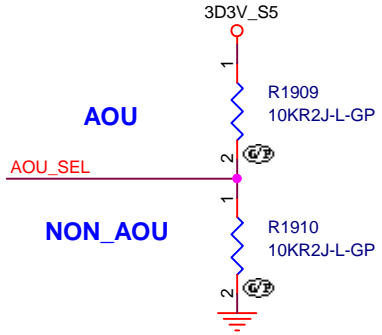
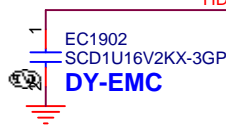
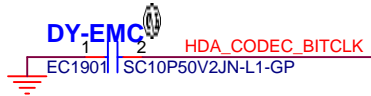
Check Clock Mapping



Main Func = PCH



SPKR/GPP_B14
 Usage: Top Swap Override
 When Sampled: Rising edge of PCH_PWROK
 The signal has a weak internal Pull-down.
 0 = Disable "Top Swap" mode. (Default)
 1 = Enable "Top Swap" mode.
 The internal Pull-down is disabled after PCH_PWROK de-asserts.
 This signal is in the primary well.

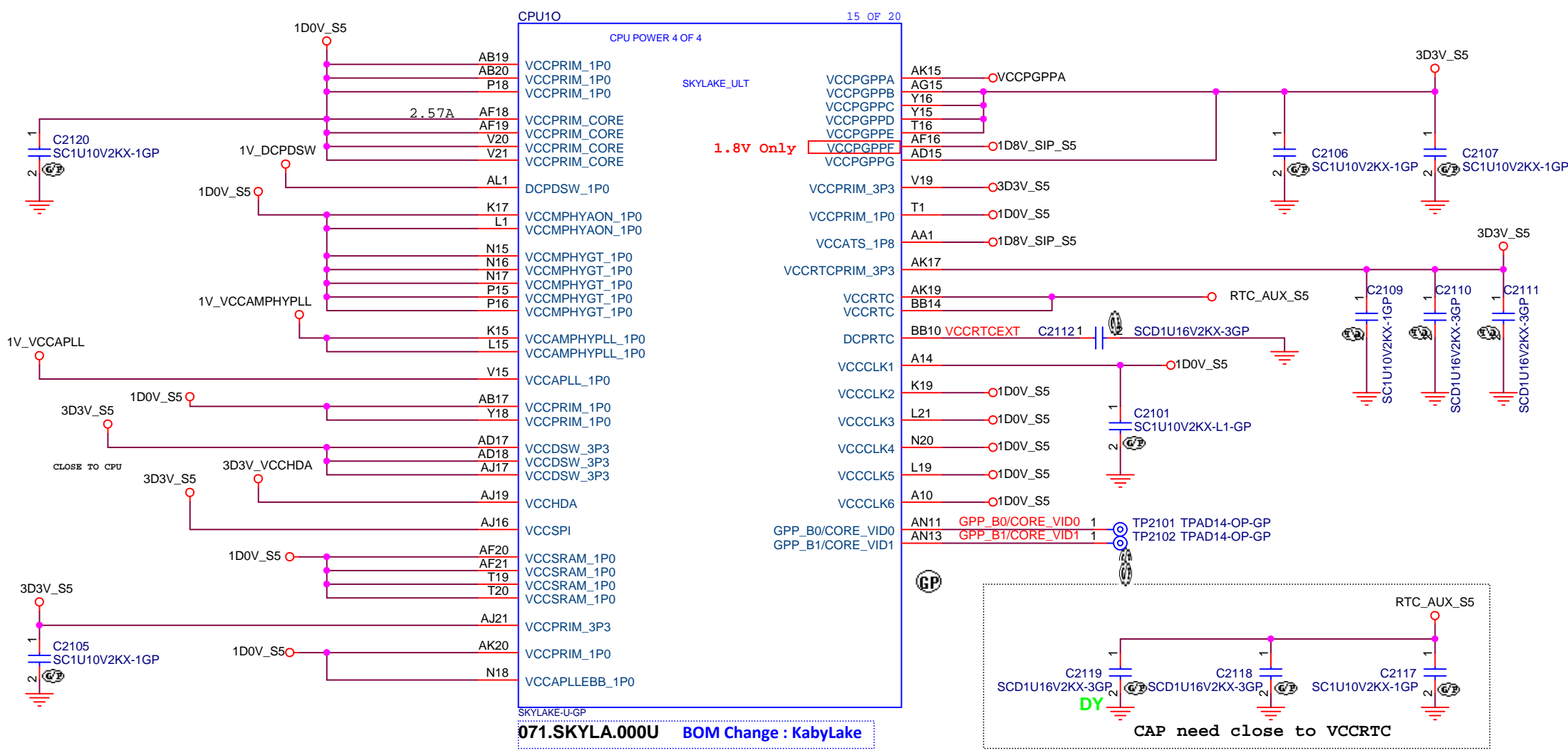


HDA_SDO /I2S_TXD0
 Usage: Flash Descriptor Security Override
 When Sampled: Rising edge of PCH_PWROK
 The signal has a weak internal Pull-down.
 0 = Enable security measures defined in the Flash Descriptor. (Default)
 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.
 The internal Pull-down is disabled after PCH_PWROK de-asserts.

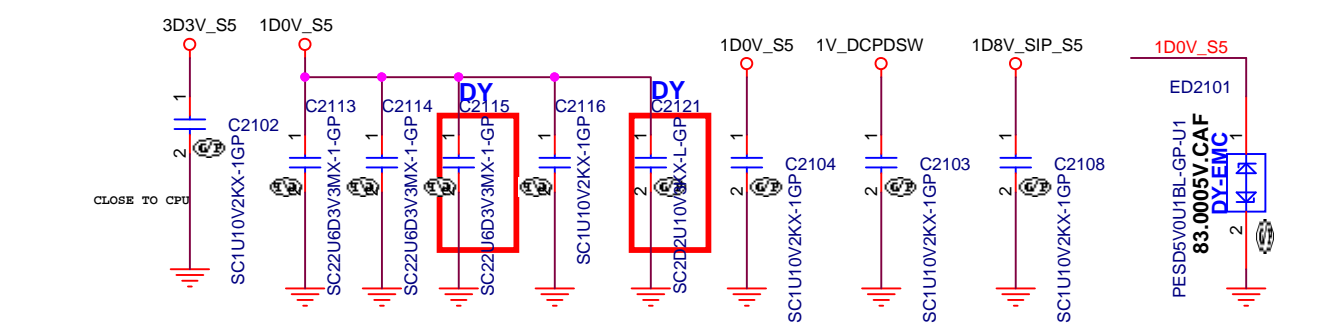
<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU (HDA/SDIO/SDXC)			
Size	Document Number		Rev
A4	Unicorn LV530_KBL_MB14		SA
Date:	Friday, December 15, 2017	Sheet	19 of 105

Main Func = PCH



SKYLAKE-U-GP
071.SKYLA.000U BOM Change : Kabylake



<Variant Name>

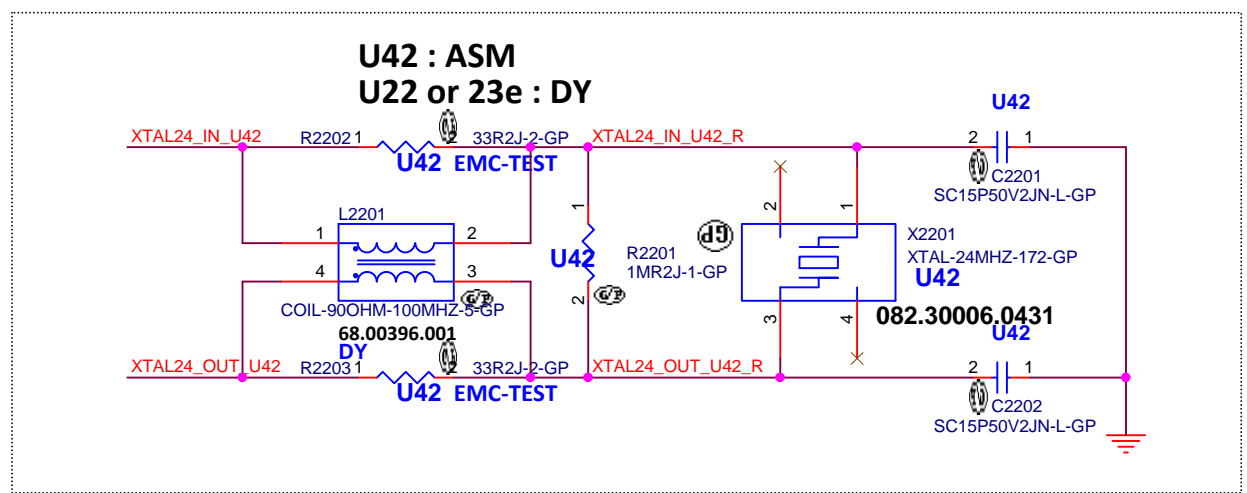
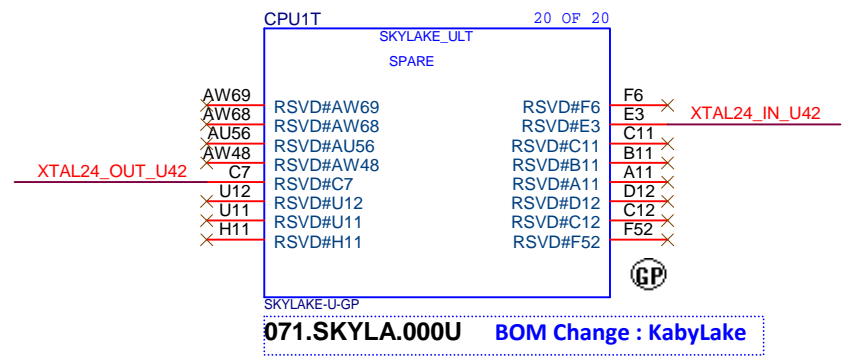
緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (POWER1)**

Size A4 Document Number Unicorn LV530 KBL MB 6A Rev

Date: Friday, December 15, 2017 Sheet 21 of 105

Main Func = PCH



<Variant Name>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **CPU (RSVD)**

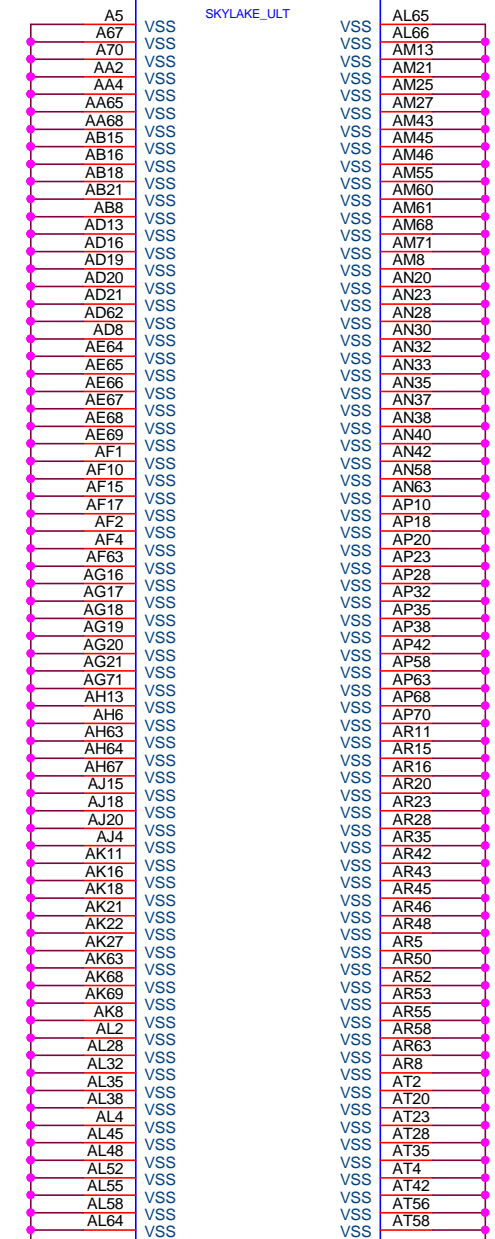
Size A4 Document Number **Unicorn LV530 KBL MB GA** Rev

Date: Friday, December 15, 2017 Sheet 22 of 105

Main Func = PCH

CPU1P 16 OF 20

GND 1 OF 3

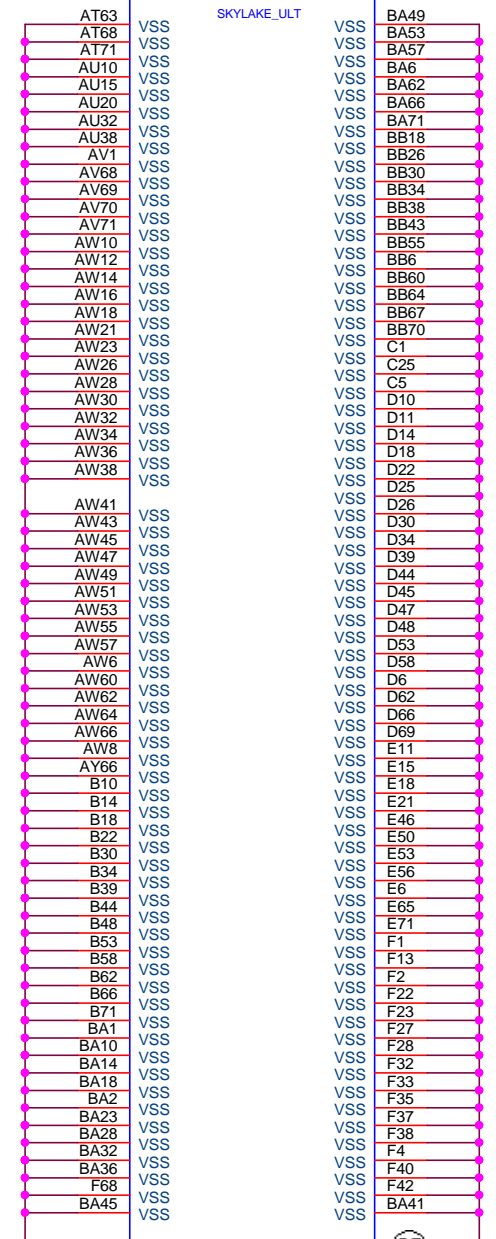


SKYLAKE-U-GP

071.SKYLA.000U BOM Change : KabyLake

CPU1Q 17 OF 20

GND 2 OF 3

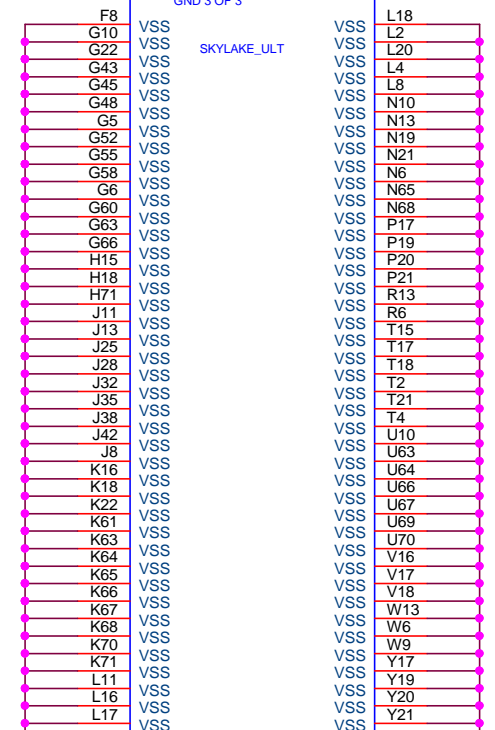


SKYLAKE-U-GP

071.SKYLA.000U BOM Change : KabyLake

CPU1R 18 OF 20

GND 3 OF 3



SKYLAKE-U-GP

071.SKYLA.000U BOM Change : KabyLake

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (VSS)

Size Custom

Document Number

Rev

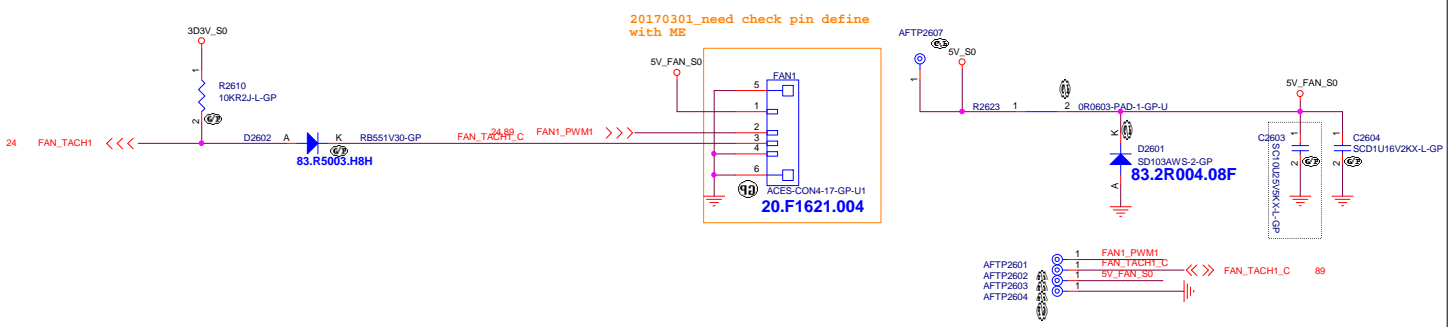
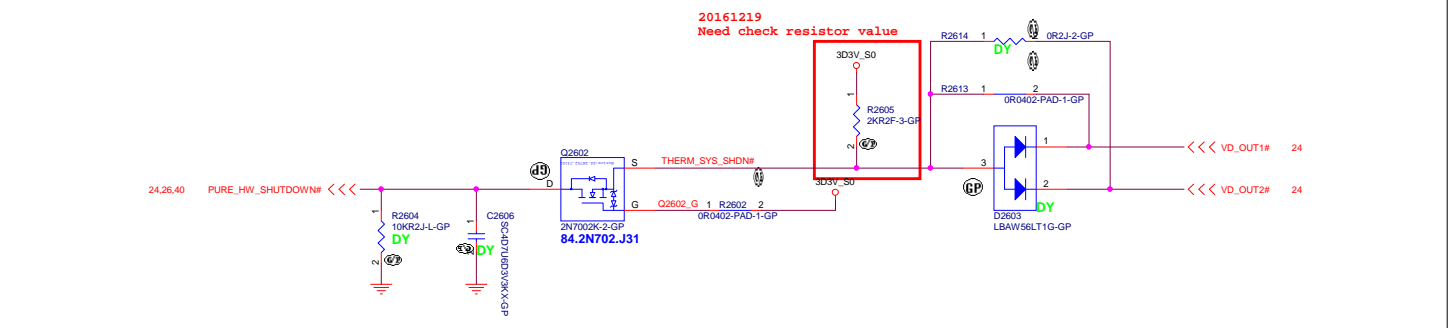
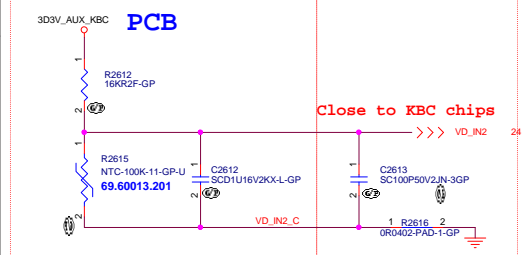
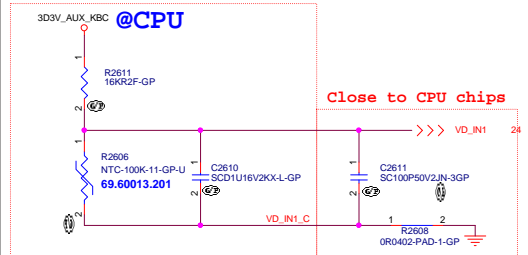
Unicorn LV530 KBL MB 6A

Date: Friday, December 15, 2017

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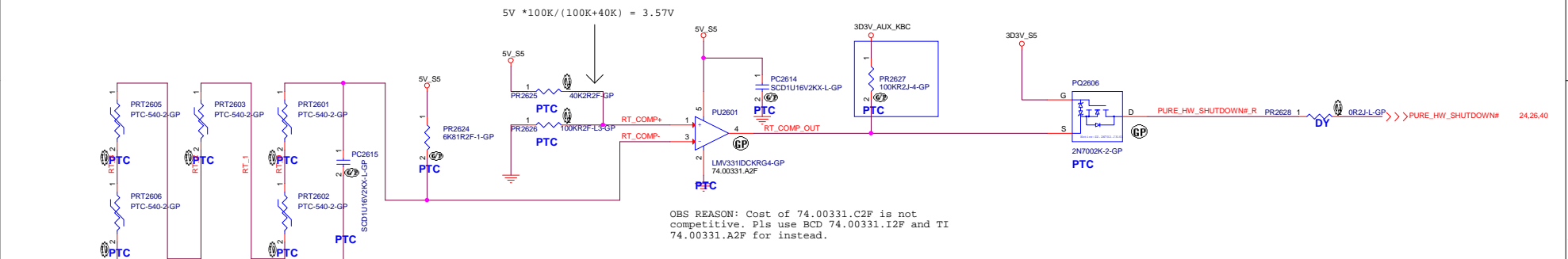
Main Func = Thermal Sensor

Close to Thermal sensor



PURE_HW_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low



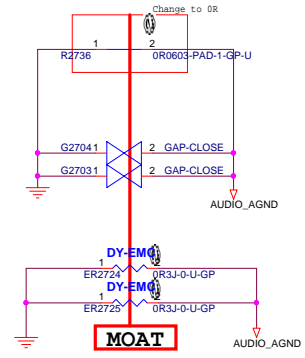
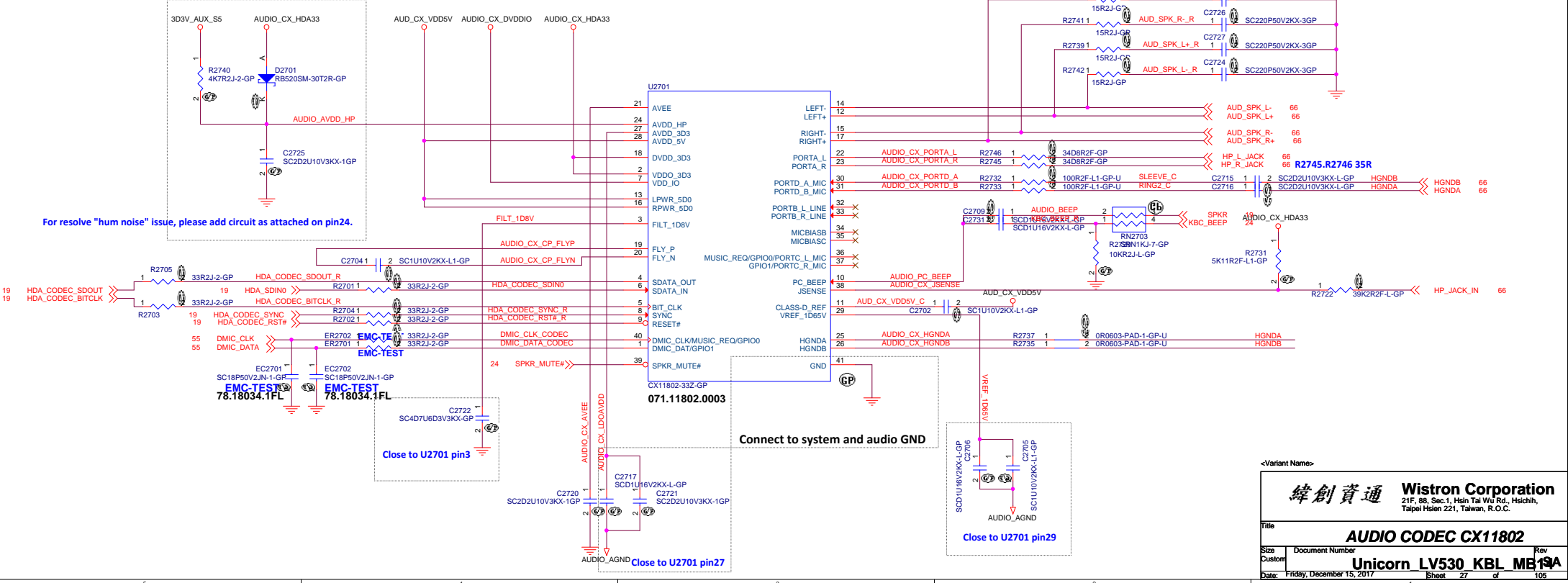
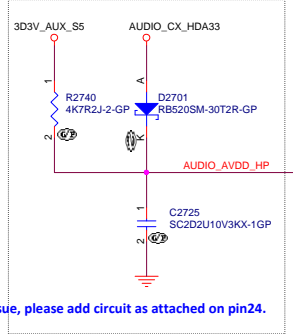
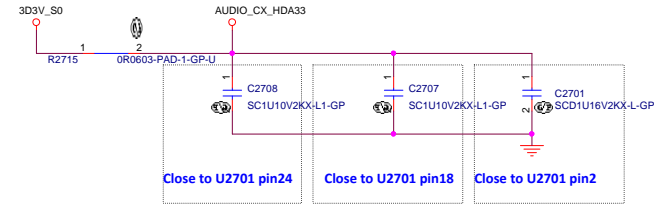
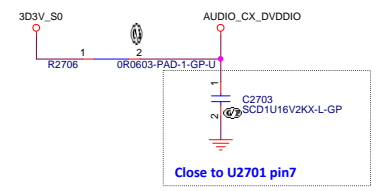
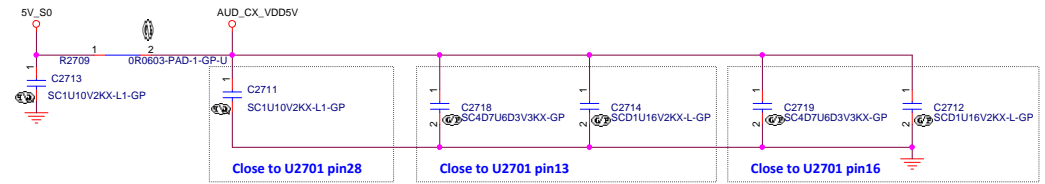
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hei Tai Wu Rd., Hsichih, Taipei Heien 221, Taiwan, R.O.C.

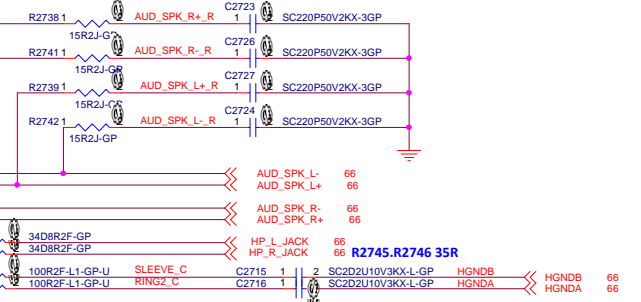
Title: **THERMAL/FAN**

Size: Custom Document Number: **Unicorn LV530 KBL ME19A** Rev: **105**

Date: Friday, December 15, 2017 Sheet 26 of 105



Install snubber networks on each net of SPKs helps control the overshoot/undershoot at the class-D outputs.



<p>緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>AUDIO CODEC CX11802</p>	
<p>Spec Custom</p>	<p>Document Number</p>
<p>Unicorn LV530 KBL MB19A</p>	
<p>Date: Friday, December 15, 2017</p>	<p>Sheet 27 of 105</p>

INTERNAL STEREO SPEAKERS
MOVE TO SMALL BOARD

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

AUDIO SPEAKER

Size

A3

Document Number

Unicorn LV530 KBL MB13A

Rev

Date: Friday, December 15, 2017

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5

4

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D

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B

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A

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(RESERVED)

Size
A4

Document Number

Unicorn_LV530_KBL_MB14BOHOL

Rev
SA

Date: Friday, December 15, 2017

Sheet 30 of 105

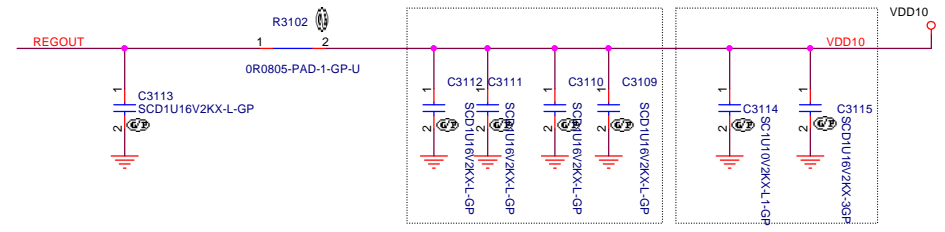
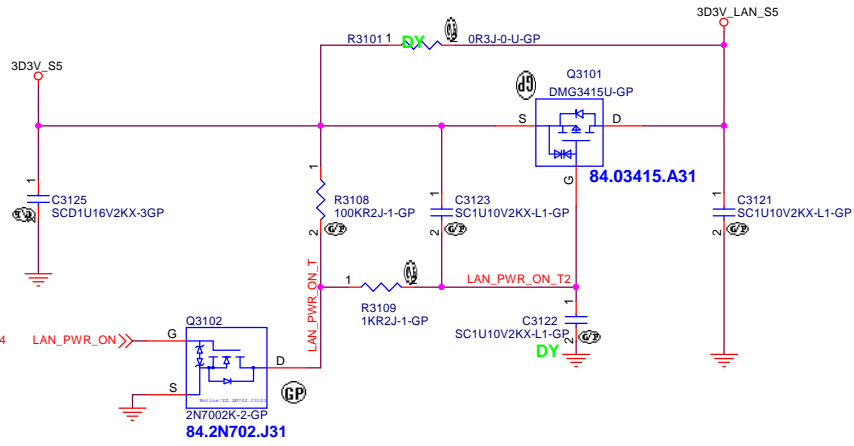
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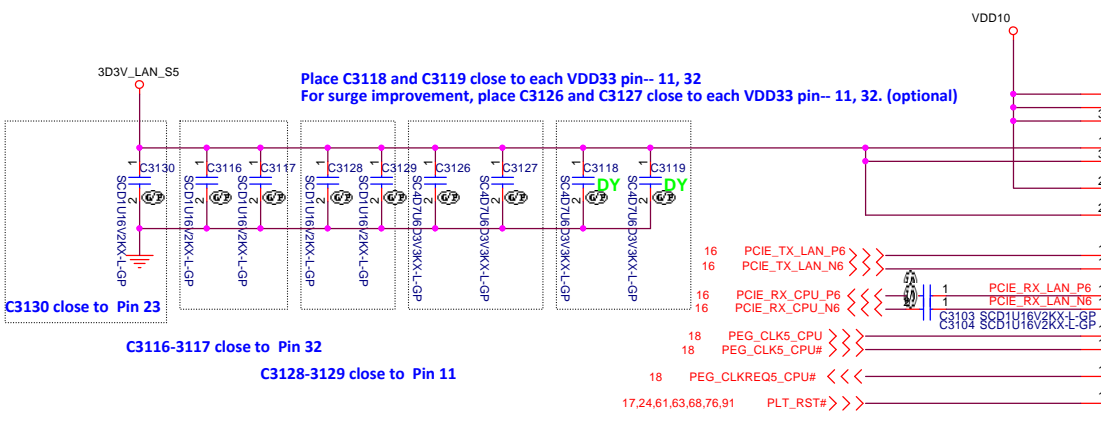
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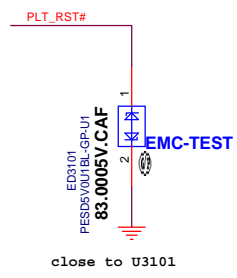
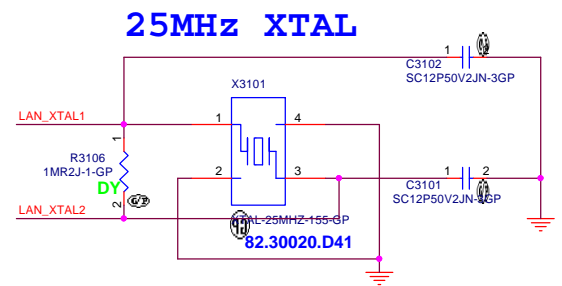
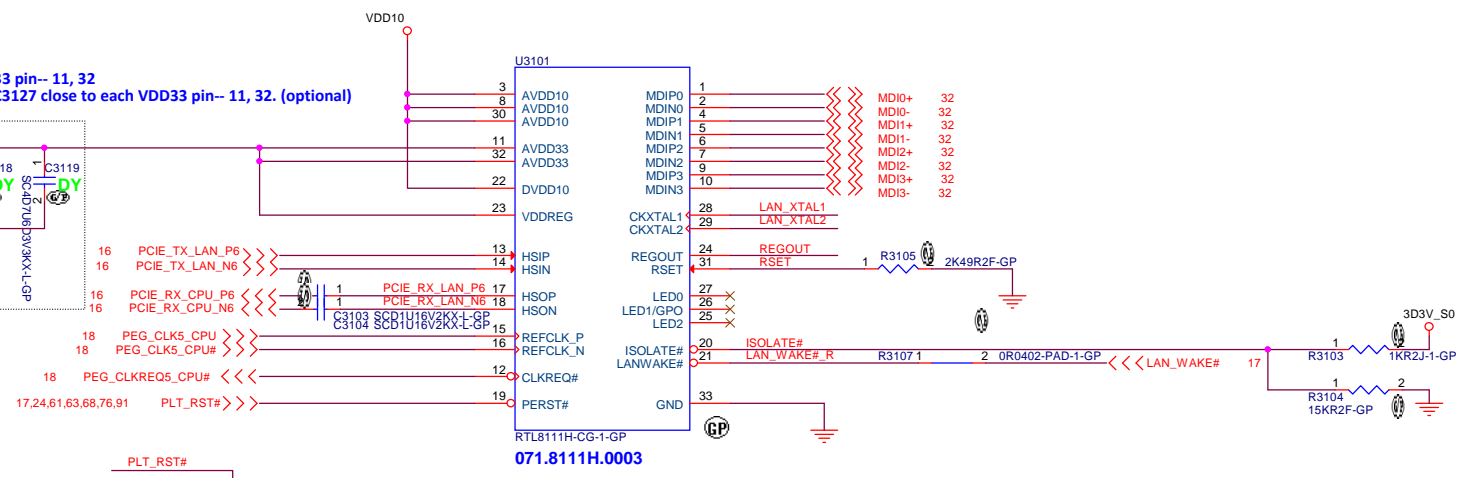
1



For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
 *Place C3109 to C3112 close to each VDD10 pin-- 3, 8, 22, 30
 For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
 *Place C3114 and C3115 close to each VDD10 pin-- 22 (Reserved)

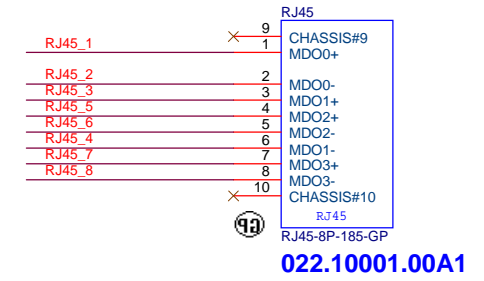
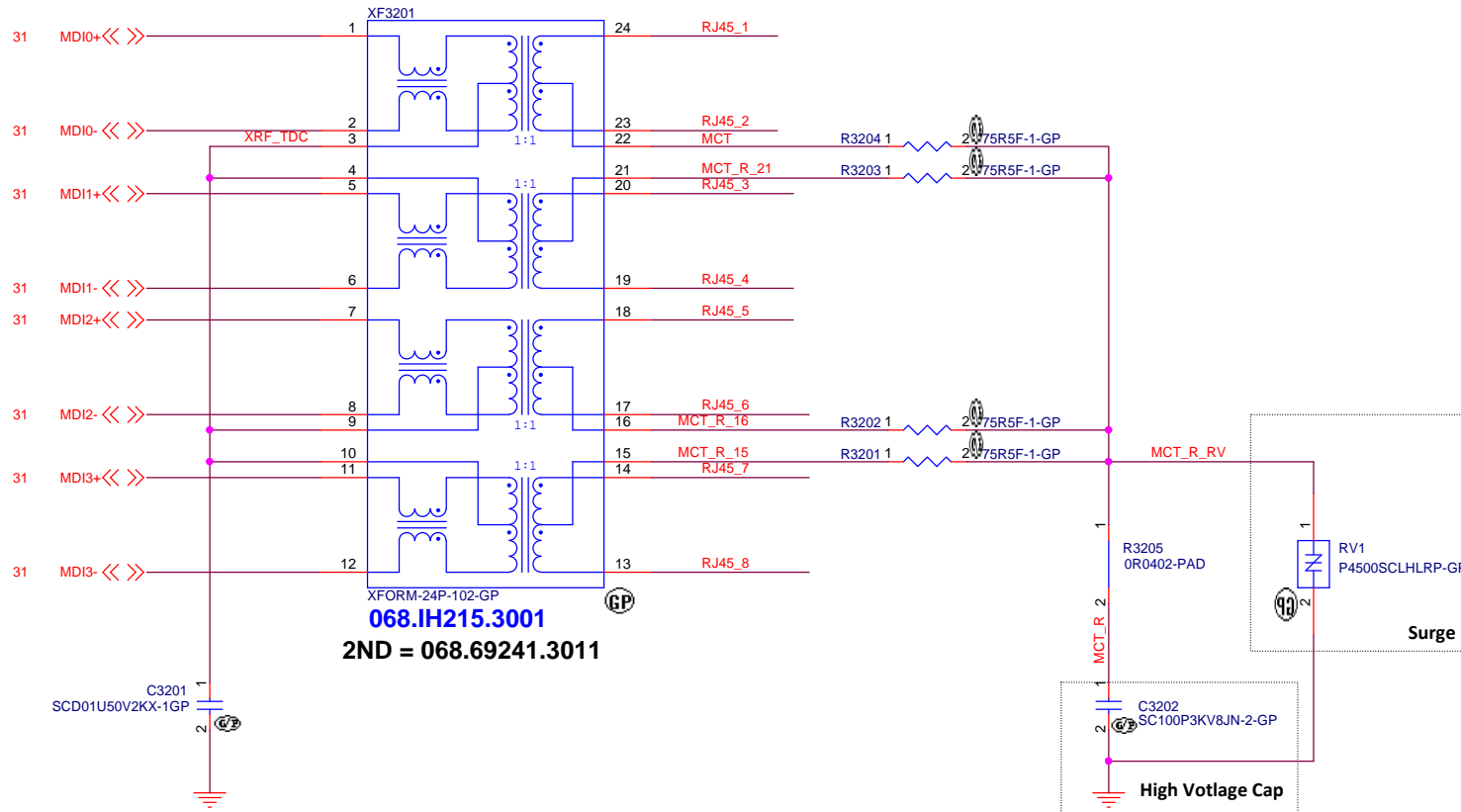


C3130 close to Pin 23
 C3116-3117 close to Pin 32
 C3128-3129 close to Pin 11

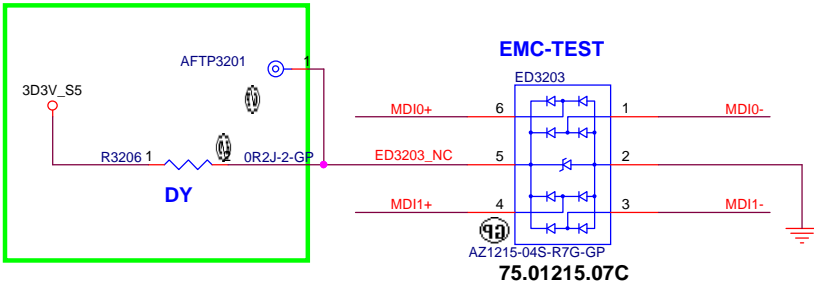


10/100M/1000M Lan Transformer

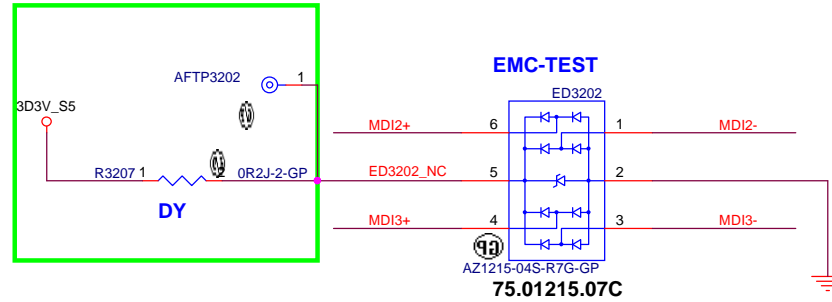
LAN Connector



20170606
EMC Tim Lee requirement

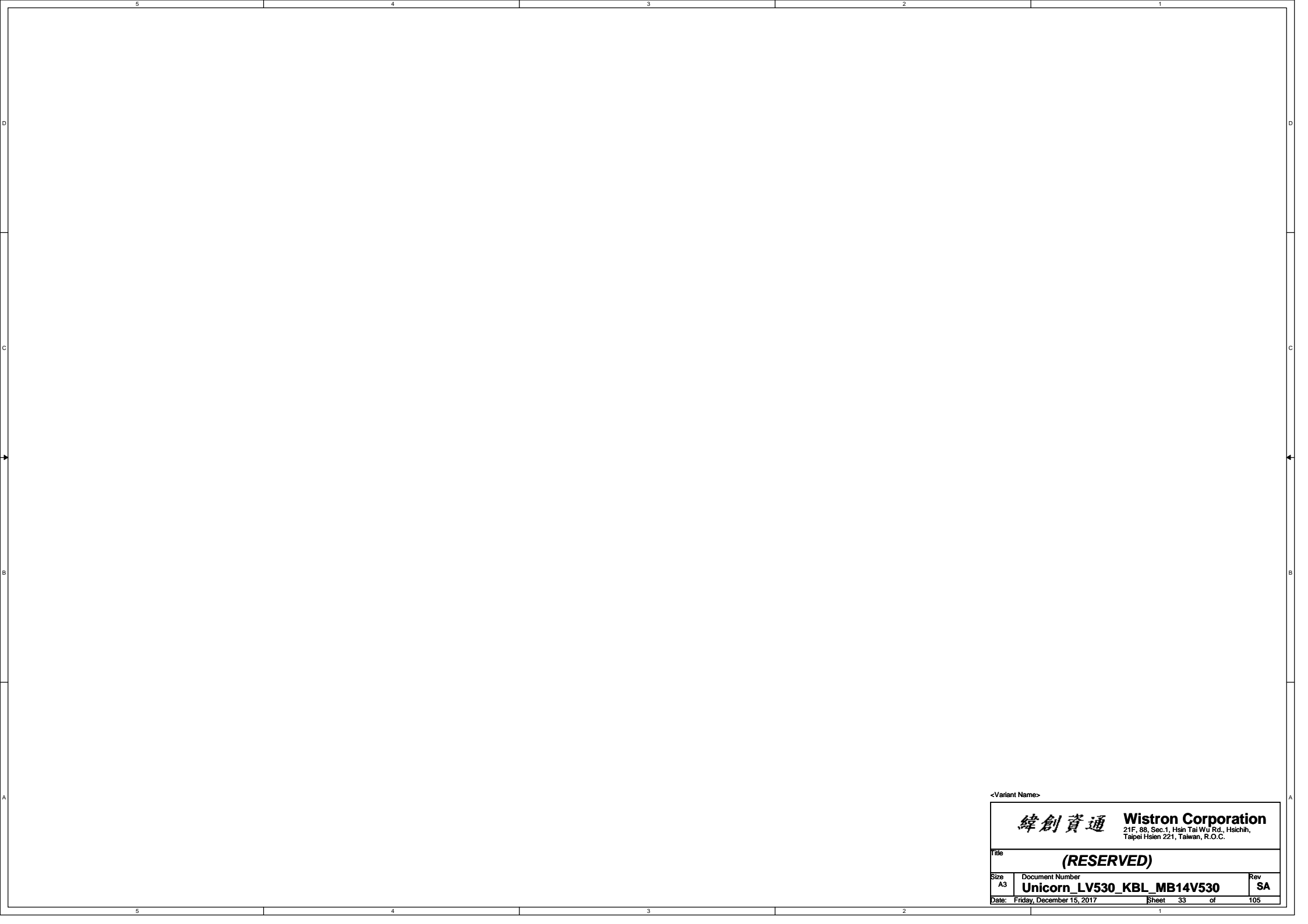


20170606
EMC Tim Lee requirement



<Variant Name>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
RJ45			
Size	Document Number	Rev	
Custom	Unicorn LV530 KBL MB13A		
Date:	Friday, December 15, 2017	Sheet	32 of 105



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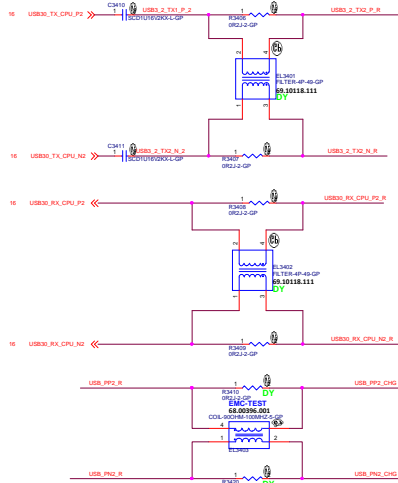
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **(RESERVED)**

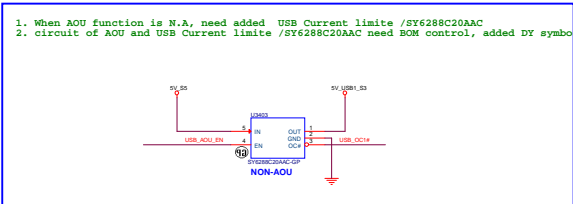
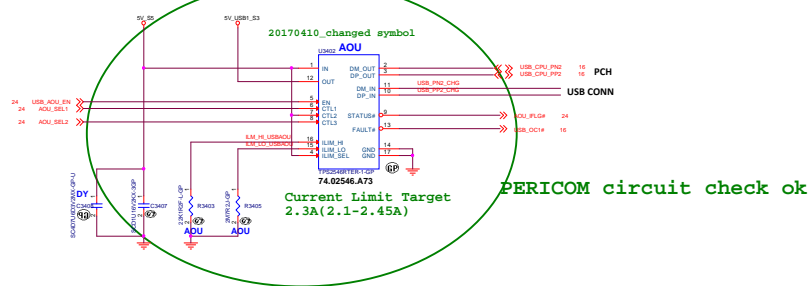
Size A3	Document Number Unicorn_LV530_KBL_MB14V530	Rev SA
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Date: Friday, December 15, 2017 Sheet 33 of 105

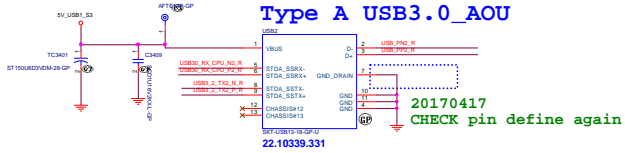
needReserve USB2.0 by pas AOU



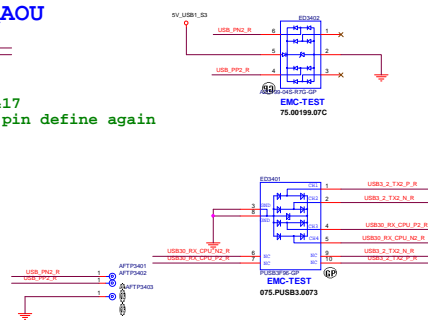
AOU
 1ST,
 TI, 74.02546.A73
 IC PWR SW TPS2546RTER QFN 16P(REV 1.1)
 2ND
 PERICOM, 074.52546.0A73
 IC PWR SW PI5USB2546ZHEX TQFN 16P REV.X



USB Port2
 Type A USB3.0_AOU



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	St-dA_SSRX-	SuperSpeed RX
6	St-dA_SSRX+	
7	GND	
8	St-dA_SSTX-	SuperSpeed TX
9	St-dA_SSTX+	



RESERVED

<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB30 RE-DRIVER			
Size	Document Number	Rev	
A3	Unicorn_LV530_KBL_MB13A	1.0	
Date: Friday, December 15, 2017		Sheet	35 of 105

5

4

3

2

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D

D

C

C

B

B

A

A

<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
TYPEC USB3.1-1			
Size	Document Number		Rev
A4	Unicorn LV530 KBL MB SA		1A
Date: Friday, December 15, 2017		Sheet 37	of 105

5

4

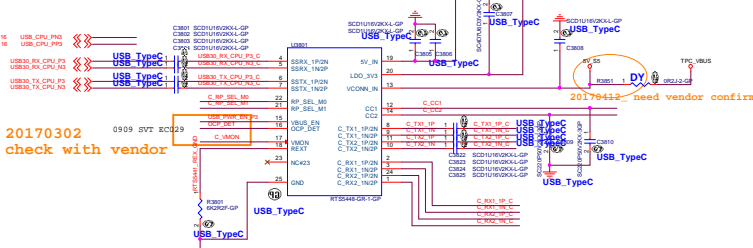
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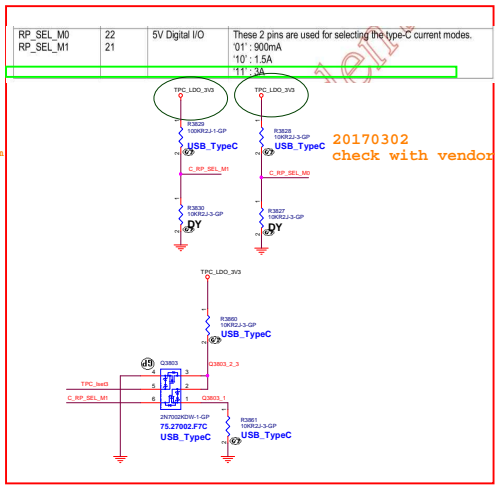
USB Port3, Type C USB3.0 only

Type C controller_MUX

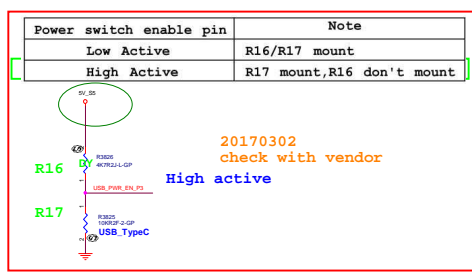


20170302 check with vendor

20170412 need vendor confirm



20170302 check with vendor

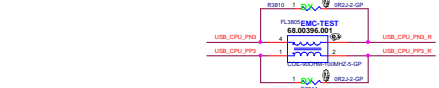
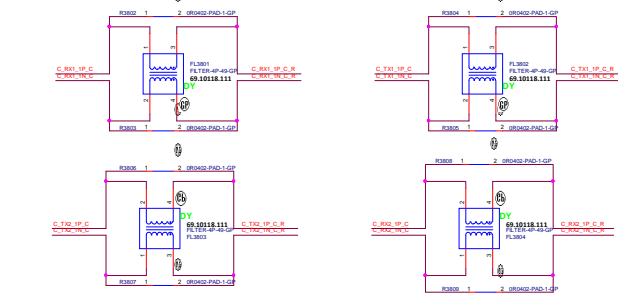


Power switch enable pin	Note
Low Active	R16/R17 mount
High Active	R17 mount, R16 don't mount

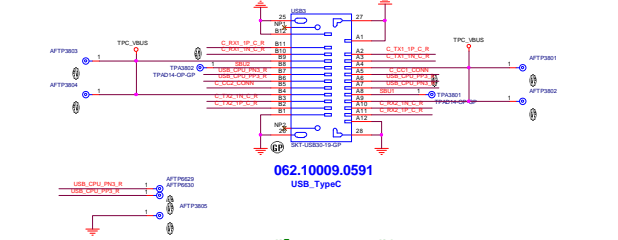
20170302 check with vendor

High active

Power switch enable pin	Note
Low Active	R3826/R3825 mount
High Active	R3825 mount, R3826 don't mount

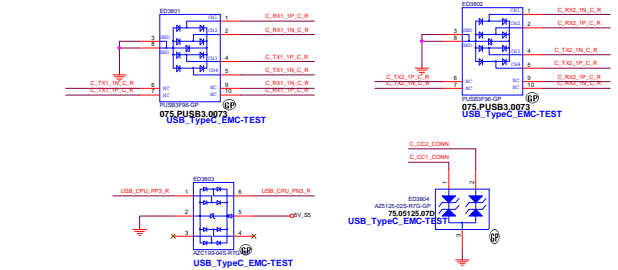


USB Port3, Type C USB3.0 only



062.10009.0591 USB_TypeC

Close to CONN

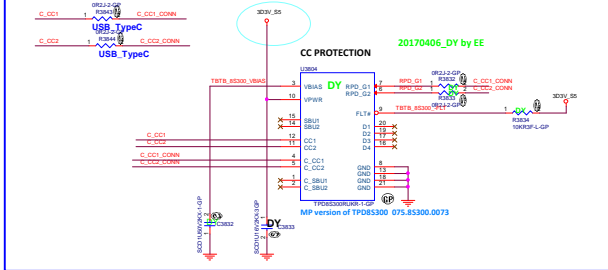


075.PUBS3.0073 USB_TypeC_EMC-TEST

075.0054.007D USB_TypeC

75.0019.07C USB_TypeC_EMC-TEST

CC Protect Function

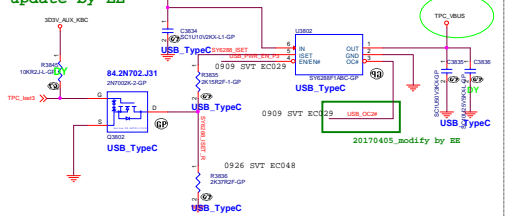


CC PROTECTION

300V.55

20170406_DY by EE

CC Limit_3A



20170322 update by EE

- 1. AC: 15W / 3A, 系統功耗不足降至4.5W / 0.9A
- 2. DC: 4.5W / 0.9A

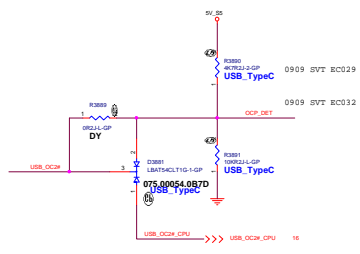
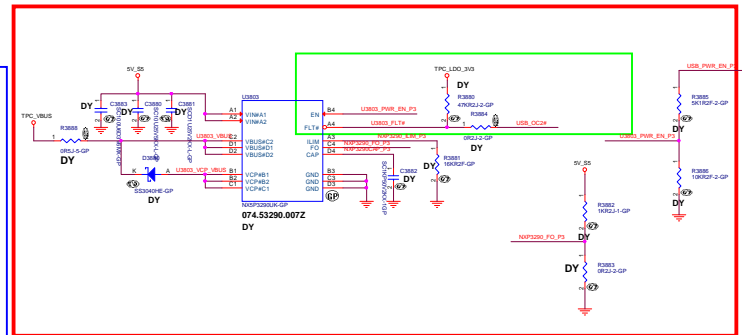
Over-current protection

The SY6288F1/F2 supports Current limit programming. Connect a resistor R_{SET} from ISET pin to ground to program the current limit:

$$I_{LIM} (A) = 6800 / R_{SET} (\Omega)$$

The minimum current limit is 0.4A. Current limit beyond 4A is not recommended.

- R3835 / 2.15K >> 3.16A
- R3835 / 2.15K + R3836 / 5.1K >> 0.94A



5

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D

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C

B

B

A

A

<Variant Name>

<Title>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

A

Document Number

Unicorn_LV530_KBL_MB14BOH01SA

Rev

Date: Friday, December 15, 2017

Sheet 39 of 105

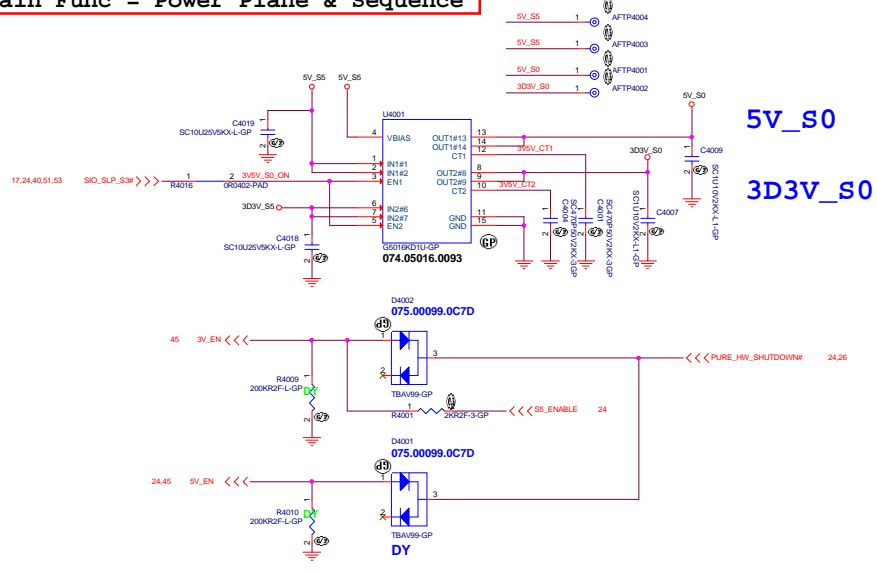
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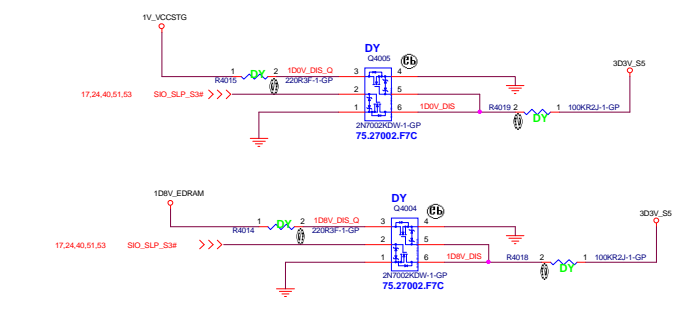
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2

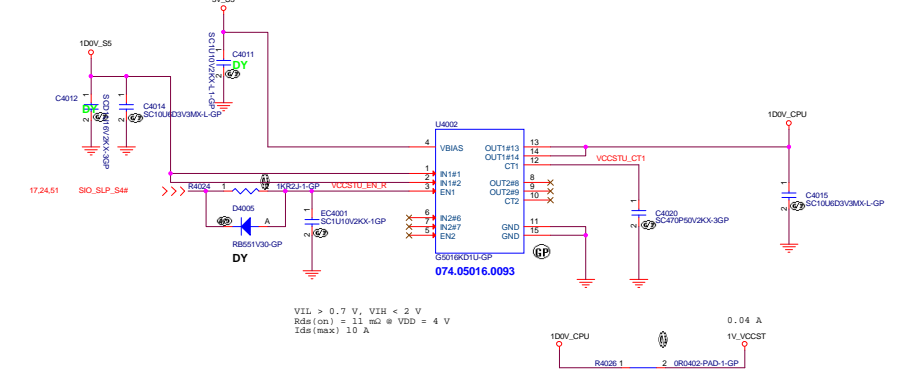
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Discharge circuit

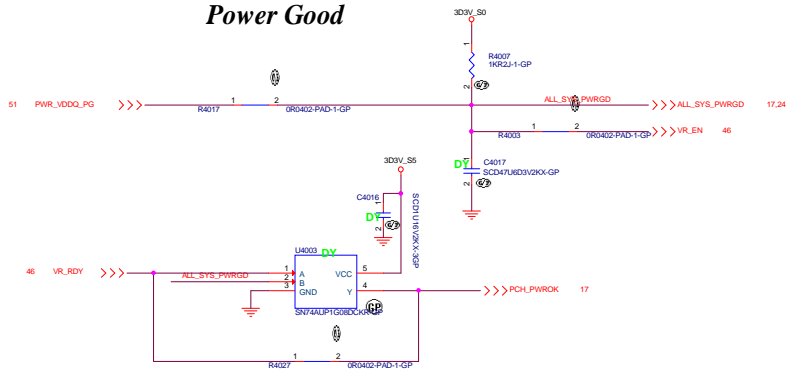


VCCSTU

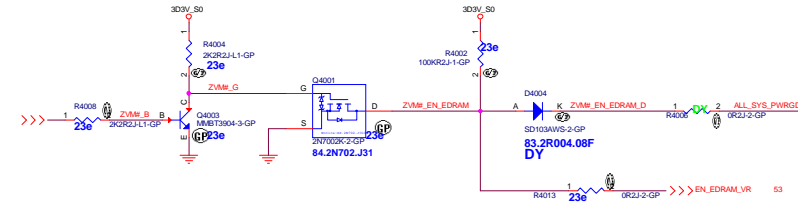


VIL > 0.7 V, VIH < 2 V
 Rds(en) = 11 mΩ @ VDD = 4 V
 Ids(max) 10 A

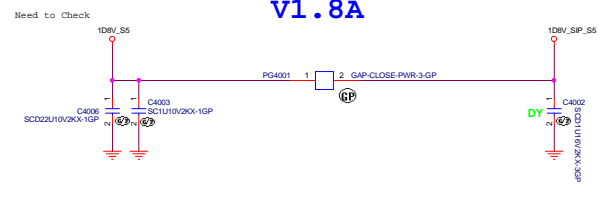
Power Good



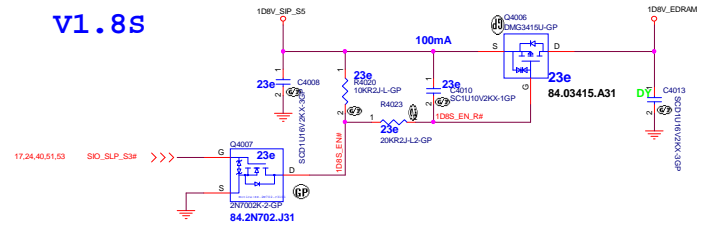
GT3 Low Power Circuit (ZVM)



V1.8A



V1.8S



561280 KBL DY PDG Rev2.0 Notes:
 On power up sequence, VCC0PC_lpb8 must never ramp up after VCC0PC/VCC0PIO under any circumstance.
 There are no ramp down requirements between VCC0PC_lpb8 and VCC0PC/VCC0PIO.
 Platform must guarantee VCC0PC/VCC0PIO falls do not start ramping back up for any reason while VCC0PC_lpb8 is ramping down or OFF.

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D

D

C

C

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B

A

A



<Variant Name>

Title
<Title>

Size A	Document Number <Doc>	Rev <RevCode>
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Date: Friday, December 15, 2017 Sheet 41 of 105

5

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1

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<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size
A4

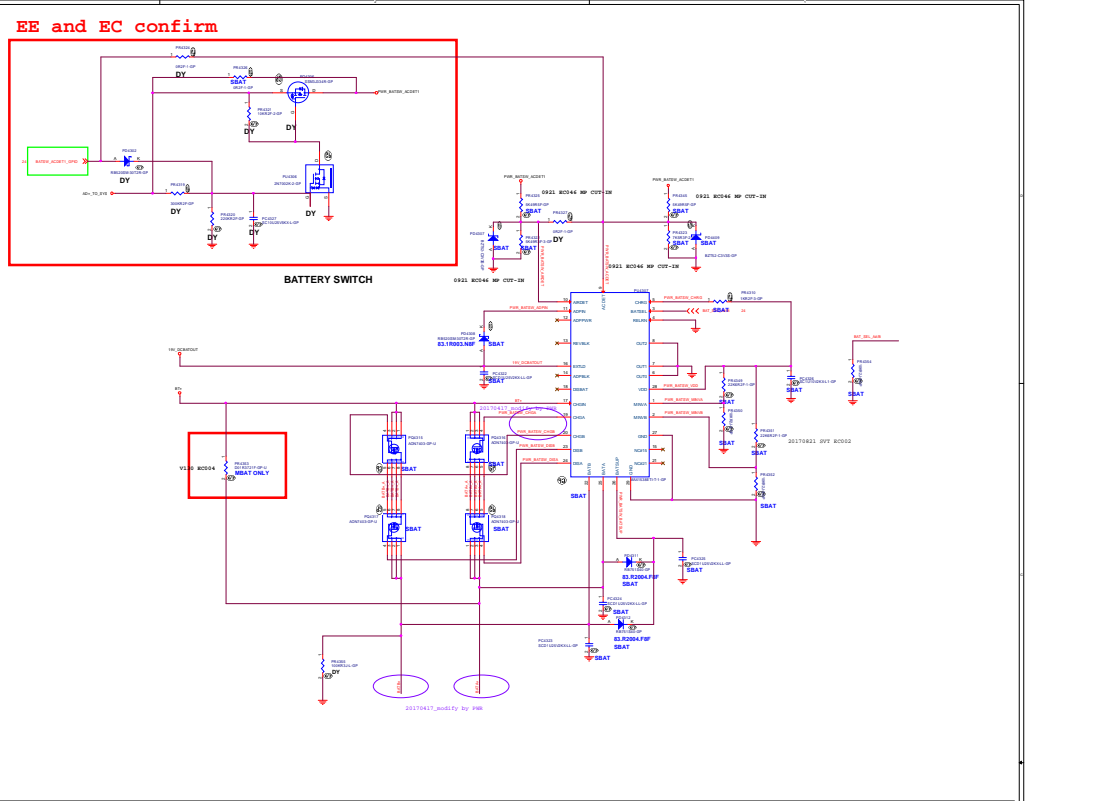
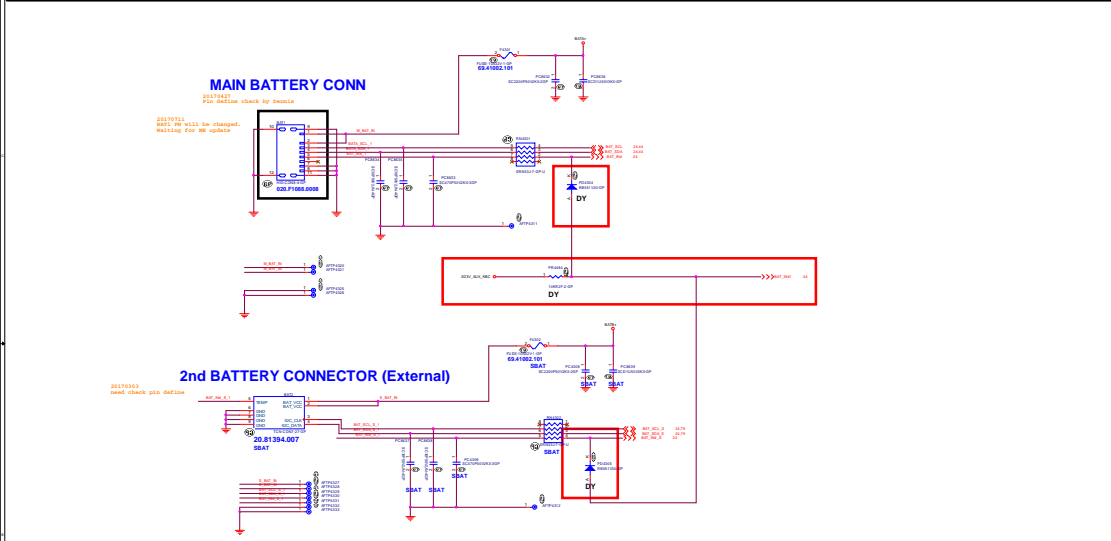
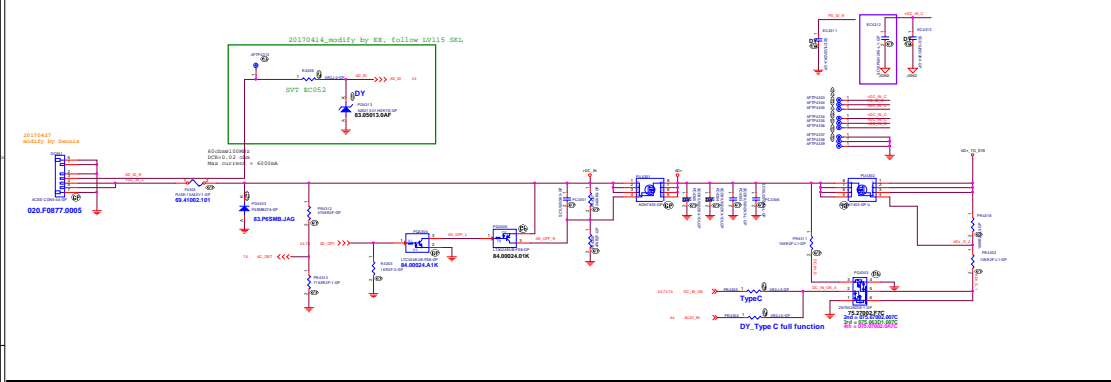
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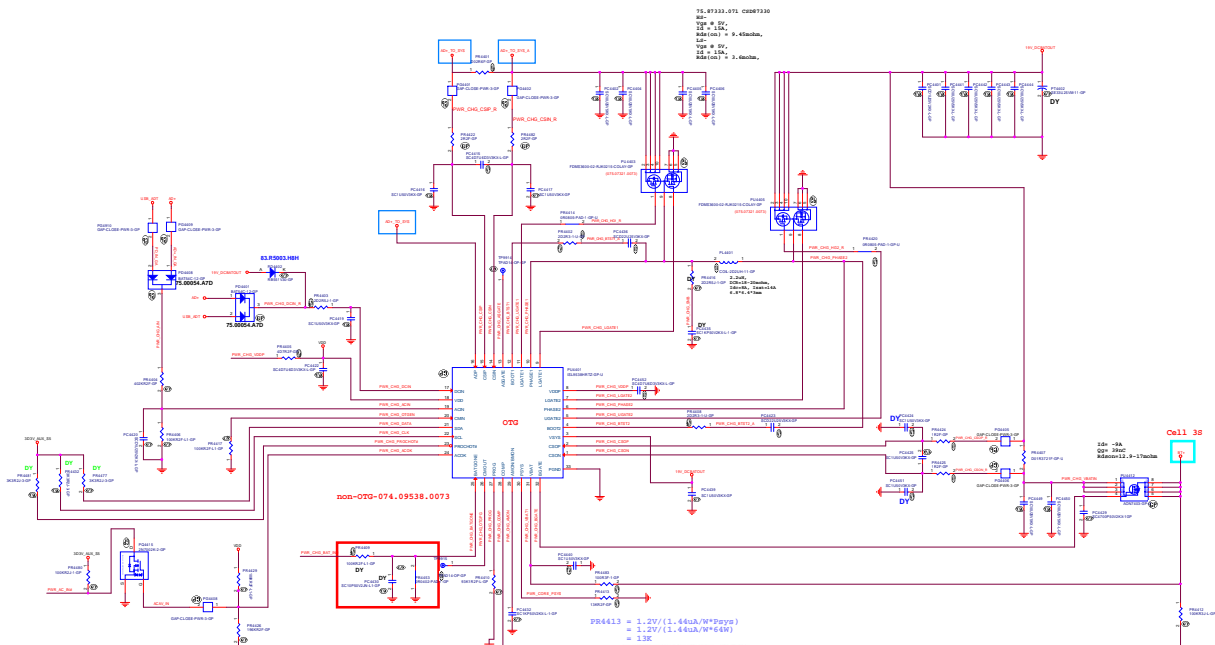
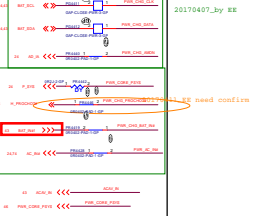
Unicorn LV530 KBL MB SA

Rev

Date: Friday, December 15, 2017

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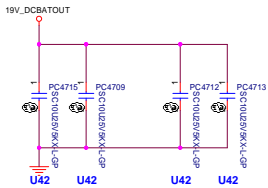
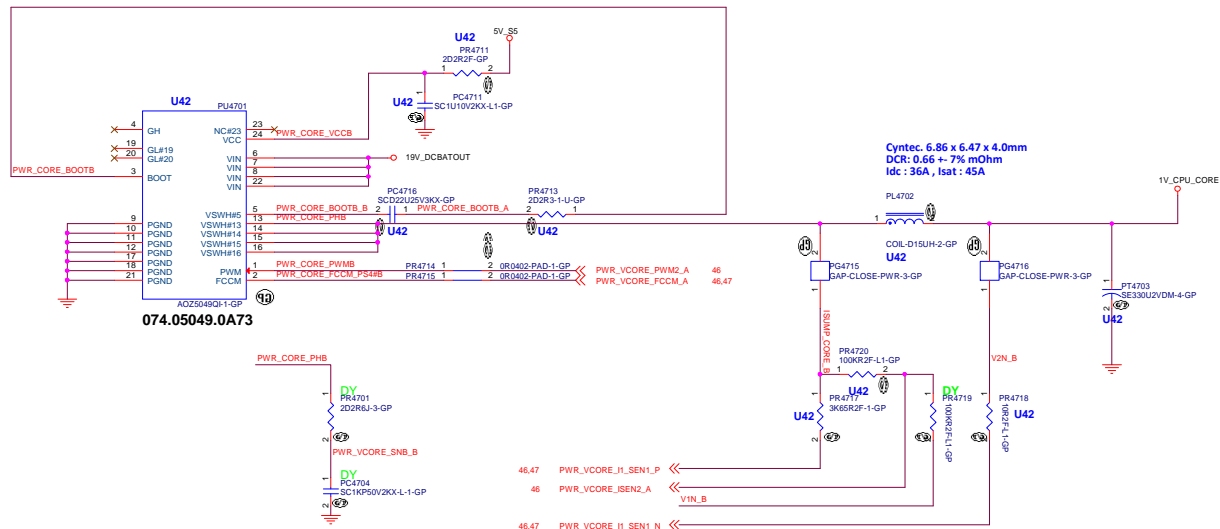
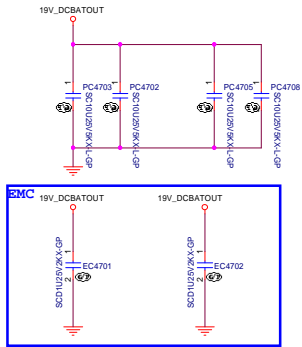
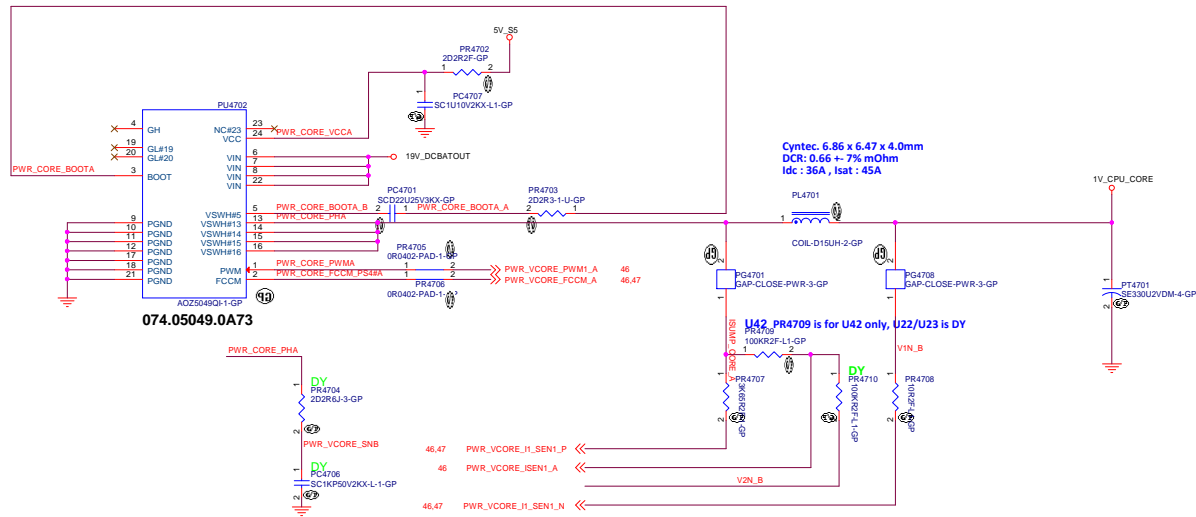
21_07111_071_C008730
 V_{IN} = 5V
 V_{OUT} = 1.1V
 I_{OUT}(MAX) = 1.44A
 V_{IN} = 5V
 I_{OUT}(MAX) = 1.44A

PR4413 = 1.2V / (1.44A * 0.001) = 1.2V / 0.00144 = 833.33Ω

TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROGRAM RESISTANCE (Ω)	MIN	MAX	CELLS	DEFAULT SETTINGS	PROGRAMMING	DEFAULT ACQUIRE TIME(A)
0	0	1	1	730Hz	No	0.476
8.46	8.46	1	1	730Hz	No	1.5
14.7	14.7	1	1	1MHz	No	1.5
21.0	21.0	1	1	1MHz	No	0.476
28.0	28.0	1	1	730Hz	Yes	0.476
35.7	35.7	1	1	730Hz	Yes	1.5
43.2	43.2	2	2	730Hz	Yes	1.5
52.8	52.8	2	2	730Hz	Yes	0.476
61.9	61.9	2	2	1MHz	No	0.476
71.5	71.5	2	2	1MHz	No	1.5
82.5	82.5	2	2	730Hz	No	1.5
93.1	93.1	2	2	730Hz	No	0.476
105	105	3	3	730Hz	No	0.476
118	118	3	3	730Hz	No	1.5
133	133	3	3	1MHz	No	1.5
147	147	3	3	1MHz	No	0.476
162	162	3	3	730Hz	Yes	0.476
178	178	3	3	730Hz	Yes	1.5
196	196	4	4	730Hz	Yes	1.5
215	215	4	4	730Hz	Yes	0.476
237	237	4	4	1MHz	No	0.476
261	261	4	4	1MHz	No	1.5
287	287	4	4	730Hz	No	1.5
316	316	4	4	730Hz	No	0.476
348	348	1	1	730Hz	No	0.476

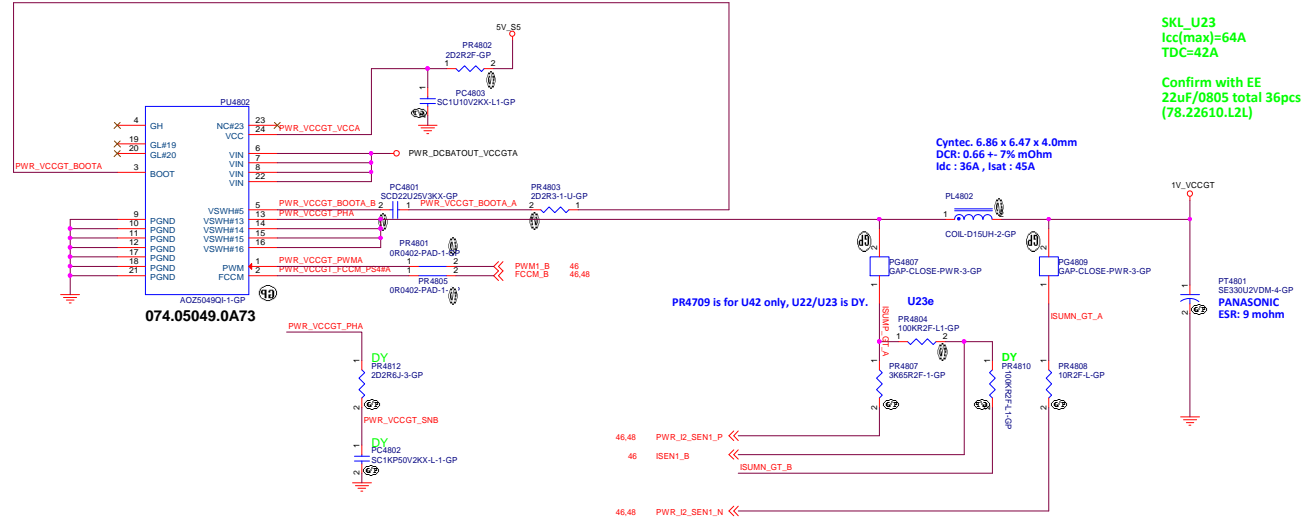
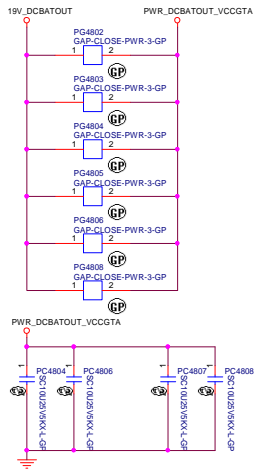
Wateon Corporation
 CHARGER(S142)HW72
 Unicorn LV530 KBL MS1500L



<Variant Name>

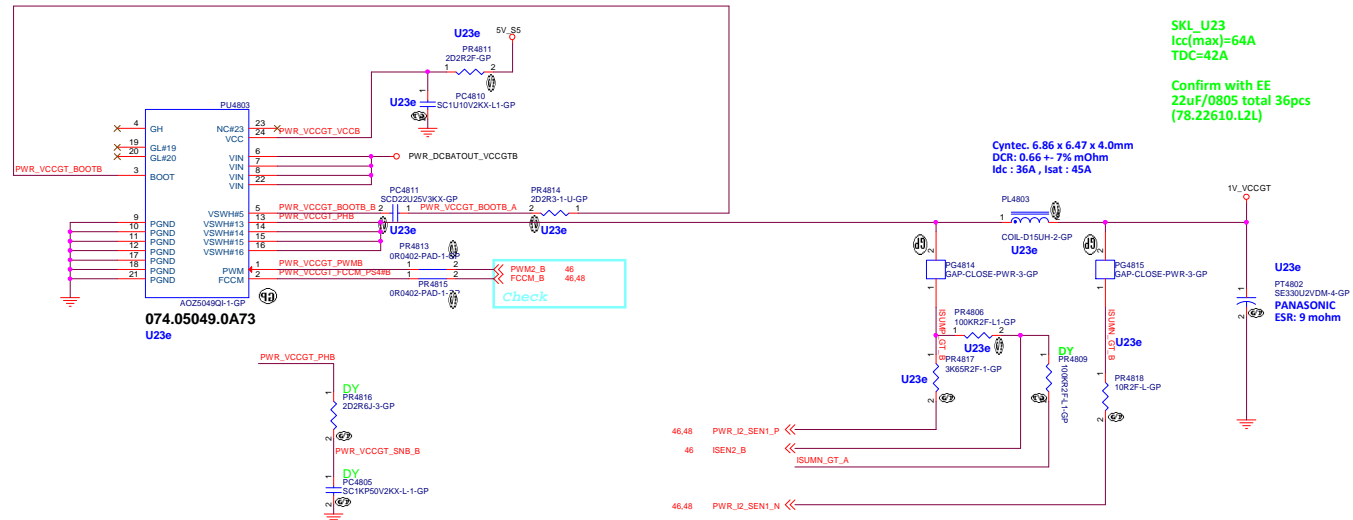
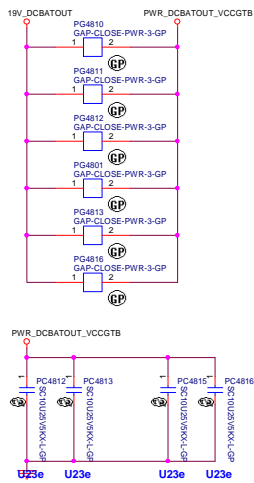
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

Title		SIC631CD CPU VCORE(2/3)	
Size	Document Number	Rev	
A2	Unicorn LV530 KBL MB	1	
Date:	Friday, December 15, 2017	Sheet	47 of 105



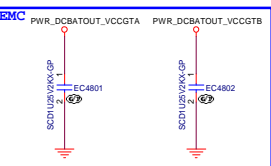
SKL_U23
Icc(max)=64A
TDC=42A

Confirm with EE
22uF/0805 total 36pcs
(78.22610.L2L)



SKL_U23
Icc(max)=64A
TDC=42A

Confirm with EE
22uF/0805 total 36pcs
(78.22610.L2L)



(Blanking)

<Variant Name>

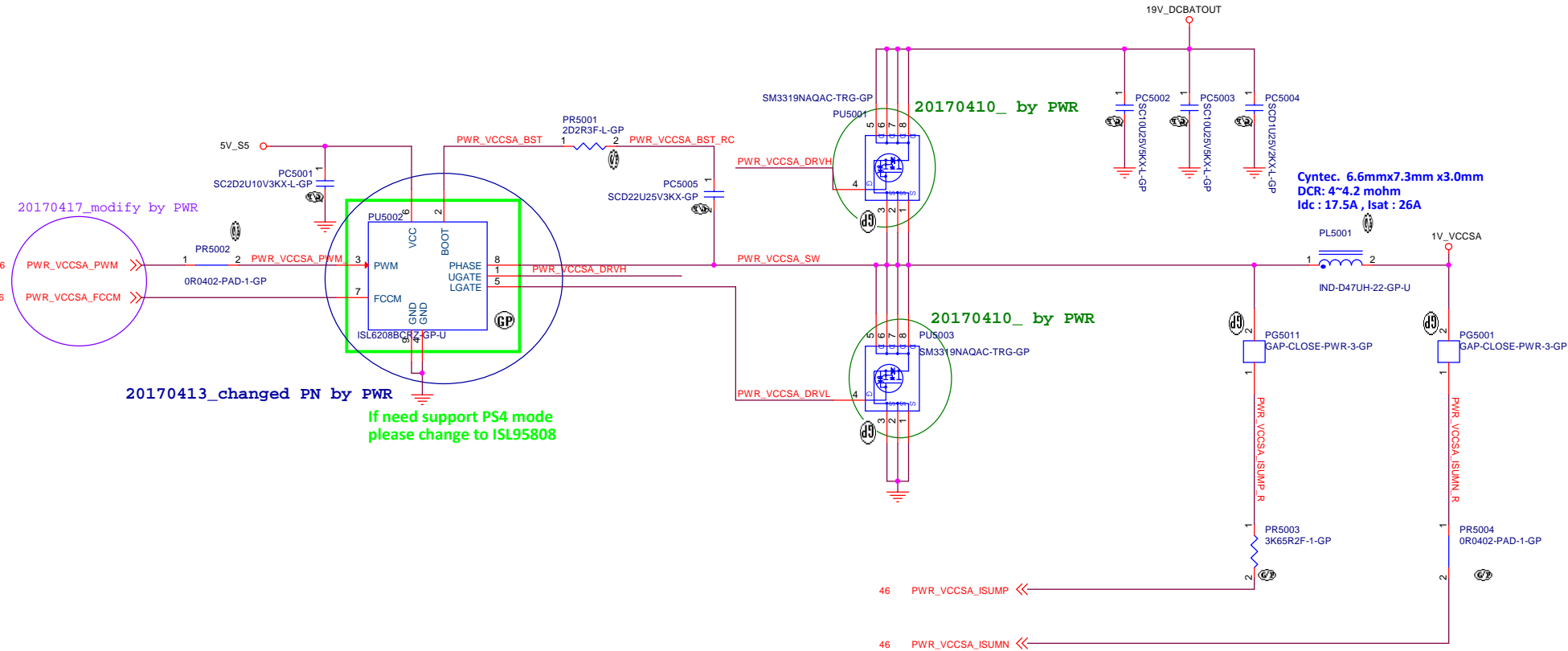
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **CPU_VCCGTUS**

Size A4	Document Number Unicorn LV530 KBL MB GA	Rev GA
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Date: Friday, December 15, 2017 Sheet 49 of 105

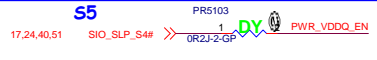
Main Func = CPU_CORE



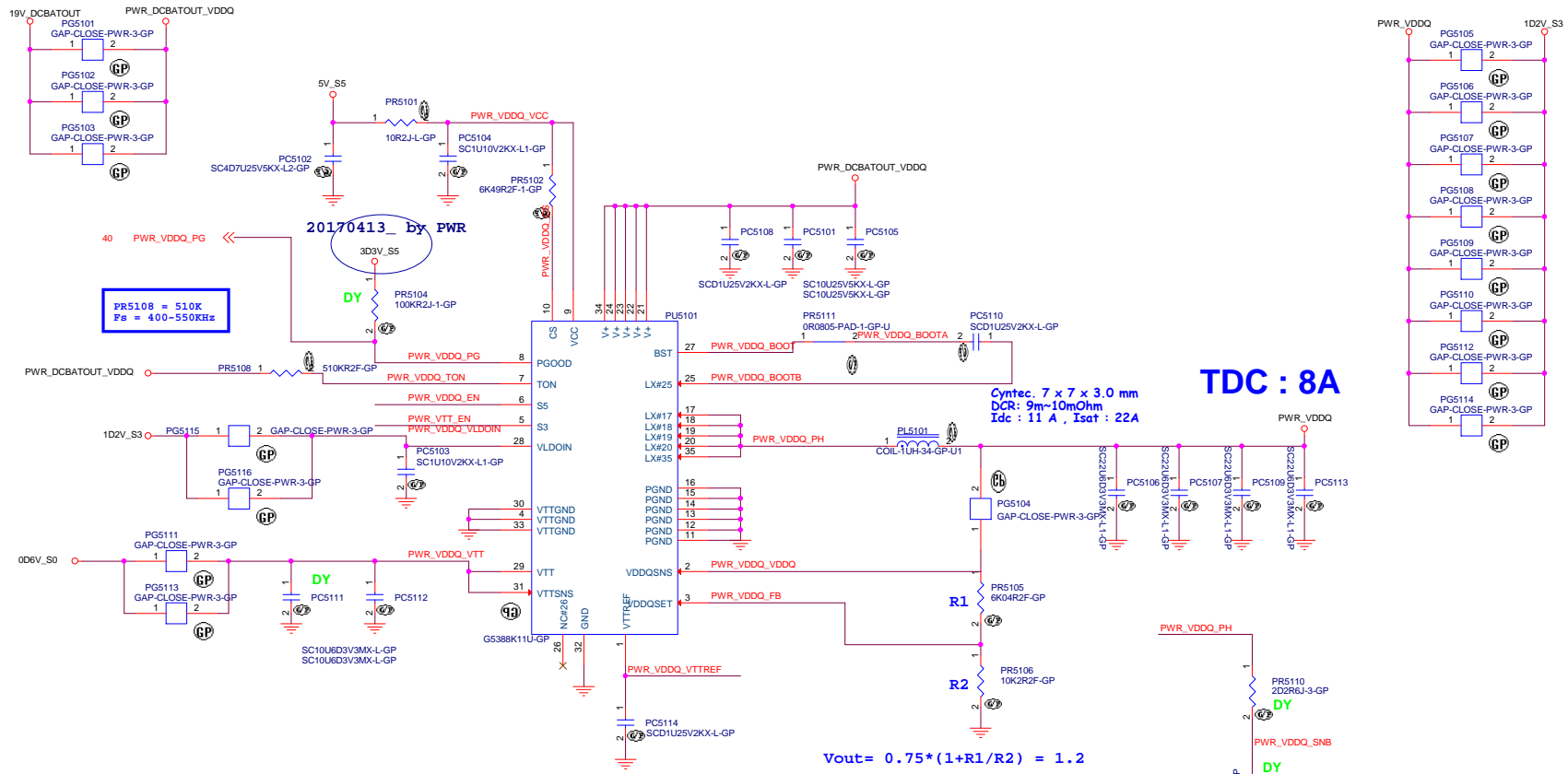
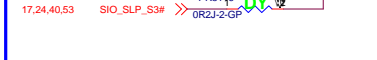
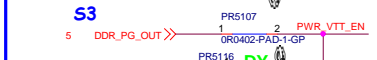
Cyntec. 6.6mmx7.3mm x3.0mm
DCR: 4~4.2 mohm
I_{dc} : 17.5A , Isat : 26A

OFFPAGE

S5



S3



20170413 by PWR

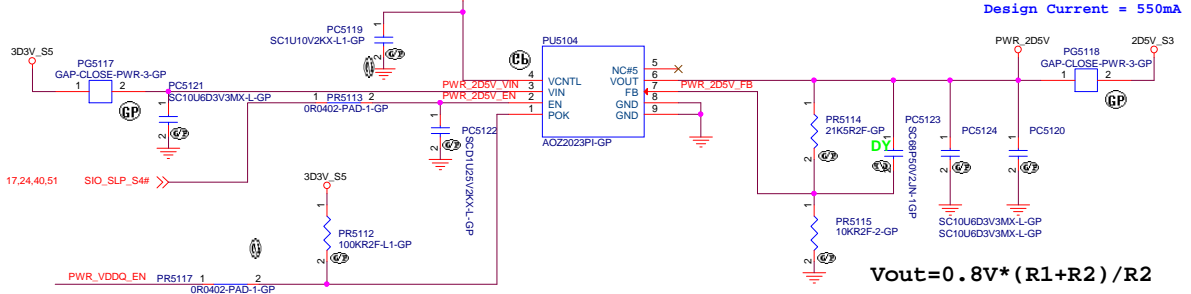
PR5108 = 510K
Fs = 400-550KHz

Cyntec, 7 x 7 x 3.0 mm
DCR: 9m-10mOhm
Idc : 11 A , Isat : 22A

TDC : 8A

$$V_{out} = 0.75 * (1 + R1/R2) = 1.2$$

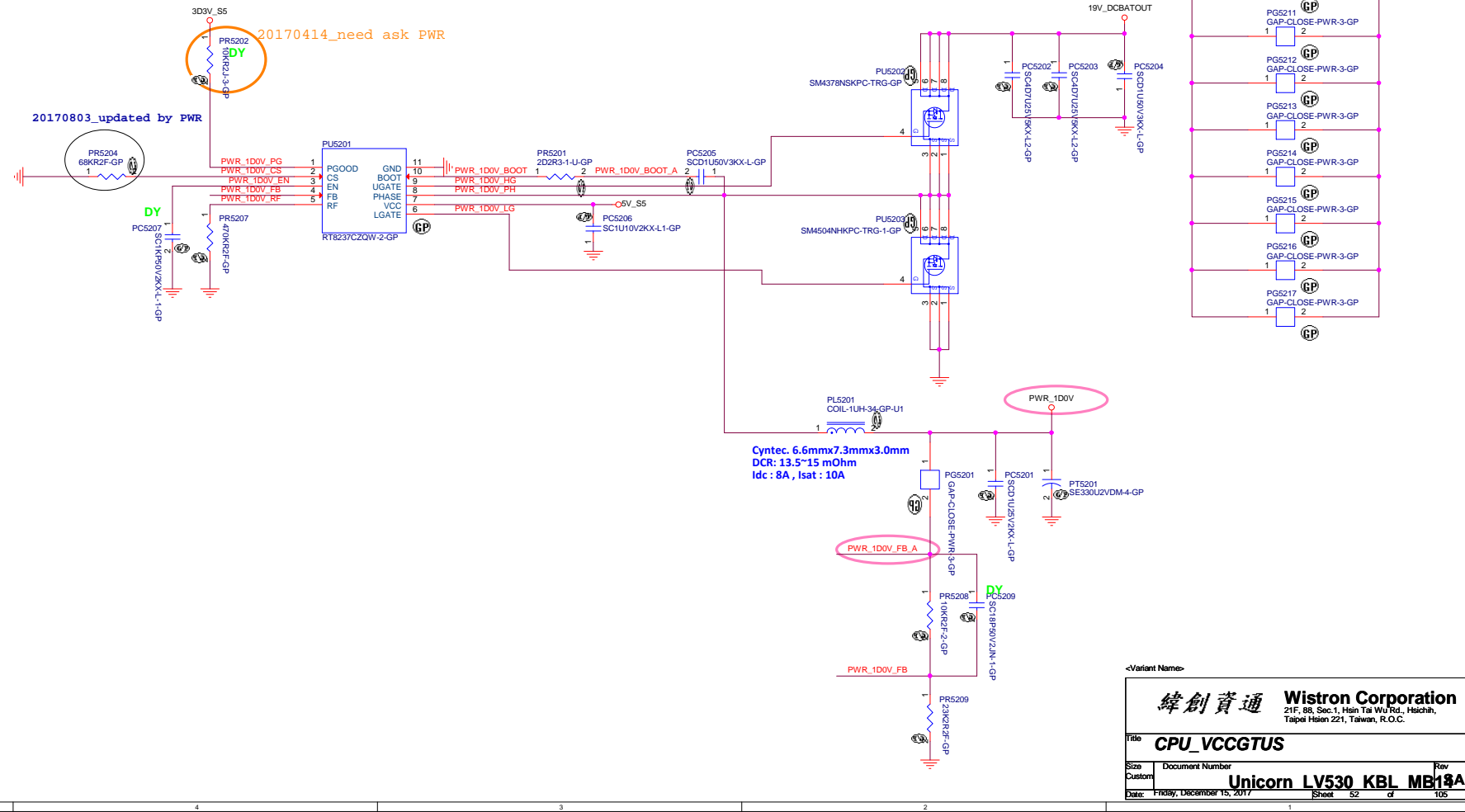
RT9025 for 2D5V



Design Current = 550mA

$$V_{out} = 0.8V * (R1 + R2) / R2$$

BOM1	
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title G5388_VDDQ	
Size Custom	Document Number Unicorn LV530 KBL MB18A
Date: Friday, December 15, 2017	Rev 105
Sheet 51	of 105



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Trd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

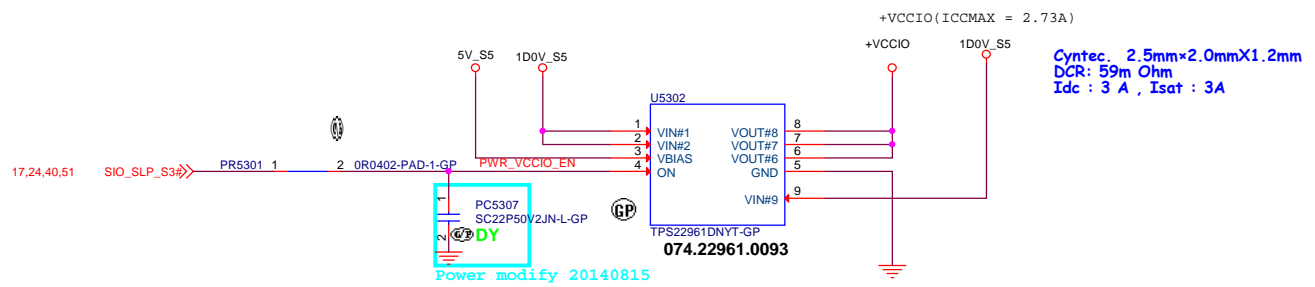
File: CPU_VCCGTUS

Size: Custom Document Number: Unicorn LV530 KBL MB14A Rev:

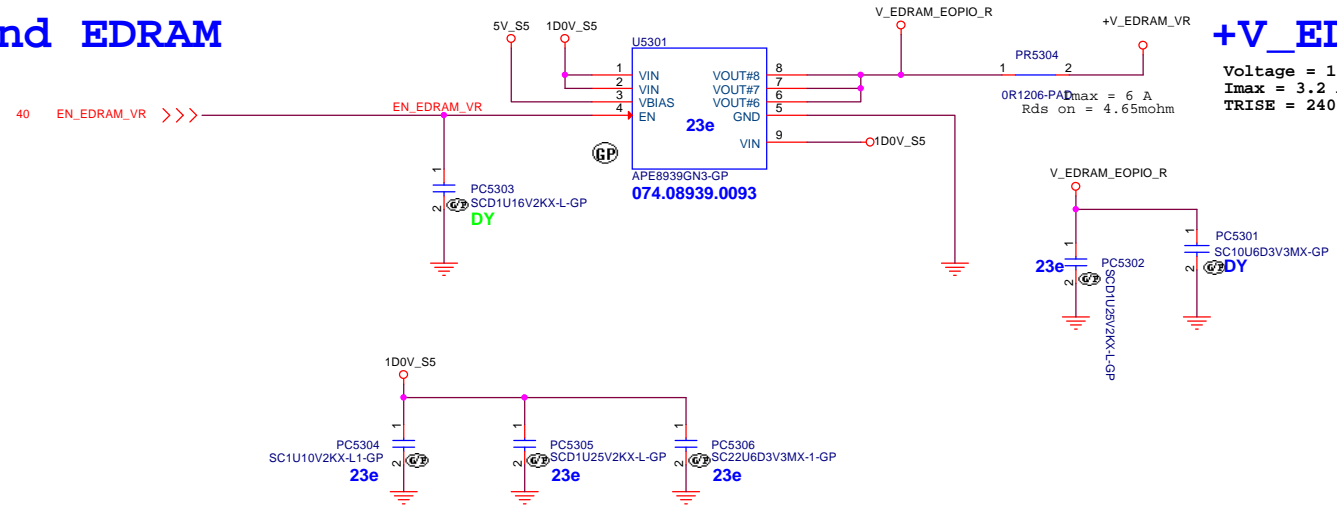
Date: Friday, December 15, 2017 Sheet: 52 of 105

Main Func = 1D0V

VCCIO



EOPIO and EDRAM



+V_EDRAM_VR

Voltage = 1.0 V ± 50 mV
 Imax = 3.2 A
 TRISE = 240 us

+V_EOPIO_VR

Voltage = 1.0 V ± 50 mV
 Imax = 2.8 A
 TRISE = 240 us

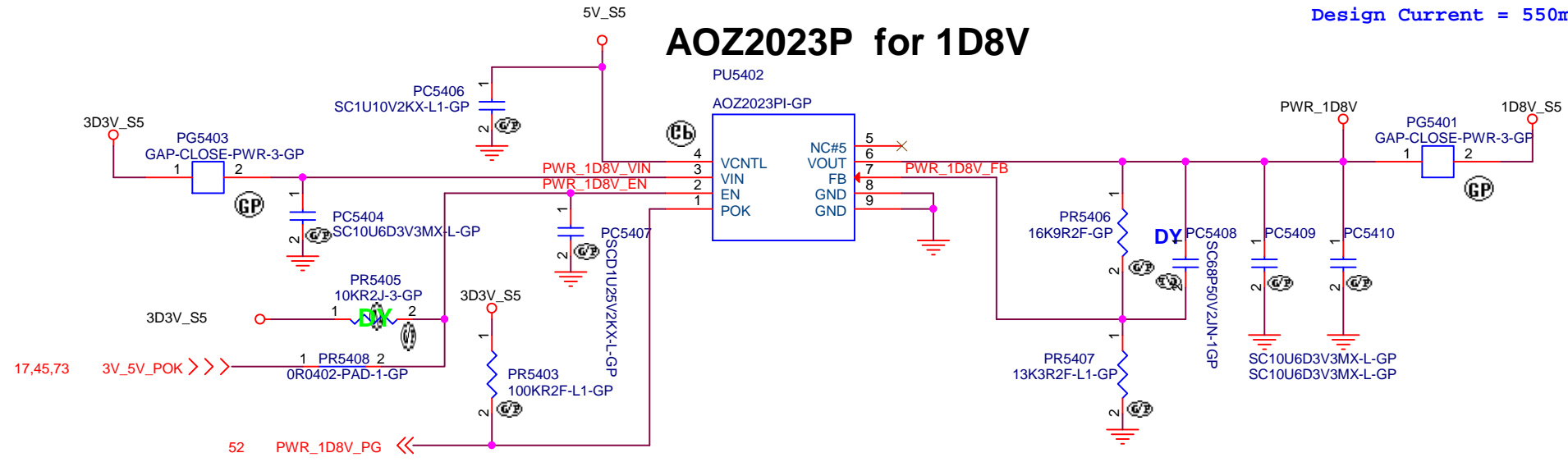


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Title TPS2296 VCCIO&VCCPRIM		
Size A3	Document Number Unicorn_LV530_KBL_MB14	Rev SA
Date: Friday, December 15, 2017	Sheet 53	of 105

Main Func = 1D8V

Design Current = 550mA

AOZ2023P for 1D8V

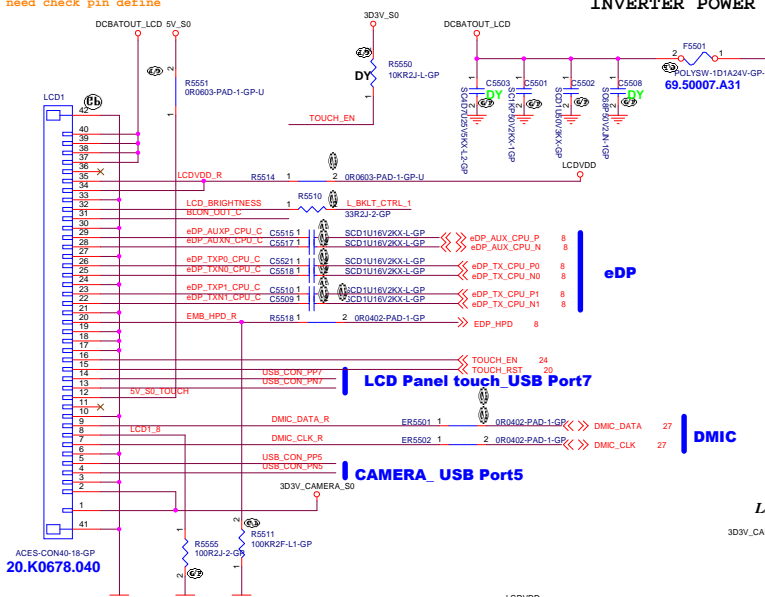


$V_{out} = 0.8V * (R1 + R2) / R2$
 <Variant Name>

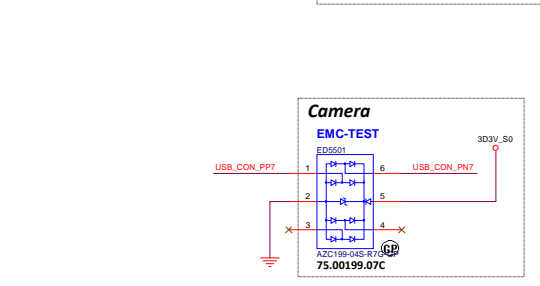
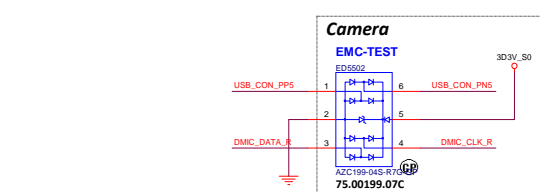
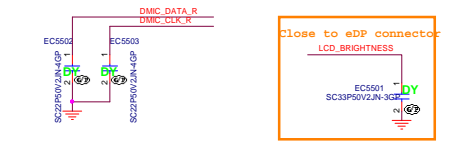
緯創資通 **Wistron Corporation**
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 Taipei Hsien 221, Taiwan, R.O.C.

Title		
RT9025 1D8V		
Size	Document Number	Rev
A4	Unicorn LV530 KBL MB GA	
Date	Friday, December 15, 2017	Sheet 54 of 105

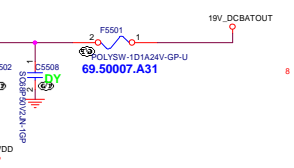
SSID = VIDEO
 20170427
 need check pin define



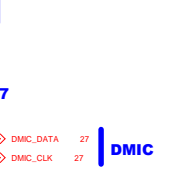
2) 3 empty-pins between wire cable(MIC, camera, or other control signals) & coaxial cable(LCD panel usage). (Apply to LNB only)



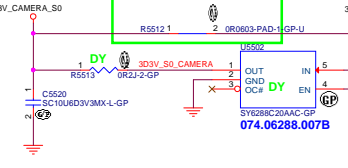
INVERTER POWER



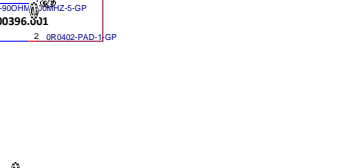
eDP



CAMERA POWER



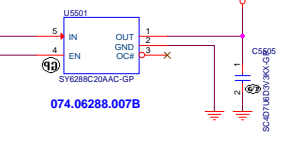
CAMERA_USB Port5



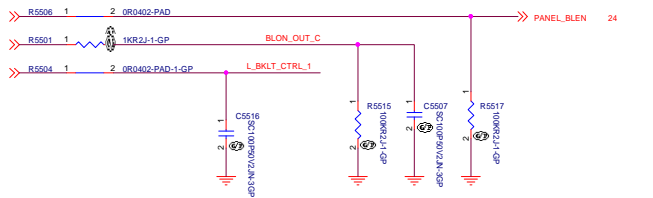
LCD Panel touch USB Port7



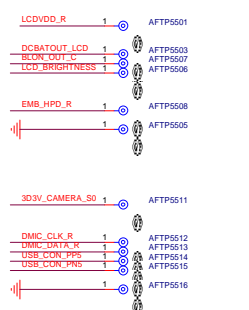
Layout 40 mil

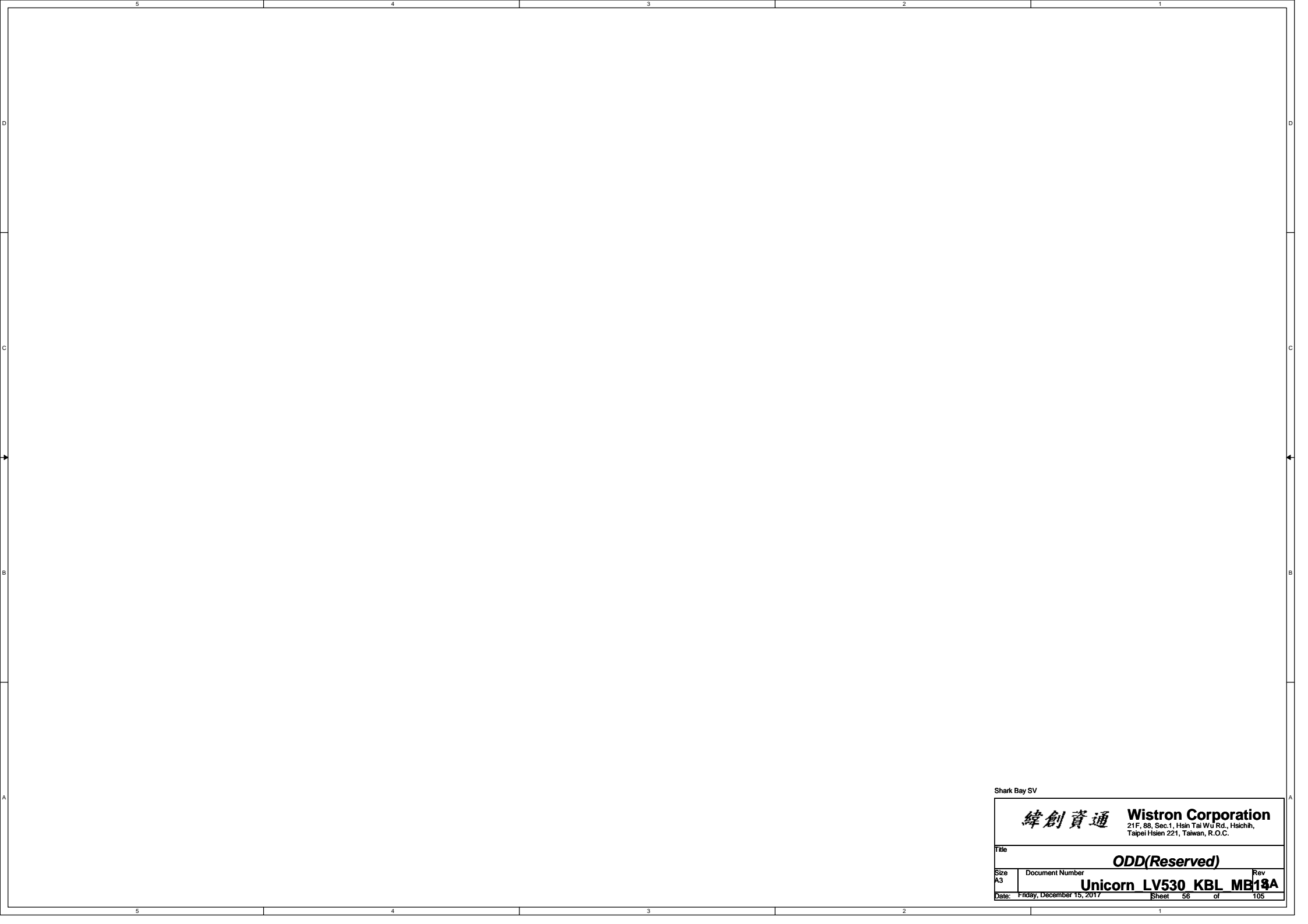


Panel BL brightness/Power En/BL En



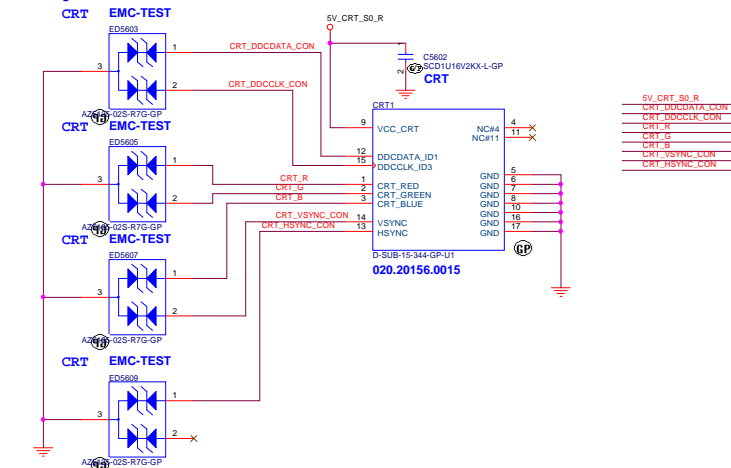
Test point



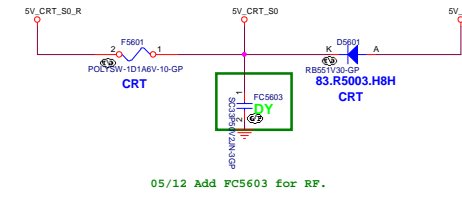


Shark Bay SV

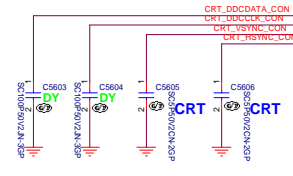
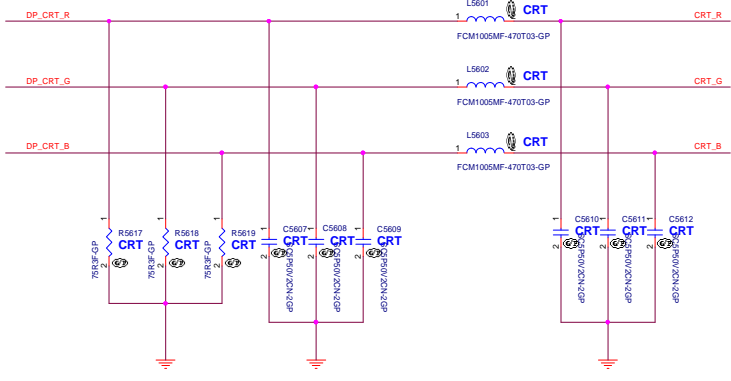
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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ODD(Reserved)			
Size	Document Number	Rev	
A3		Unicorn LV530 KBL MB13A	
Date: Friday, December 15, 2017		Sheet	56 of 105



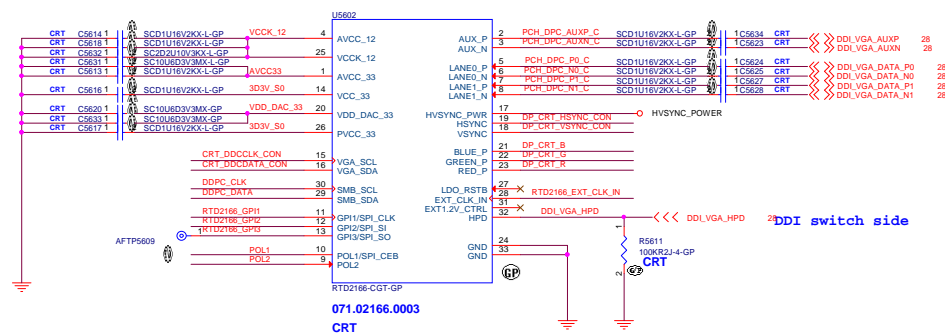
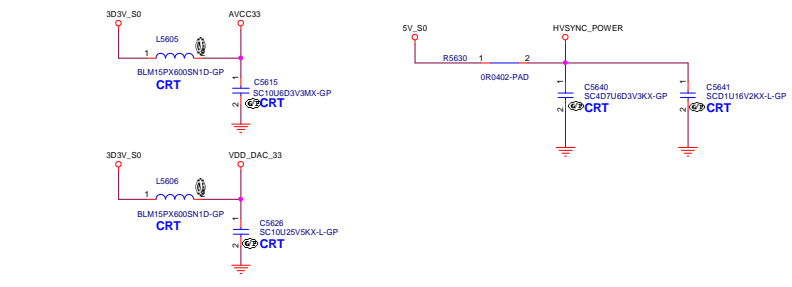
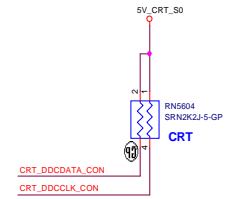
5V_CRT_S0_R	1	AFTP5601
CRT_DDCDATA_CON	1	AFTP5602
CRT_DDCCLK_CON	1	AFTP5603
CRT_G	1	AFTP5604
CRT_B	1	AFTP5605
CRT_VSYNC_CON	1	AFTP5606
CRT_HSYNC_CON	1	AFTP5607
	1	AFTP5608



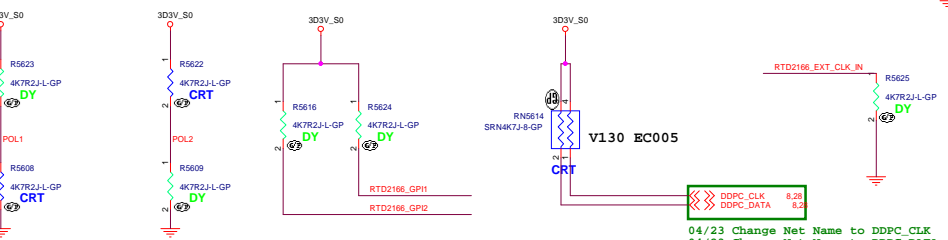
05/12 Add FC5603 for RF.



LAYOUT NOTE:
 All cap need close to chip
 especially C616 close pin5
 C618 and C619 close pin19
 C620 and C621 close pin9
 C617 close pin20
 C614 close pin25
 C613 lose pin24



DDI switch side



04/23 Change Net Name to DDPC_CLK
 04/23 Change Net Name to DDPC_DATA

(Blank)

BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size
A4

Document Number

Unicorn LV530 KBL MB SA

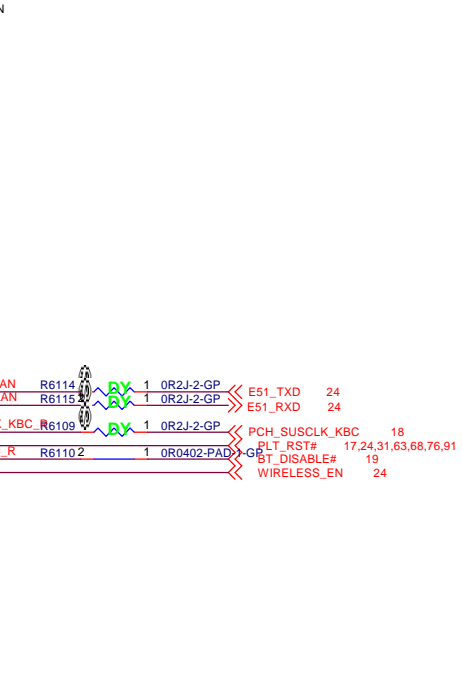
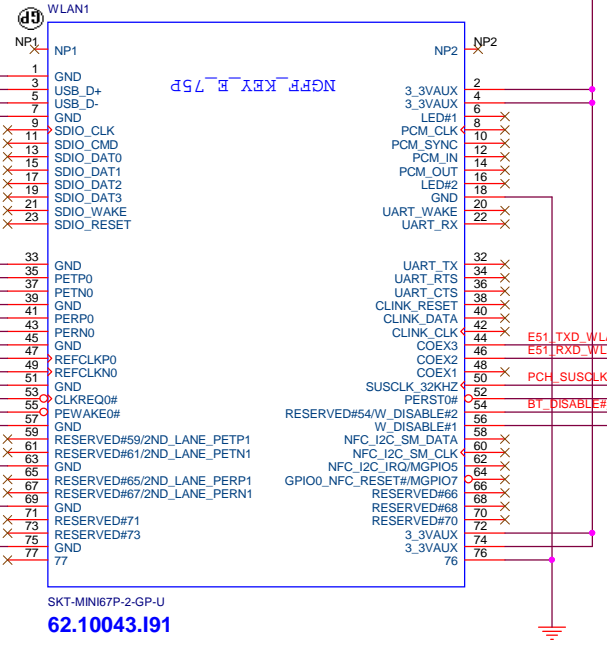
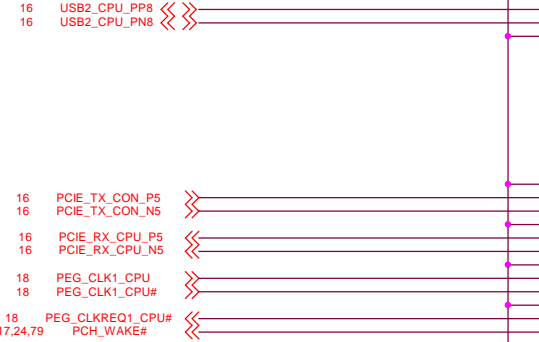
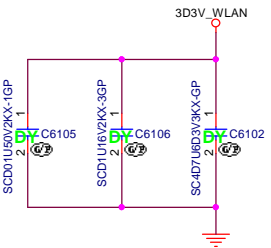
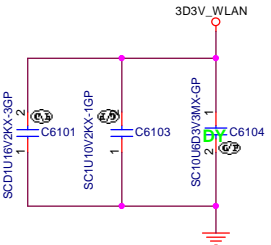
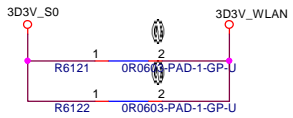
Rev

Date: Friday, December 15, 2017

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M.2 Key-E FOR WLAN / BT

2.5A peak
1.1A Cont



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BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size
A4

Document Number

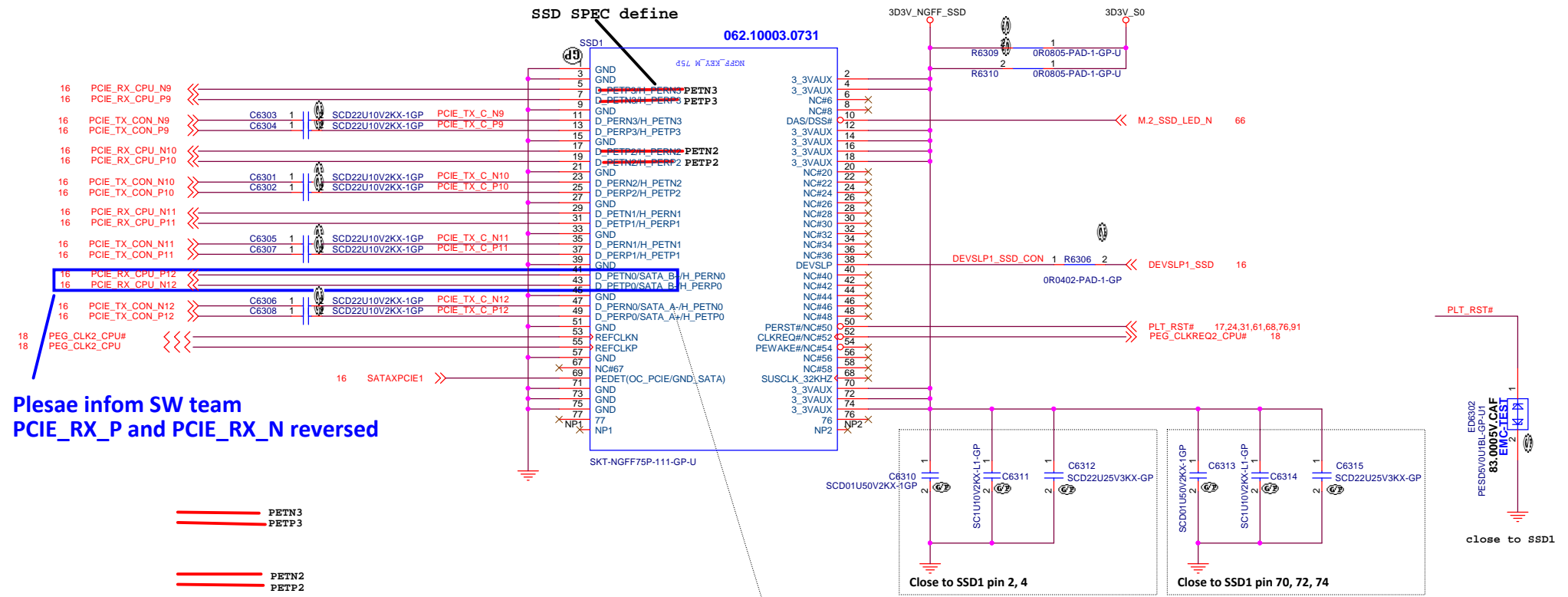
Unicorn LV530 KBL MB SA

Rev

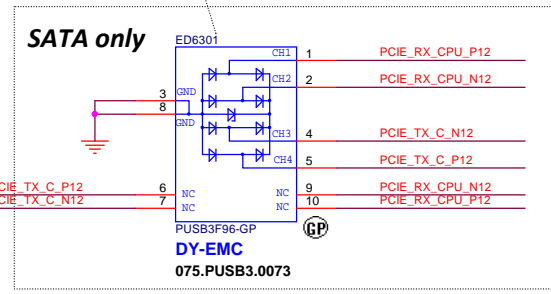
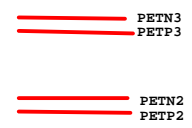
Date: Friday, December 15, 2017

Sheet 62 of 105

Main Func = SSD TYPE-M NGFF CARD FOR PCIE SSD/Optane



**Please inform SW team
PCIE_RX_P and PCIE_RX_N reversed**



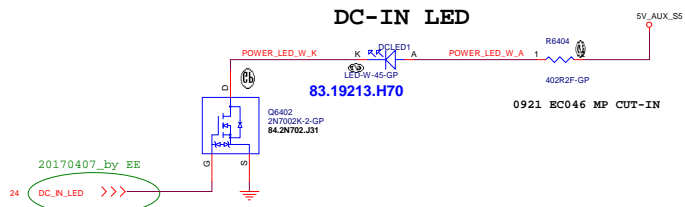
BOM1

緯創資通 Wistron Corporation
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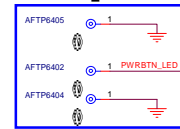
Title: **M.2 SSD SLOT**

Size: A3
Document Number: **Unicorn LV530_KBL_MB14**
Date: Friday, December 15, 2017

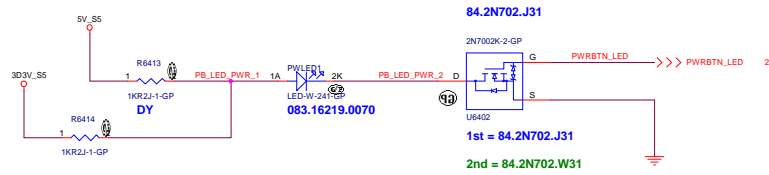
Rev: SA
Sheet: 63 of 105



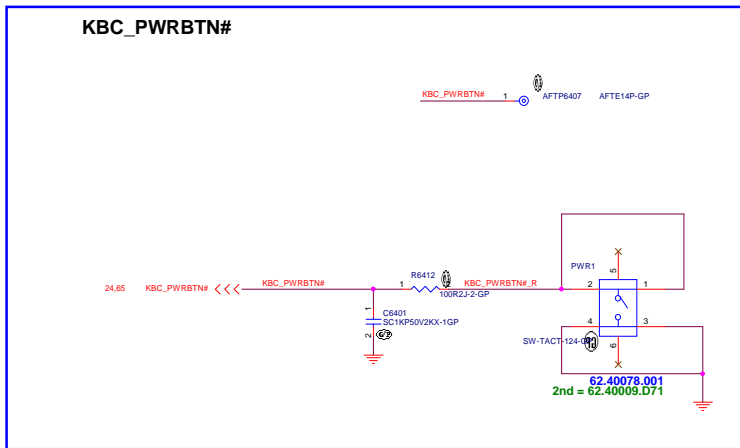
Test point



POWER BTN LED



KBC_PWRBTN#



BOM1

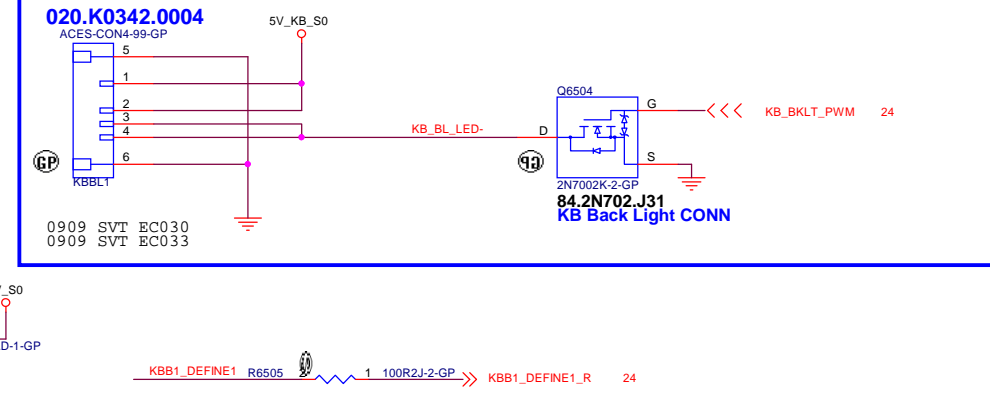
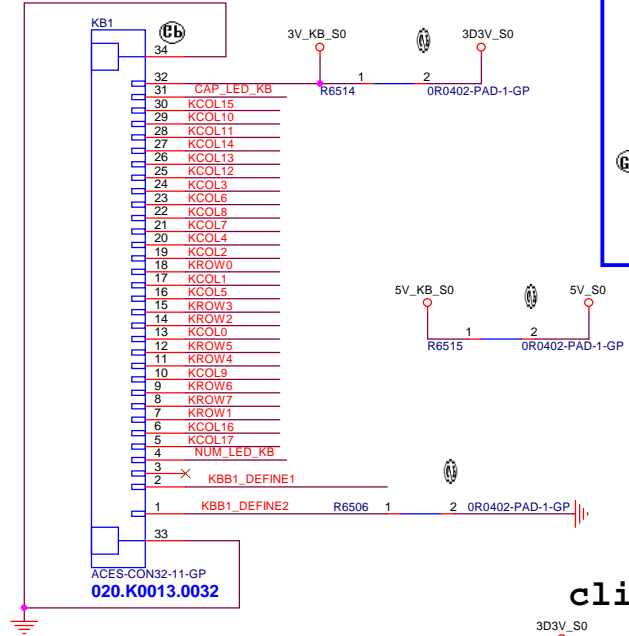
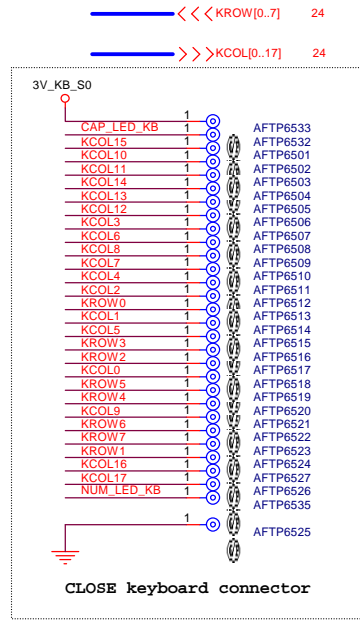
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title LED/POWER BUTTON			
Size A2	Document Number Unicorn LV530_KBL_MB14	Rev. SA	
Date Friday, December 15, 2017	Sheet 64	of 106	

SSID = Touch.Pad

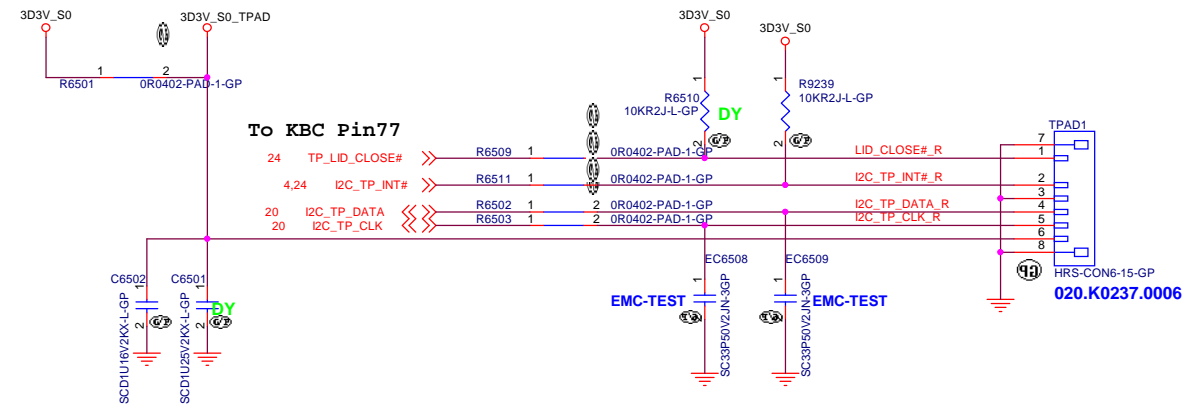
20170427_pin deifne check by Dennis

KB_LED

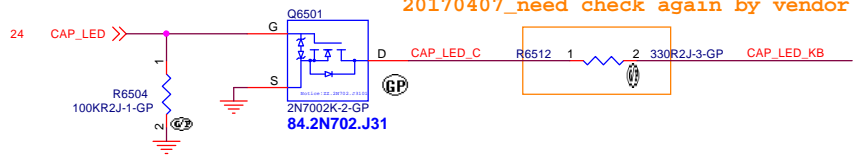


20170421
Change pin define by Dennis

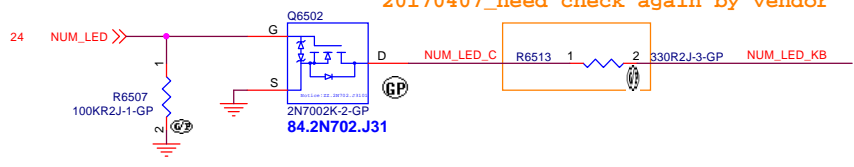
click pad



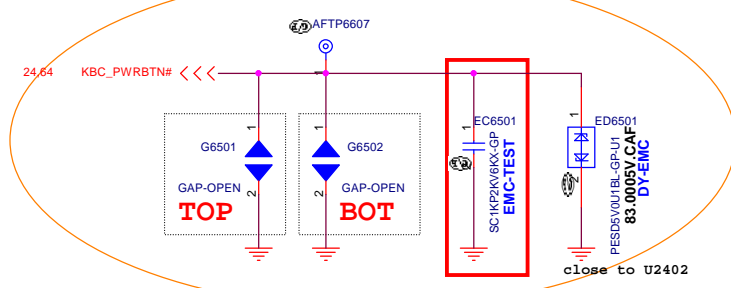
20170407_need check again by vendor



20170407_need check again by vendor



20170412_WKS test by LB720



BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

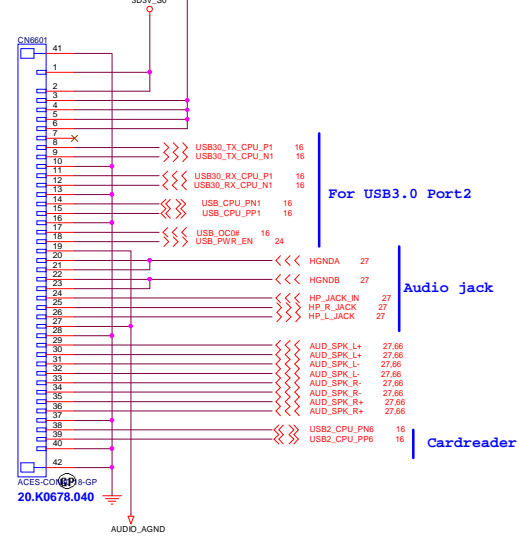
Title
KEYBOARD/TOUCH PAD

Size A3 Document Number
Unicorn LV530 KBL MB14 Rev SA

Date: Friday, December 15, 2017 Sheet 65 of 105

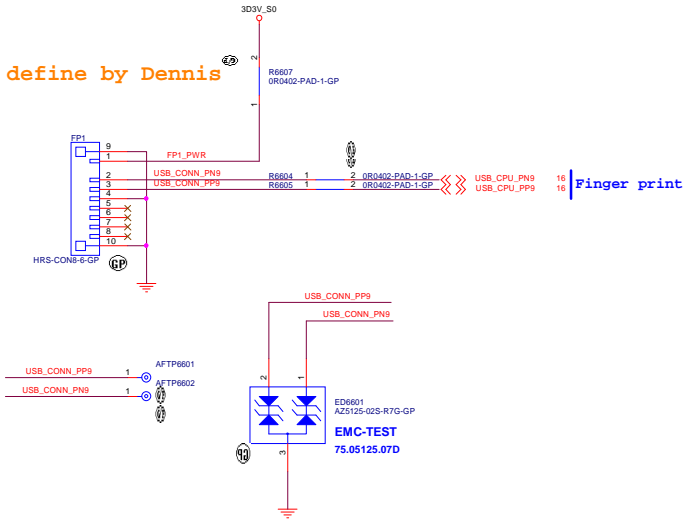
IO CONN

Type A USB3.0 USB Redrive Card reader

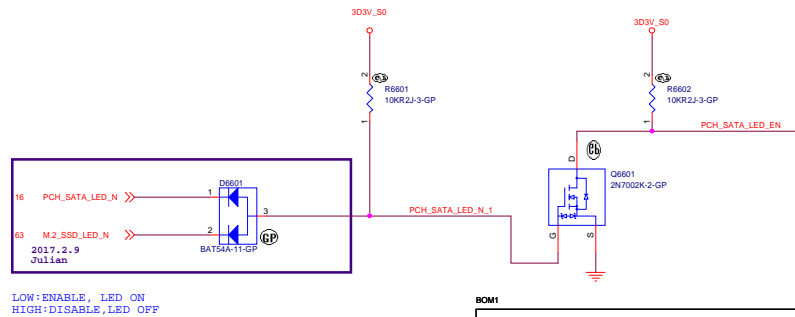
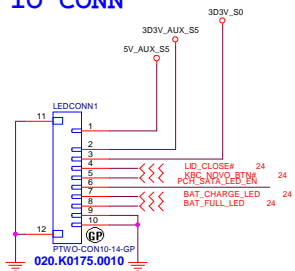


20170421
Change pin define by Dennis

Finger print



LED IO CONN



LOW:ENABLE, LED ON
HIGH:DISABLE,LED OFF

Wistron Corporation 2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.	
Title: LEDIO IO BOARD CONN	
Size: A2	Document Number: Unicom LV530_KBL_MB14
Date: Friday, December 15, 2017	Rev: SA
Sheet 66 of 105	

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BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size
A4

Document Number

Unicorn LV530 KBL MB SA

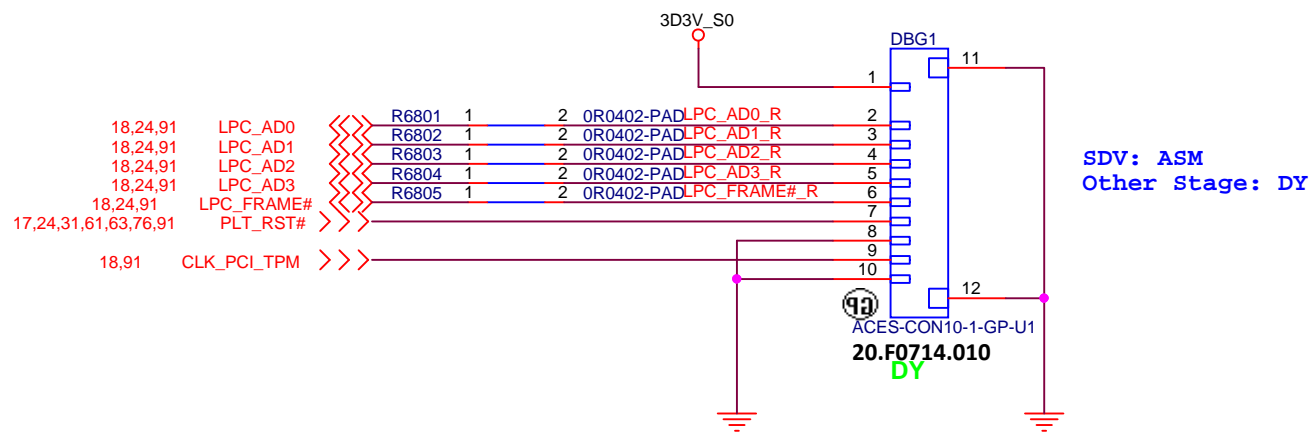
Rev

Date: Friday, December 15, 2017

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Main Func = Debug

Debug Connector



BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DEBUG CONN			
Size	Document Number	Rev	
A4	Unicorn_LV530_KBL_MB14	SA	
Date:	Friday, December 15, 2017	Sheet	68 of 105

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BOM1

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Title

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Size
A4

Document Number

Unicorn LV530 KBL MB SA

Rev

Date: Friday, December 15, 2017

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BOM1

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Title

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Size
A4

Document Number

Unicorn LV530 KBL MB GA

Rev

Date: Friday, December 15, 2017

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BOM1

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Title

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Size
A4

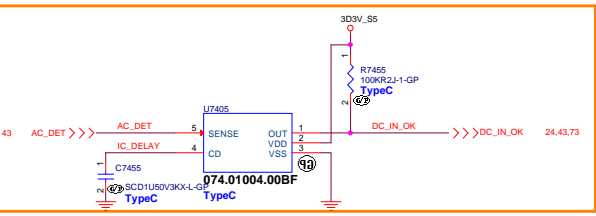
Document Number

Unicorn LV530 KBL MB SA

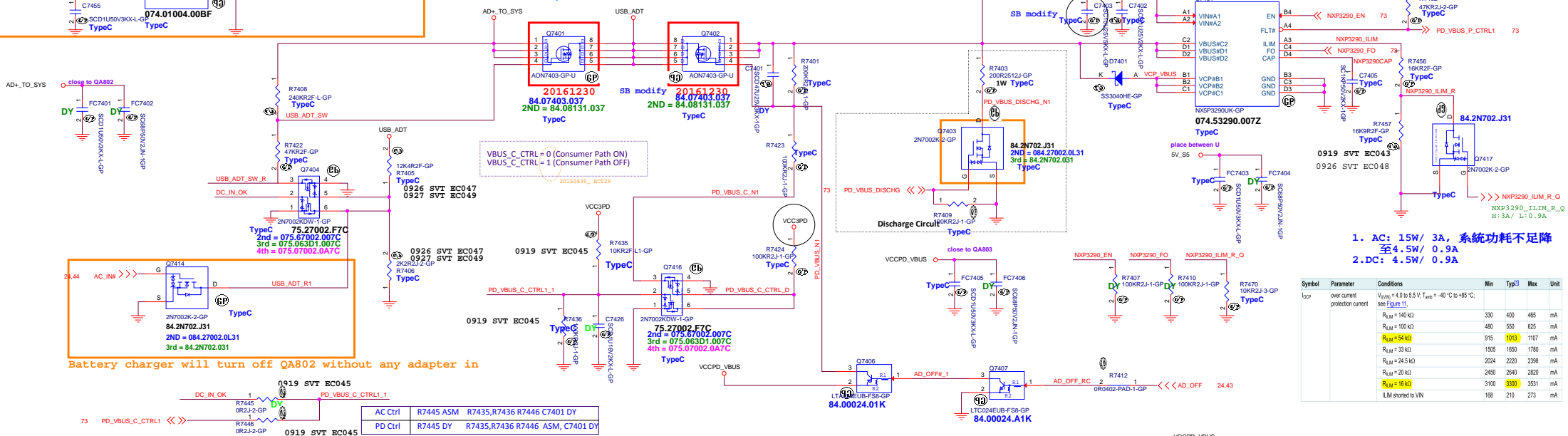
Rev

Date: Friday, December 15, 2017

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USB PD (Consumer: 20V 3.25A, Provider: 5V 2A)

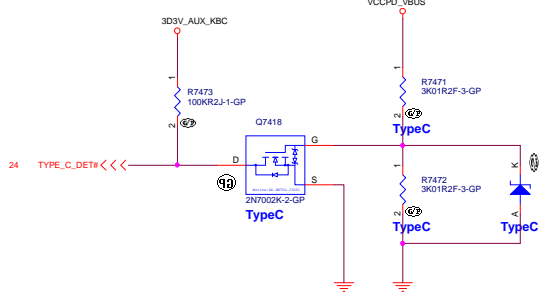


Battery charger will turn off QA802 without any adapter in

1. AC: 15W/ 3A, 系統功耗不足降
至 4.5W/ 0.9A
2. DC: 4.5W/ 0.9A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{over}	over current protection current	V _{IN} = 4.0 to 5.5V, T _{amb} = -40 °C to +85 °C, see Figure 15				
		R _{ILIM} = 140kΩ	330	400	465	mA
		R _{ILIM} = 100kΩ	480	550	625	mA
		R _{ILIM} = 53kΩ	915	1035	1107	mA
		R _{ILIM} = 33kΩ	1595	1650	1760	mA
		R _{ILIM} = 24.5kΩ	2024	2220	2368	mA
	R _{ILIM} = 20kΩ	2450	2640	2820	mA	
	R _{ILIM} = 15kΩ	3100	3330	3531	mA	
		ILIM shorted to VIN	168	210	273	mA

19V Power source type	Control Pin				PMOS Location	Status	Remark
	Net name	Status	Net name	Status			
Normal adapter Only	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	Control by DC_IN_OK
		High	PD_VBUS_C_CTRL1	High	Q7402	OFF	Control by PD_VBUS_C_CTRL1
		ON	PD_VBUS_C_CTRL1	High	PU4302	ON	Control by DC_IN_OK or ACAV_IN
Type-C adapter Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	Low	Q7401	ON	Control by BGATE
		Low	PD_VBUS_C_CTRL1	Low	Q7402	ON	
		OFF	PD_VBUS_C_CTRL1	Low	PU4302	OFF	
Normal adapter + Type-C	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	
		High	PD_VBUS_C_CTRL1	High	Q7402	OFF	
		OFF	PD_VBUS_C_CTRL1	High	PU4302	ON	
Battery Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	High	Q7401	OFF	
		Low	PD_VBUS_C_CTRL1	High	Q7402	OFF	
		OFF	PD_VBUS_C_CTRL1	High	PU4302	OFF	
		ON	PD_VBUS_C_CTRL1	High	PU4412	ON	Battery to 19V_DCBATOUT



BOM1

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Title: **TYPEC PD Controller**

Size: Document Number: **Unicorn LV530_KBL_MB14** Rev: **SA**

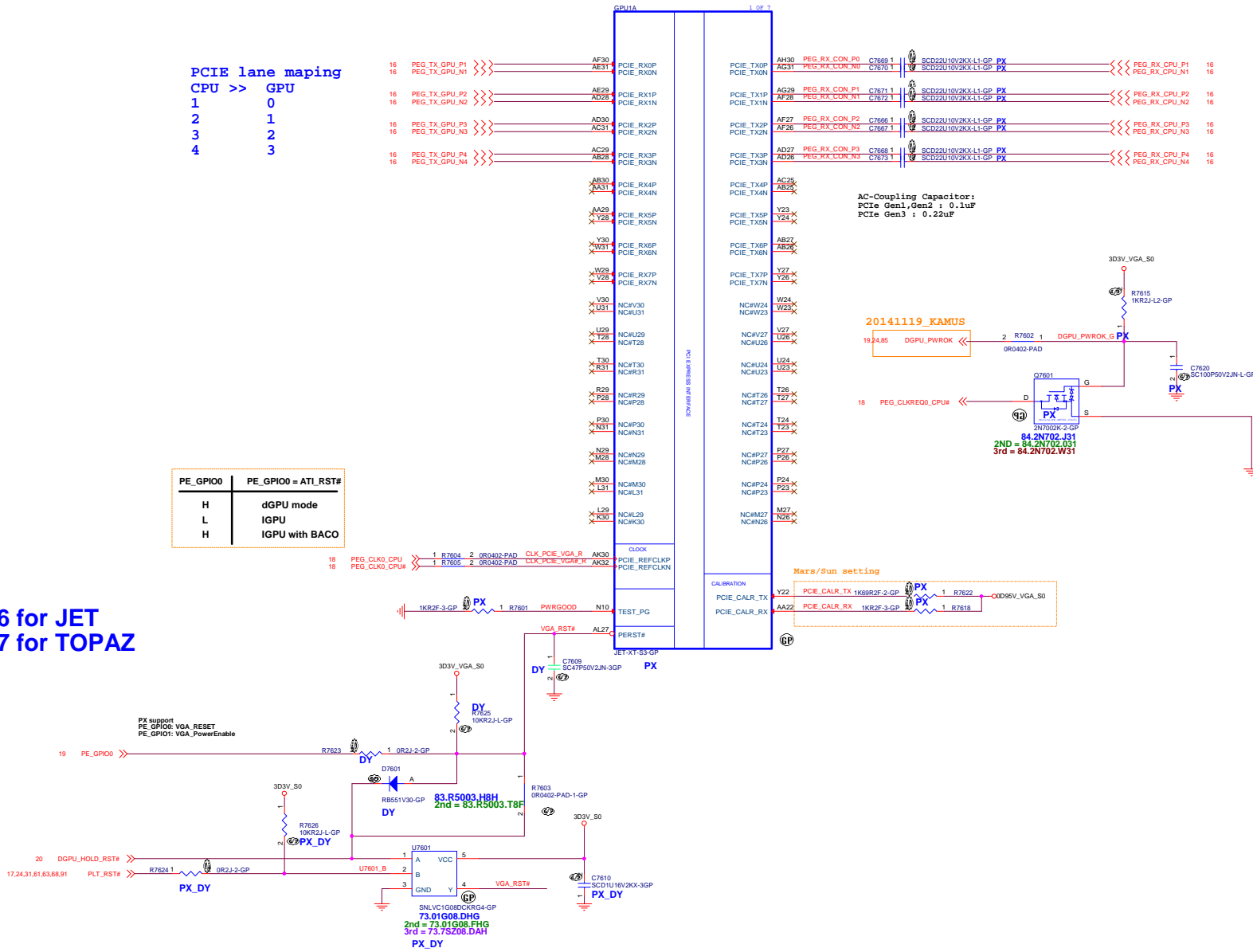
Date: 11/05/2015 2017 Page: 74 of 105

PCIE lane mapping
CPU >> GPU

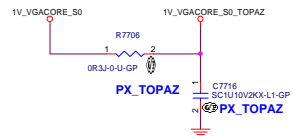
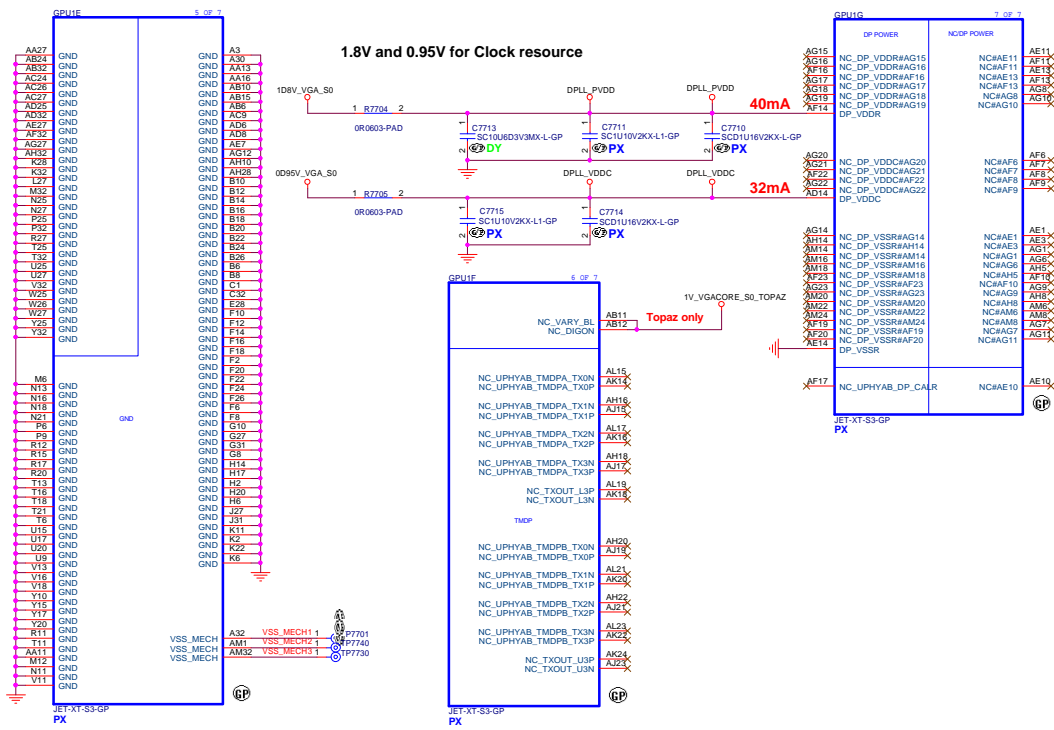
1	0
2	1
3	2
4	3

PE_GPIO0	PE_GPIO0 = ATI_RST#
H	dGPU mode
L	IGPU
H	IGPU with BACO

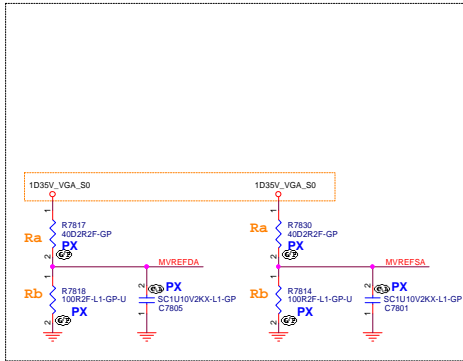
R16 for JET
R17 for TOPAZ



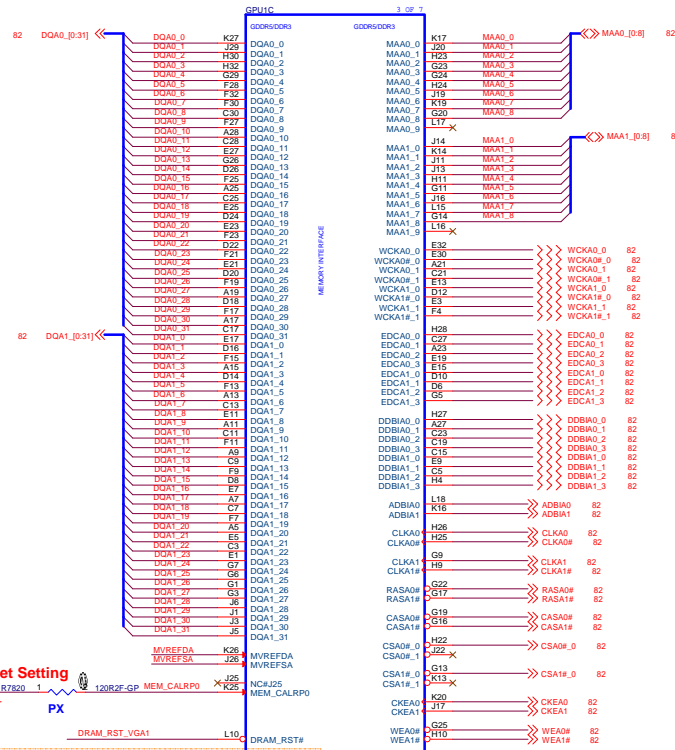
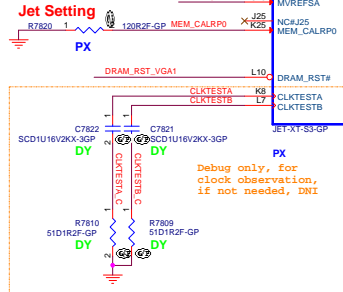
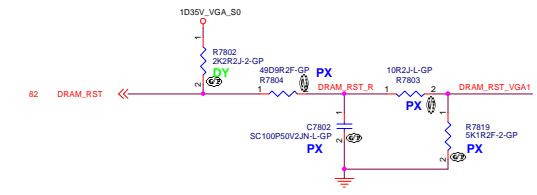
BOM1



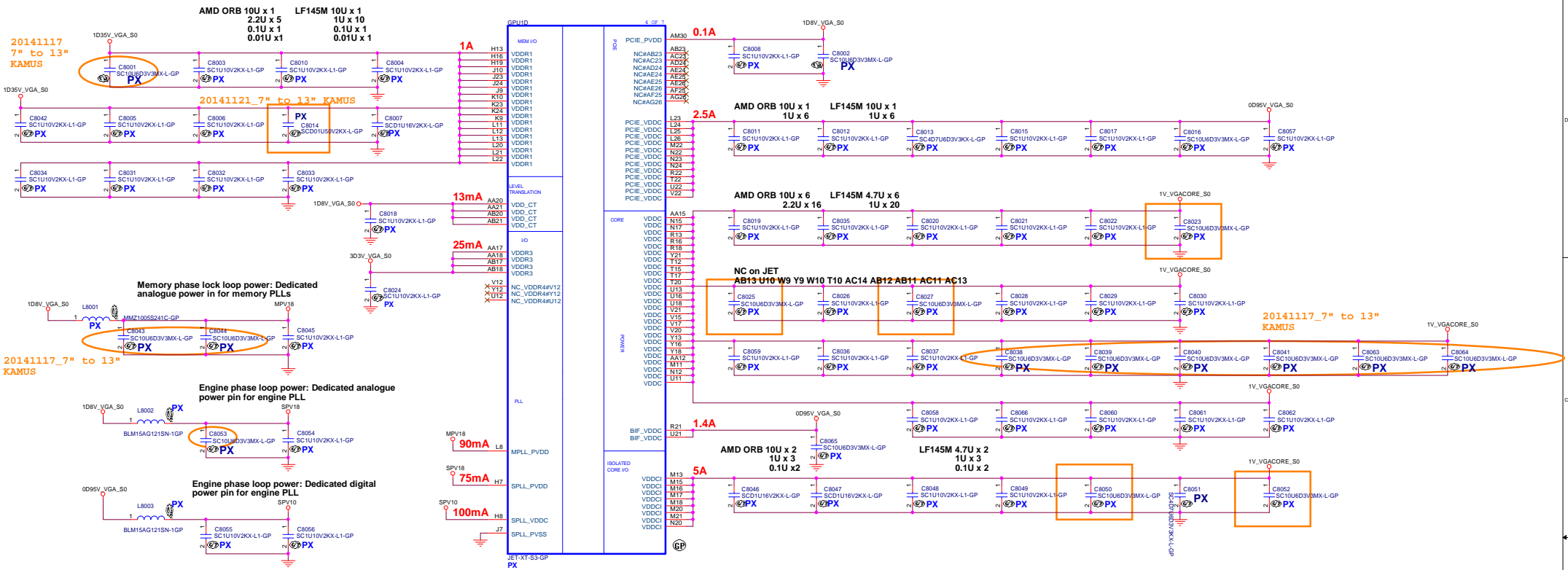
Please MVREF drivers and Caps close to ASIC



Place all these components very close to GPU (within 25mm) and keep all components close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR5



BOM1



5

4

3

2

1

D

D

C

C

B

B

A

A

BOM1

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		<small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
GPU VRAM1.2 (1/4)			
Size C	Document Number Unicorn LV530 KBL MB14	Rev SA	
<small>Date: Friday, December 15, 2017</small>		<small>Sheet 81 of 105</small>	

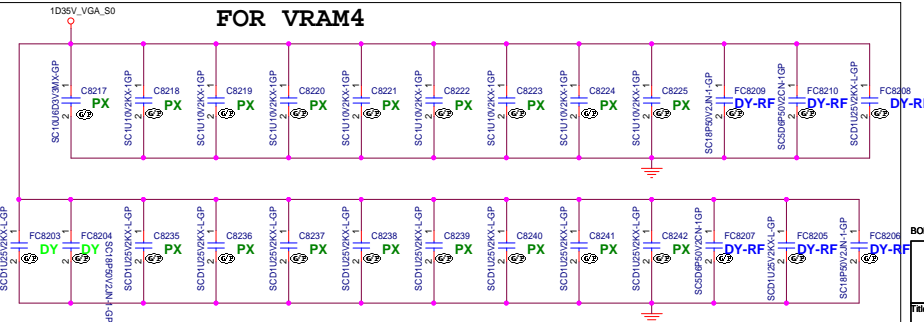
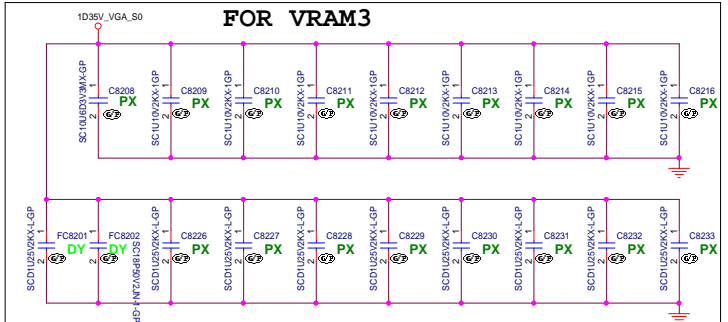
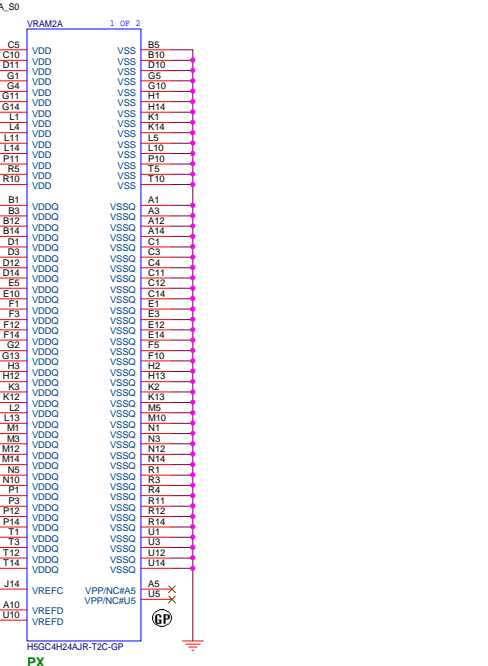
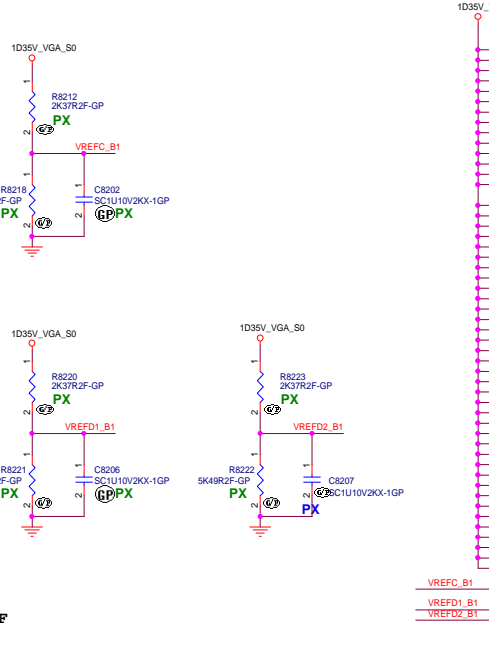
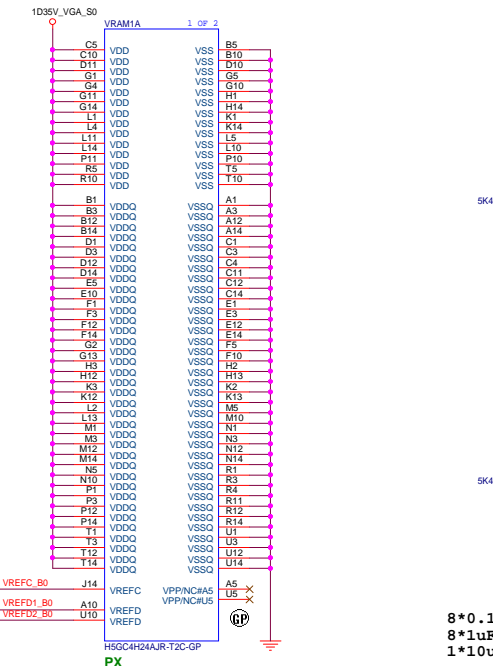
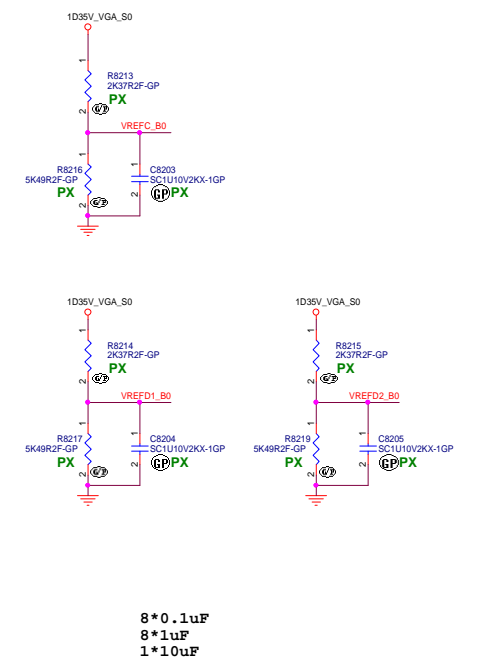
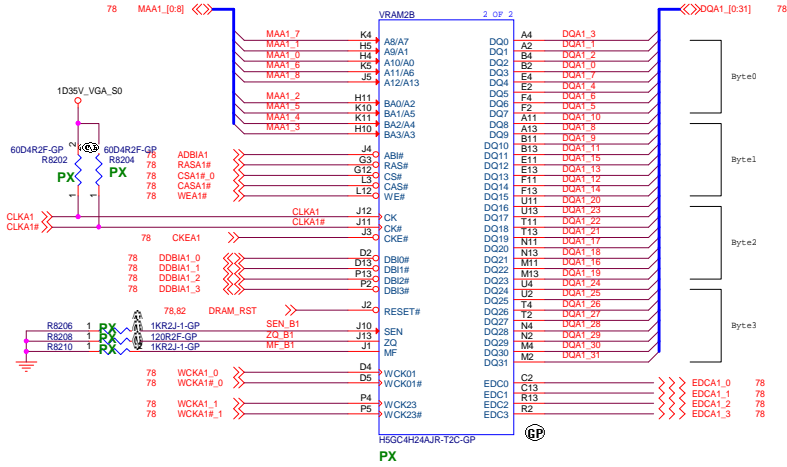
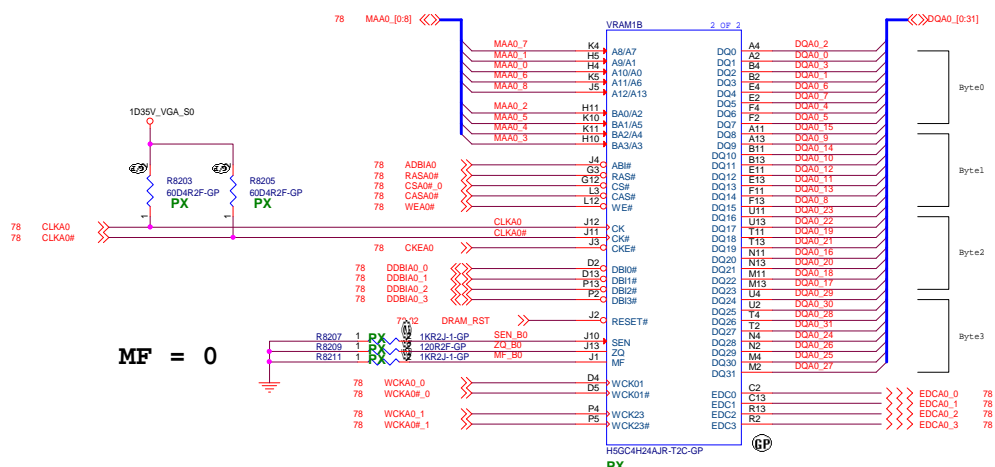
5

4

3

2

1



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GPU VRAM3,4 (2/4)

Document Number: **Unicorn_LV530_KBL_MB#A**

Rev: **1.0**

Date: Friday, December 15, 2017 Sheet: **82** of **105**

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BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size

A

Document Number

Unicorn LV530 KBL MB1A

Rev

Date: Friday, December 15, 2017

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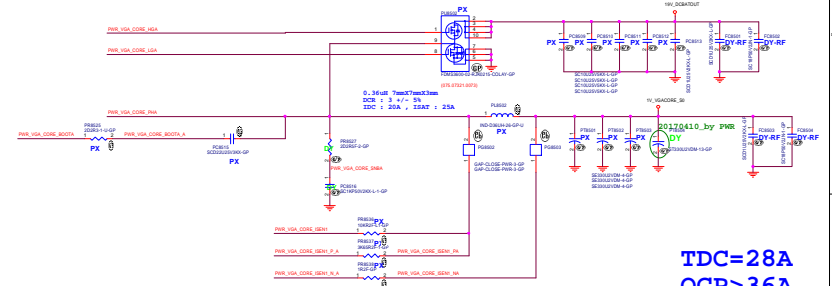
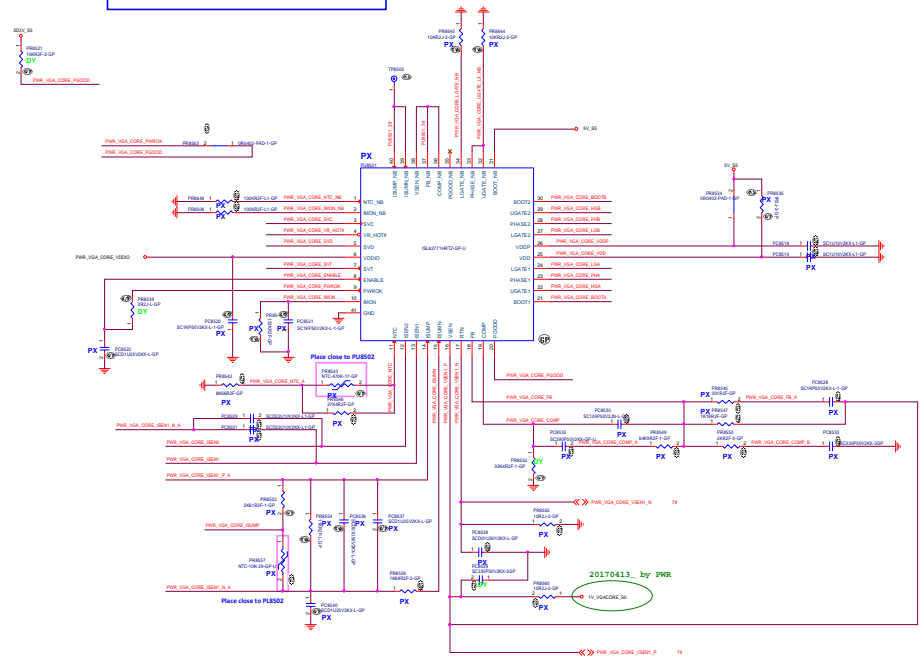
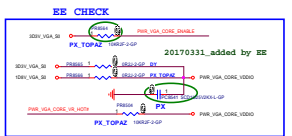
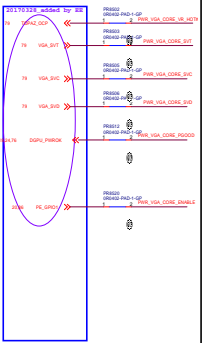
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BOM1

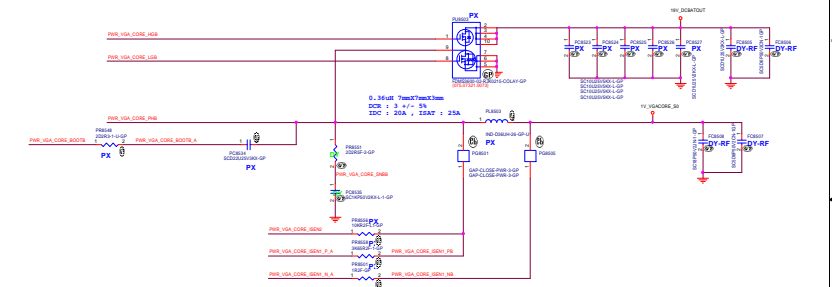
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU VRAM7,8 (4/4)			
Size	Document Number		Rev
A	Unicorn LV530 KBL MB19A		1A
Date:	Friday, December 15, 2017	Sheet 84 of	105

OFFPAGE

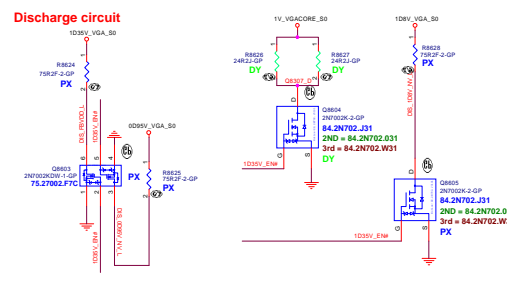
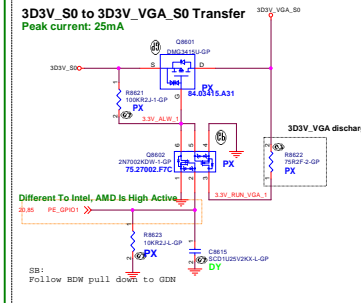
EE CHECK



TDC=28A
OCP>36A



20151106 need Add MOS to Control 1D35V_EN# IN SB version

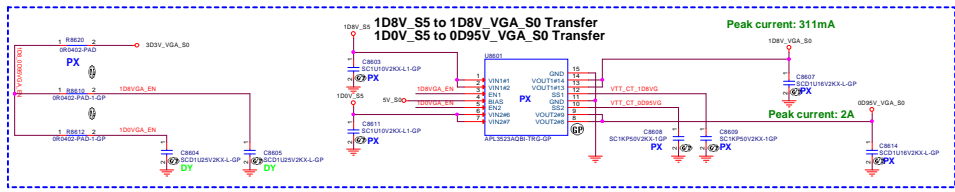


GPU PWR Sequencing
3D3V_VGAS0
=> 0D95V_VGA_S0/1D8V_VGA_S0
=> 1D35V_VGA_S0
=> VGA_CORE

All the ASIC supplies must reach their respective nominal voltages withing **20ms** of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.

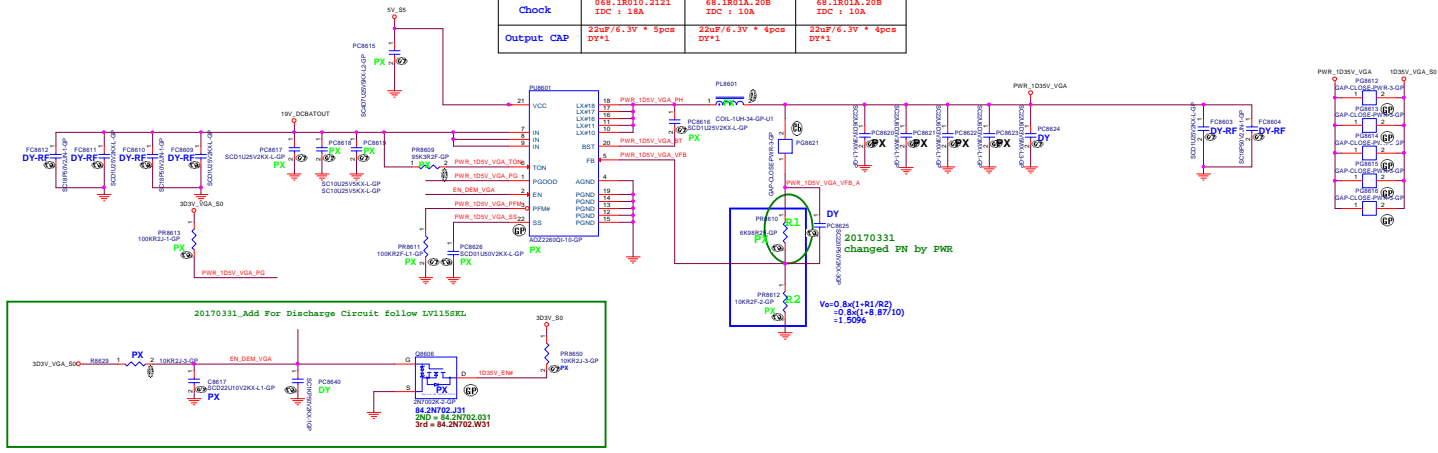
It is recommended that the 3.3V rail ramp up first.

It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.



EE need to confirm 20170208
EE confirm 20170413

IC	AOZ2262 (10A)	AOZ2261 (8A)	AOZ2260 (6A)
COM	668.1801A.2121	66.1801A.208	66.1801A.208
Check	IDC : 1.8A	IDC : 10A	IDC : 10A
Output CAP	22uF/6.3V + 5pcs DY*1	22uF/6.3V + 4pcs DY*1	22uF/6.3V + 4pcs DY*1



5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>

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Title

(RESERVED)

Size
A4

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Unicorn LV530 KBL MB GA

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5

4

3

2

1

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BOM1

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Title

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Size
A4

Document Number

Unicorn LV530 KBL MB GA

Rev

Date: Friday, December 15, 2017

Sheet 88 of 105

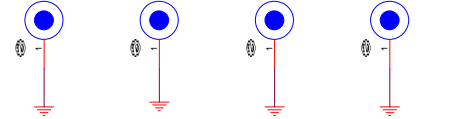
EMI Clip

EMI Clip

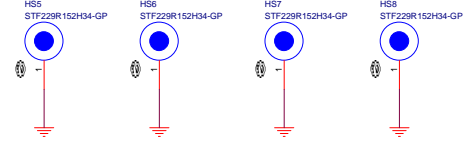
34.4GD01.101 will change to 434.0DB04.0001 by ME request
Waiting for symbol

34.4WZ01.001 34.4WZ01.001 34.4WZ01.001 34.4WZ01.001

HS1 STF237R128H42-7-GP HS2 STF237R128H42-7-GP HS3 STF237R128H42-7-GP HS4 STF237R128H42-7-GP

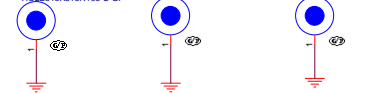


434.0DB04.0001434.0DB04.0001 434.0DB04.0001434.0DB04.0001



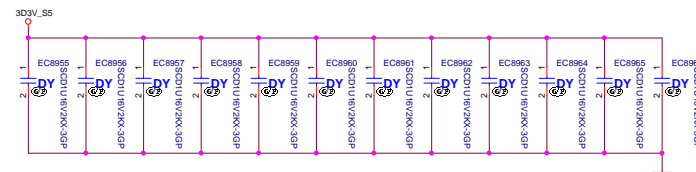
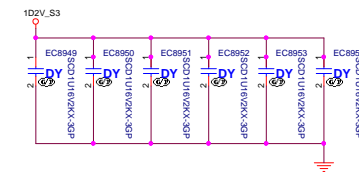
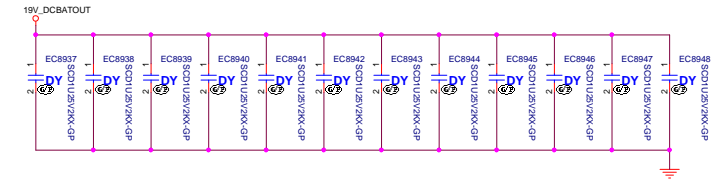
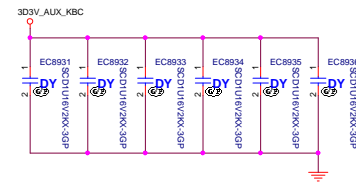
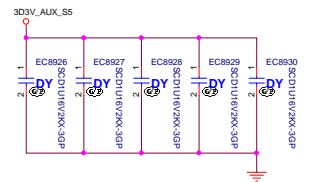
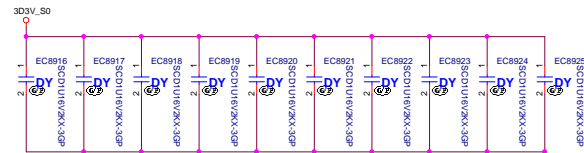
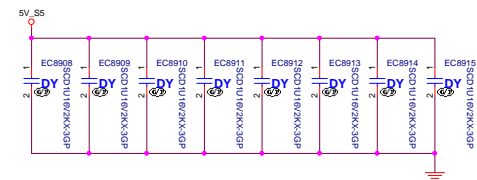
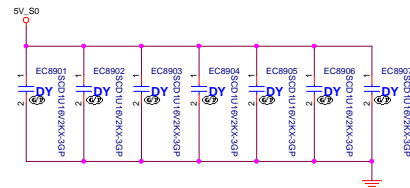
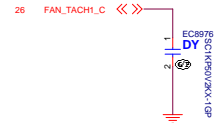
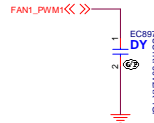
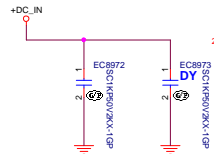
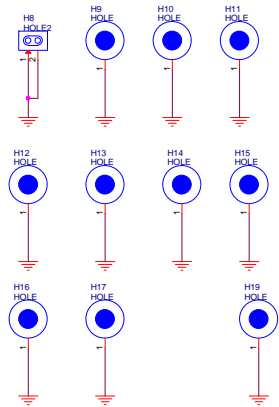
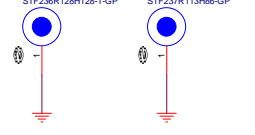
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H5 HOLE15X316R103-S-GP H6 HOLE237R103-GP H7 HOLE256R123-1-GP



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HS9 STF236R128H128-1-GP HS10 STF237R113H86-GP



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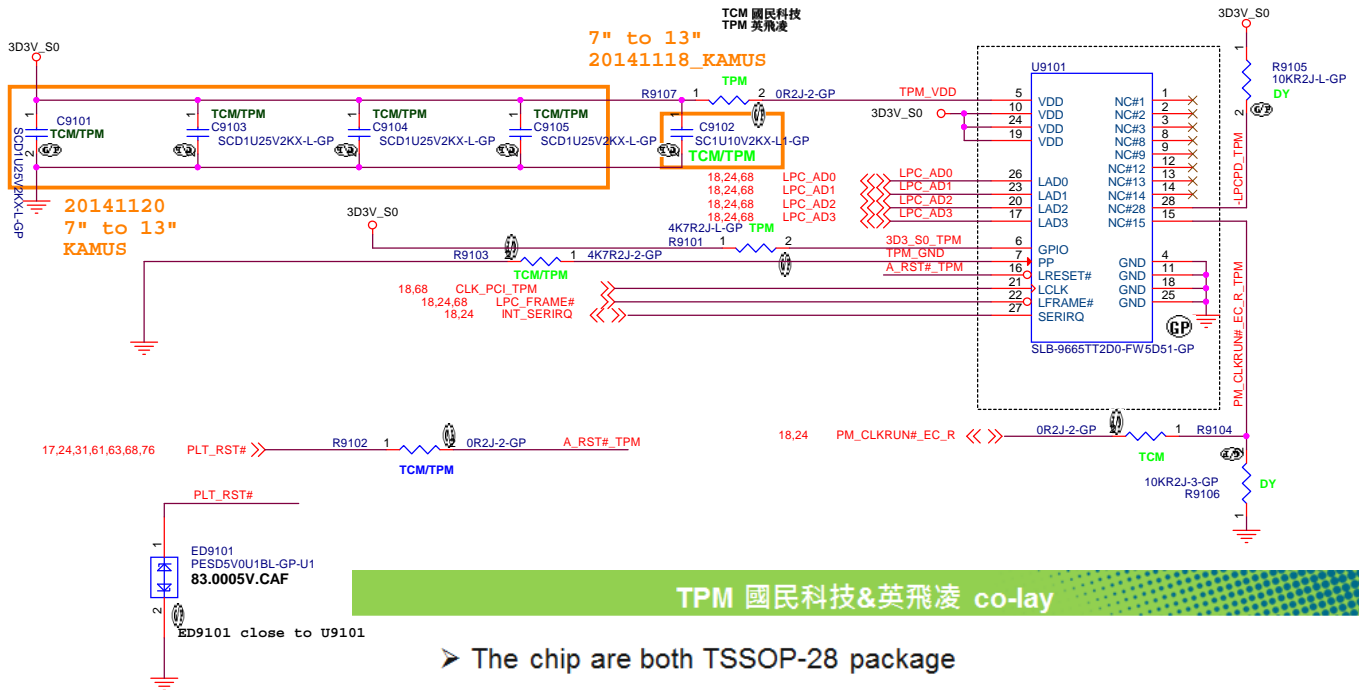
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TPM 國民科技&英飛凌 co-lay

➤ The chip are both TSSOP-28 package

Pin define	國民	英飛凌	Remark	Pin define	國民	英飛凌	Remark
1	NC	NC		15	CLKRUN#	NC	0ohm
2	NC	NC		16	LRESET#	LRESET#	
3	NC	NC		17	LAD3	LAD3	
4	GND	GND		18	GND	GND	
5	NC	VDD	0ohm	19	VDD	VDD	
6	NC	GPIO	0ohm	20	LAD2	LAD2	
7	NC	PP	0ohm	21	LCLK	LCLK	33ohm for 國民
8	NC	NC		22	LFRAME#	LFRAME#	
9	NC	NC		23	LAD1	LAD1	
10	VDD	VDD		24	VDD	VDD	
11	GND	GND		25	GND	GND	
12	NC	NC		26	LAD0	LAD0	
13	NC	NC		27	SIRQ	SERIRQ	
14	NC	NC		28	LPCPD#	NC	0ohm

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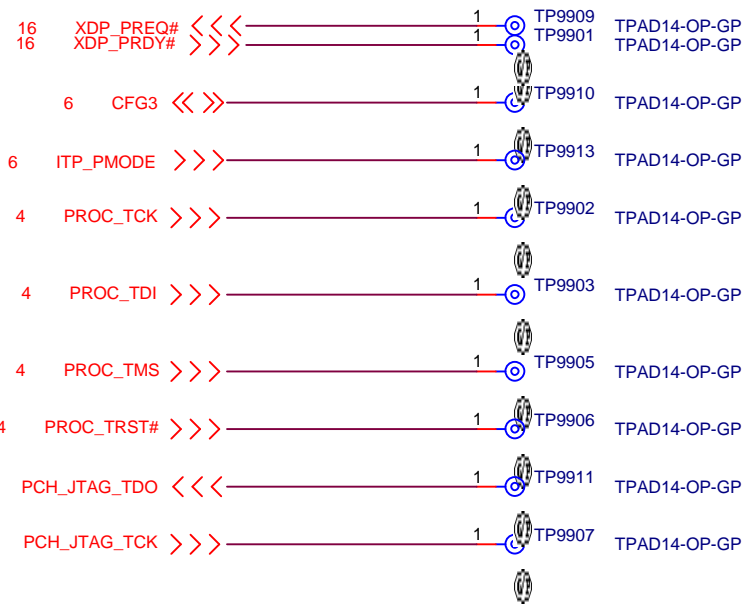
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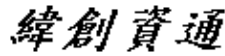
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Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)

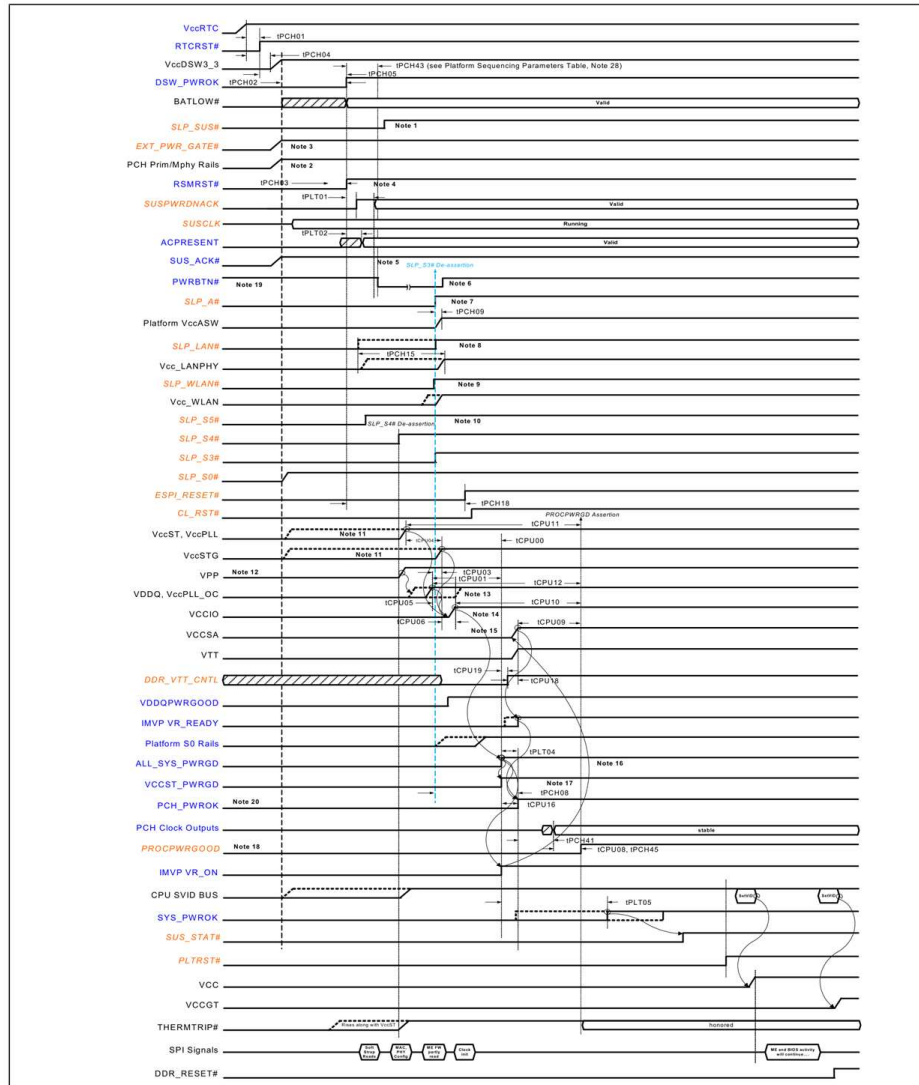


Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 2 of 2)

Notes:

1. SLP_SUS# is ignored in Non-DSx systems
2. Refer Rail-to-Rail Power Sequencing Requirement section for details on PCH prime rail-to-rail power and power down dependencies
3. EXT_PWR_GATE# has been de-featured. This pin, in native mode, will never be driven low
4. For a non-DeepSx system DSU_PWROK and RSMRST# go high at the same time (connected on board)
5. For a non-DeepSx system SUS_ACK# will rise with prime voltage rail powering the VCCPGPPA power pin, due to weak internal pull-up.
6. Minimum duration of PWRBTN# assertion = 16mS. PWRBTN# can assert before or after RSMRST#
7. On first exit from G3, SLP_A# de-asserts with SLP_S3# de-assertion
8. High for WoL=1, Low for WoL=0. SLP_LAN# may rise before, but no later than SLP_A#
9. On first exit from G3, SLP_WLAN# de-asserts with SLP_S3# de-assertion
10. Delay between SLP_S5#, SLP_S4#, and SLP_S3# exaggerated for drawing purposes. If the system EC is driving these signals in ESPI mode if the, the minimum delay between SLP_S3#, SLP_S4#, and SLP_S5# is not guaranteed
11. VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer to Chapter 42, "Platform Debug and Test Hooks" for more details. VCCSTG should only ramp up equal to or after VCCST.
12. Only required with LPDDR3 and DDR4 memory configurations
13. VDDQ must ramp after VPP on DDR4 and LPDDR3 based systems, thus VDDQ may ramp up after SLP_S3# de-assertion due to VR ramp timing and configuration
14. VCCIO, VCCSA must ramp after VccST, VccSTG, and VDDQ have completed their ramps. If VCCSTG and VCCIO supplies are merged together as a single supply, VCCSA must ramp after VccST, VccSTG/VCCIO, and VDDQ have completed their ramps
15. IMVP_VR_ON is recommended to be triggered by ALL_SYS_PWRGD in order to help minimize boot latency.
16. ALL_SYS_PWRGD is assumed to logically AND together the pwrgood signals for the major system power rails
17. VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it. It is recommended that both VCCST_PWRGD and PCH_PWROK include ALL_SYS_PWRGD in their generation. This ensures during failure events, both signals de-assert at the same time
18. PROCPWRGD is used only for power sequence debug and is not required to be connected to anything on the platform.
19. When "Power Button" is the trigger for wake or sleep event for the system
20. The Platform should ensure that PCH_PWROK does not glitch when RSMRST# is de-asserted

Additional Notes:

The state of the SLP_A# and SUSPWRDNACK signals are used by the EC to determine if PCH requires the suspend-well to stay powered.

- SUSPWRDNACK
 - Platform not supporting M3 - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted **OR** System state is S3. Else, EC has an option to do whatever it wants with the SUS Rails
 - Platform supporting M3 - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted **OR** System state is S3 **OR** SLP_A# is de-asserted **OR** it is the first 200mS after SUS Rails power has been applied. Else, EC has an option to do whatever it wants with the SUS Rails
- Primary rails and Deep Sx Rails should **never** be active while VccRTC rail is inactive.

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POWER BLOCK DIAGRAM

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SMBUS BLOCK DIAGRAM

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