

LV530 KBL/ SKL Schematics

Kabylake-U U22 / U2+3e / U42

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
 For the value, it can be read by the number before R. (R means resistor)
 For the tolerance, it can be read from the last letter.
 For the rating, we don't show on the symbol name.
 For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

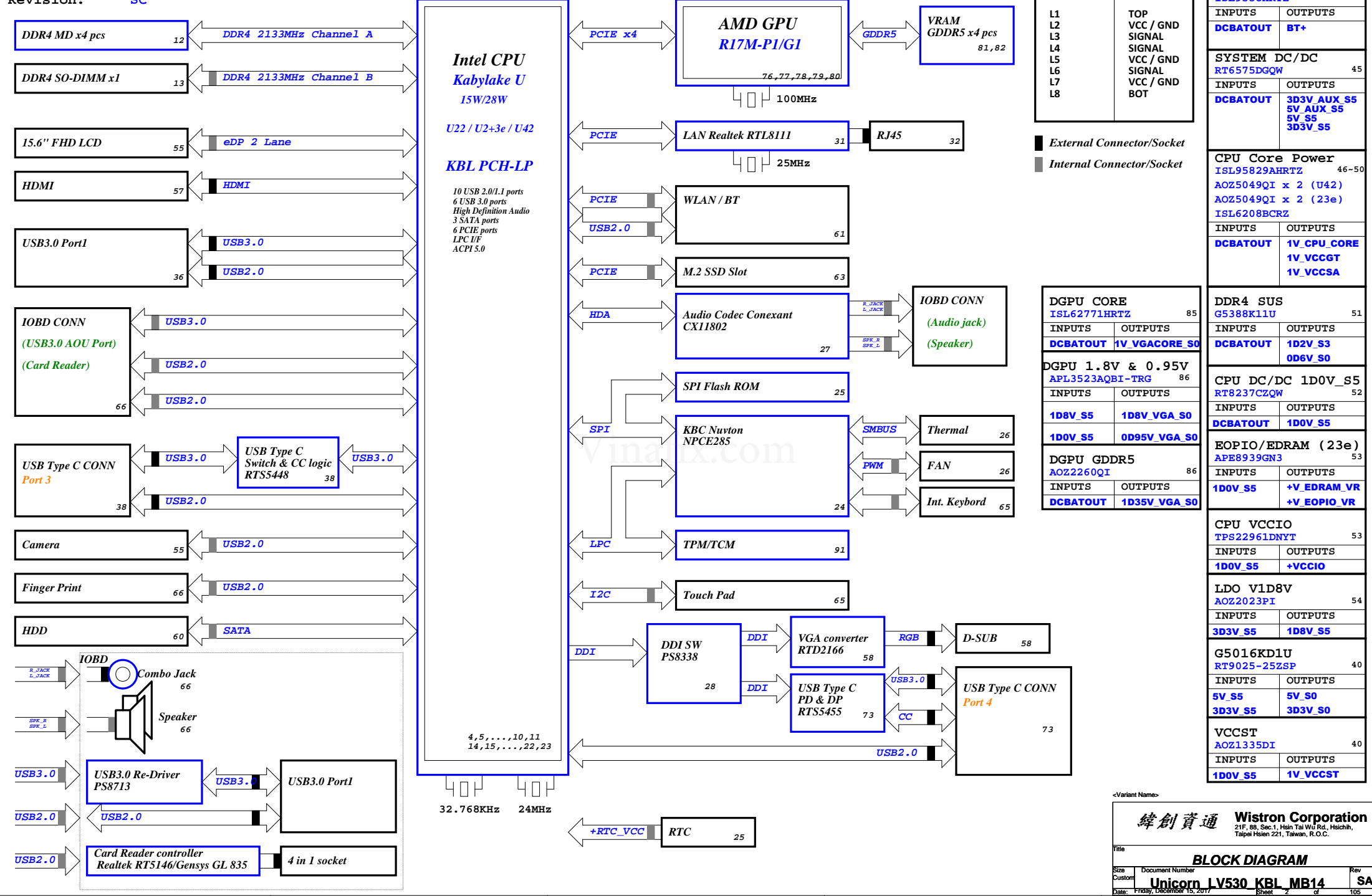
The naming rule is
 Capacitor type + value + rating + size + tolerance + material
 SCD1U10V2MX-1
 SC=> SMT Ceremic, TC=> POS cap or SP cap
 D1U => 0.1uF
 10V => the voltage rating is 10V
 2=> 0402, 3=>0603, 5=>0805
 M=>tolerance M, K, Z
 X=> X7R/X5R, Y=> Y5V
 -1 => symbol version, nonsense to EE characteristic

DY	DUMMY
DY-EMC	Follow EMC team request (SDV DY)
EMC-TVS	SDV : ASM FVT&SIT : By SKU (SKU1 DY / SKU2 ASM)
EMC-TEST	For EMC team SDV test (SDV : ASM)
23e	U2+3e only
U42	U42 only
NON-U42	U22 or U2+3e
UMA	UMA only
PX	Discrete only

<Variant Name>

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COVER PAGE	
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LV315 KBL-U Block Diagram



PCB LAYER	
L1	TOP
L2	VCC / GND
L3	SIGNAL
L4	SIGNAL
L5	VCC / GND
L6	SIGNAL
L7	VCC / GND
L8	BOT

External Connector/Socket
 Internal Connector/Socket

CHARGER	
ISL9538HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC	
RT6575DGQW 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

CPU Core Power	
ISL95829AHRTZ 46-50	
AOZ5049QI x 2 (U42) AOZ5049QI x 2 (23e) ISL6208BCRZ	
INPUTS	OUTPUTS
DCBATOUT	1V_CPU_CORE 1V_VCCGT 1V_VCCSA

DDR4 SUS	
G5388K11U 51	
INPUTS	OUTPUTS
DCBATOUT	1D2V_S3 0D6V_S0

CPU DC/DC 1D0V_S5	
RT8237CZQW 52	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

EOPPIO/EDRAM (23e)	
APE8939GN3 53	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5 +V_EDRAM_VR +V_EOPPIO_VR

CPU VCCIO	
TPS22961DNYT 53	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5 +VCCIO

LDO V1D8V	
AOZ2023PI 54	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 1D8V_S5

G5016KD1U	
RT9025-25ZSP 40	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 3D3V_S0

VCCST	
AOZ1335DI 40	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5 1V_VCCST

DGPU CORE	
ISL62771HRTZ 85	
INPUTS	OUTPUTS
DCBATOUT	1V_VGACORE_S0

DGPU 1.8V & 0.95V	
APL3523AQBI-TRG 86	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S5 1D8V_VGA_S0 1D0V_S5 0D95V_VGA_S0

DGPU GDDR5	
AOZ2260QI 86	
INPUTS	OUTPUTS
DCBATOUT	1D35V_VGA_S0

Main Func = CPU

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<Variant Name>

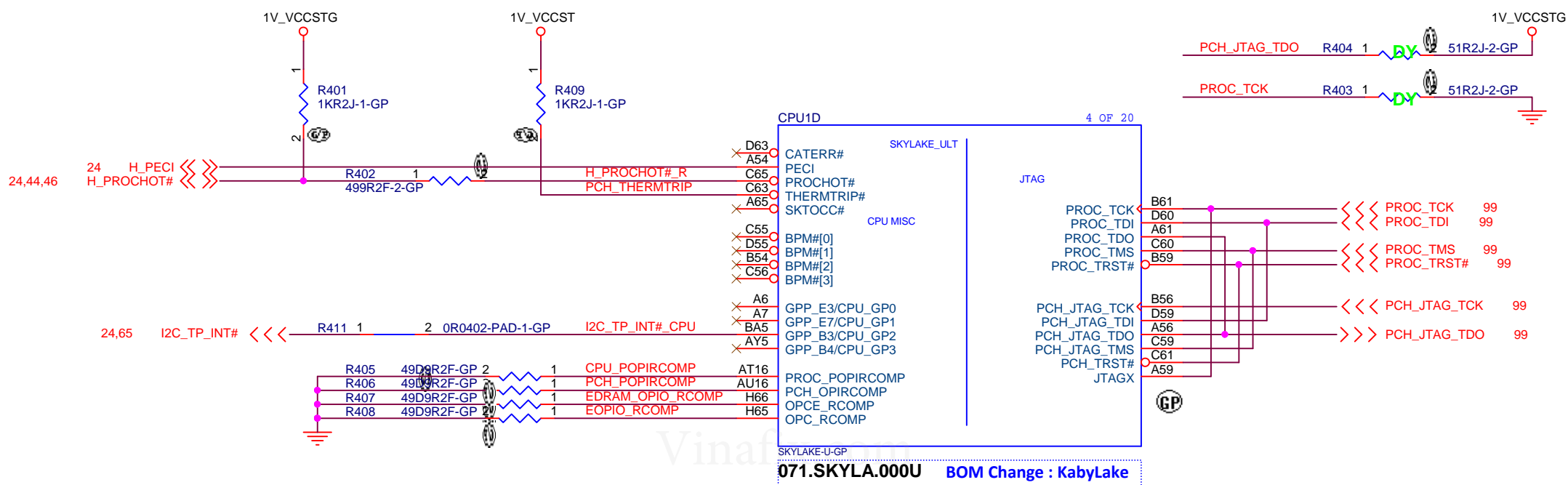
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RESERVED

Size A4	Document Number Unicorn LV530 KBL MB GA	Rev GA
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Main Func = CPU



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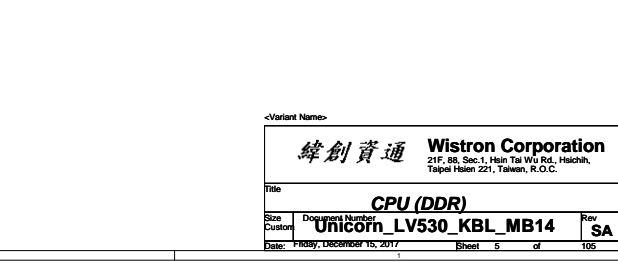
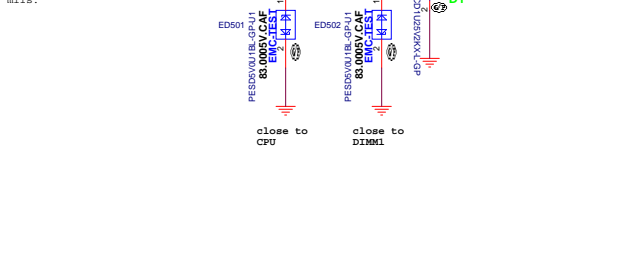
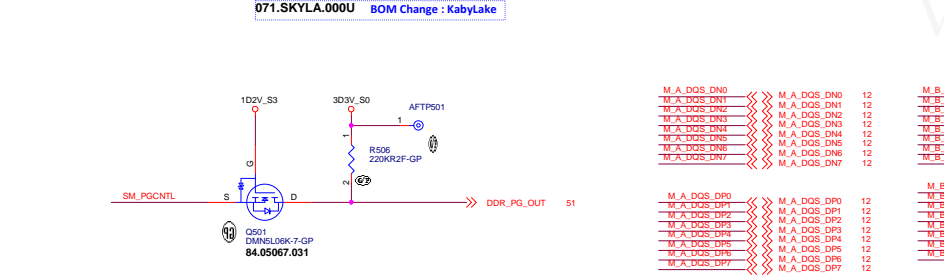
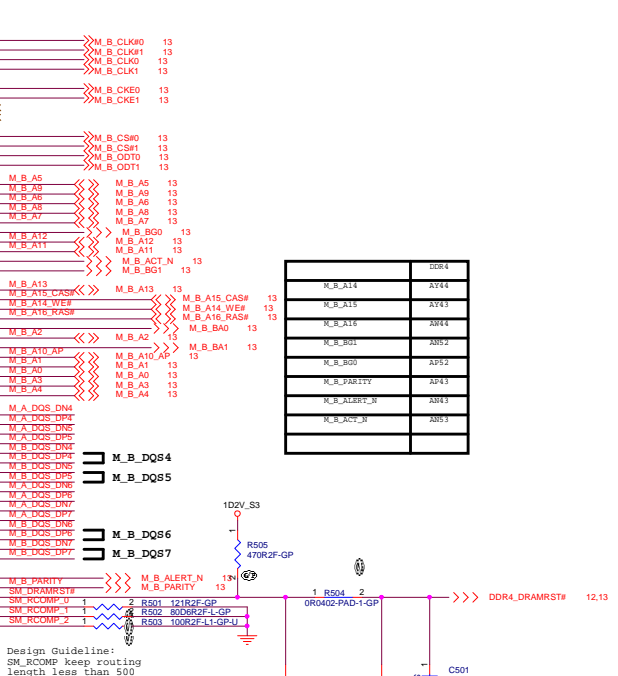
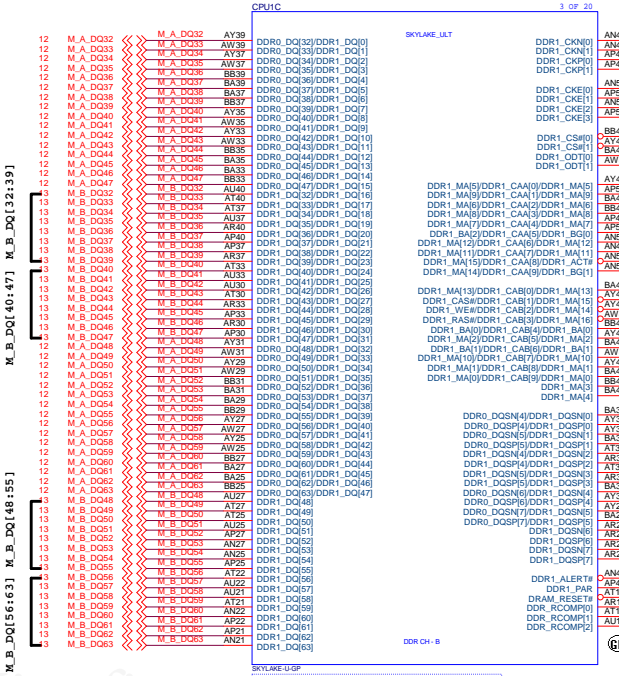
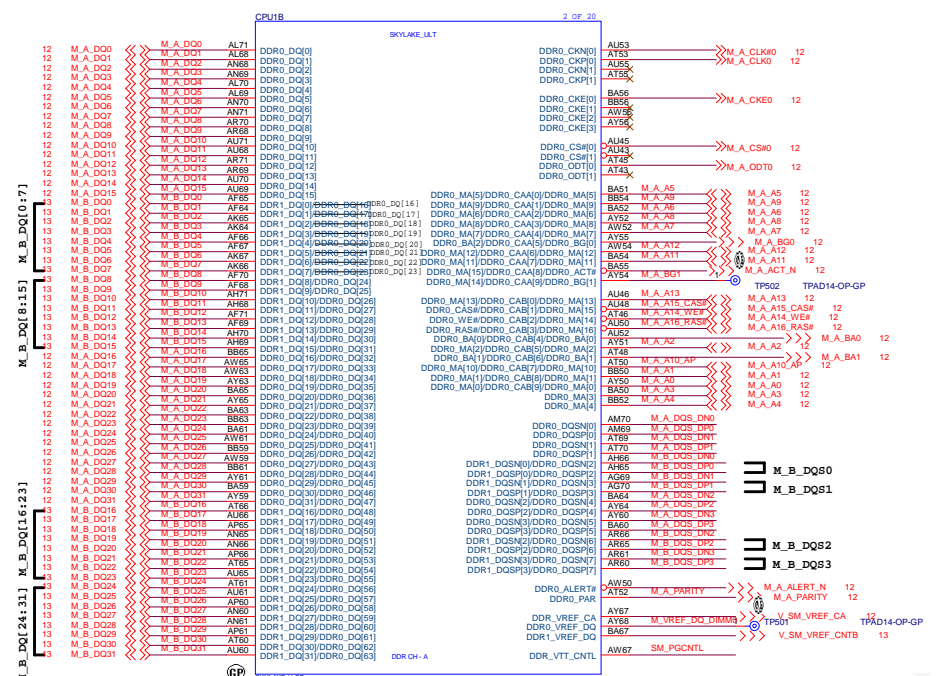
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Title: **CPU (JTAG/CPU SIDE BAND)**

Size: A4 Document Number: **Unicorn LV530_KBL_MB14** Rev: SA

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M_A_BGL, M_VREF_DQ_DIMMO Reserve Testpoint only



071.SKYLA.000 BOM Change : KabyLake

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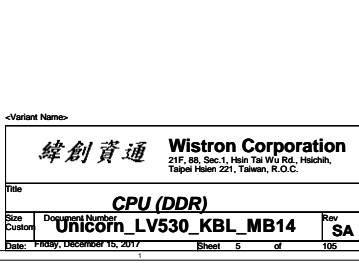
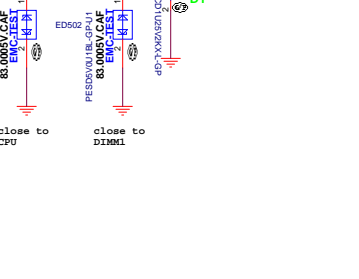
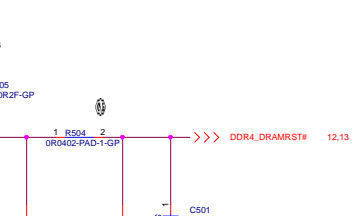
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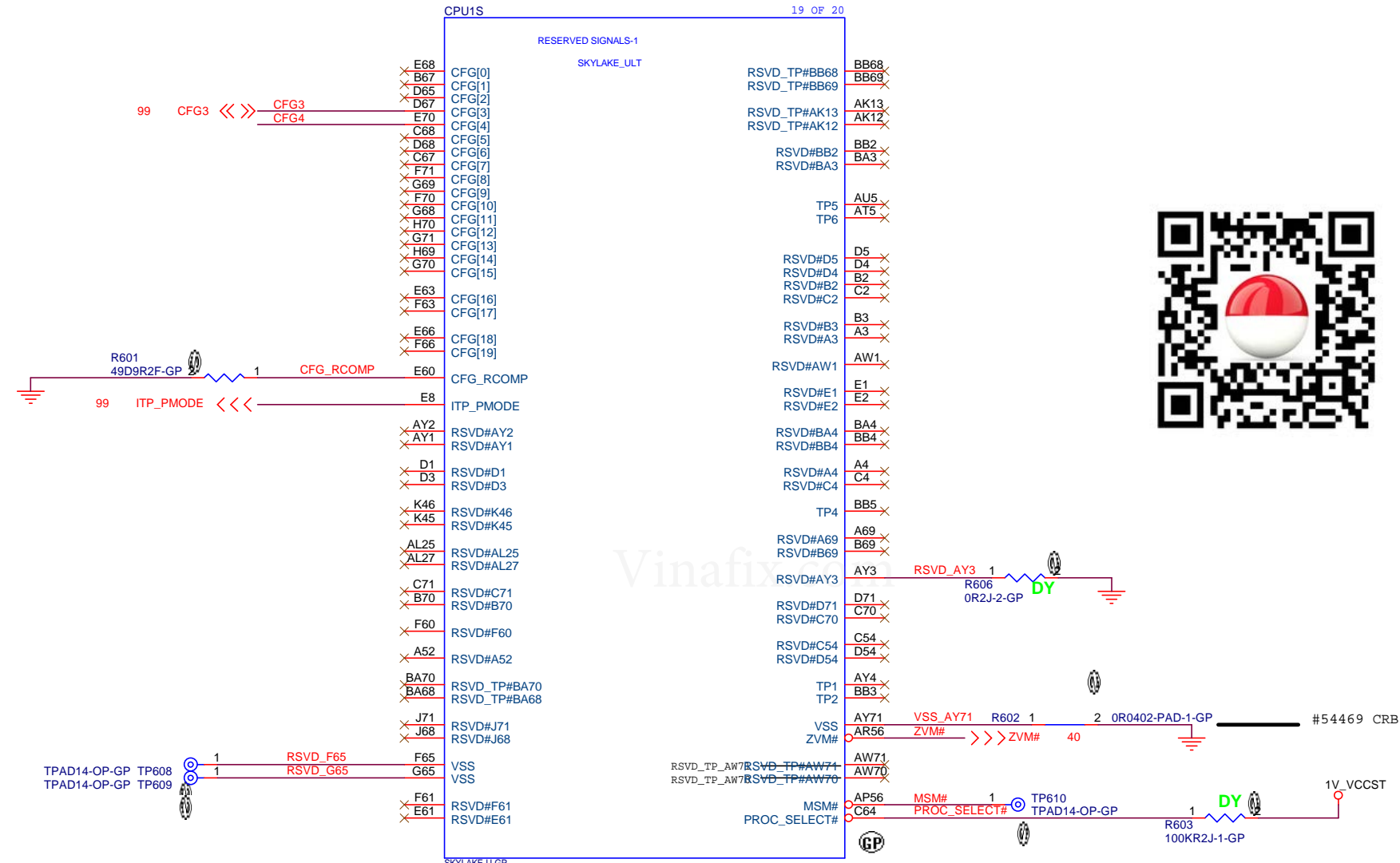
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M_B_A14	A544
M_B_A15	A543
M_B_A16	A544
M_B_B01	A552
M_B_B02	A552
M_B_PARITY_N	A543
M_B_ACTN_N	A553

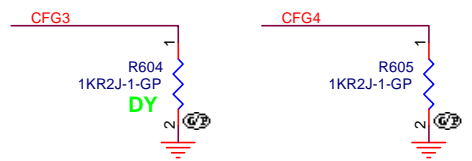


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 Title: CPU (DDR)
 Design Number: Unicorm_LV530_KBL_MB14
 Rev: SA
 Date: Friday, December 15, 2017 Sheet 5 of 105

Main Func = CPU



071.SKYLA.000U BOM Change : KabyLake

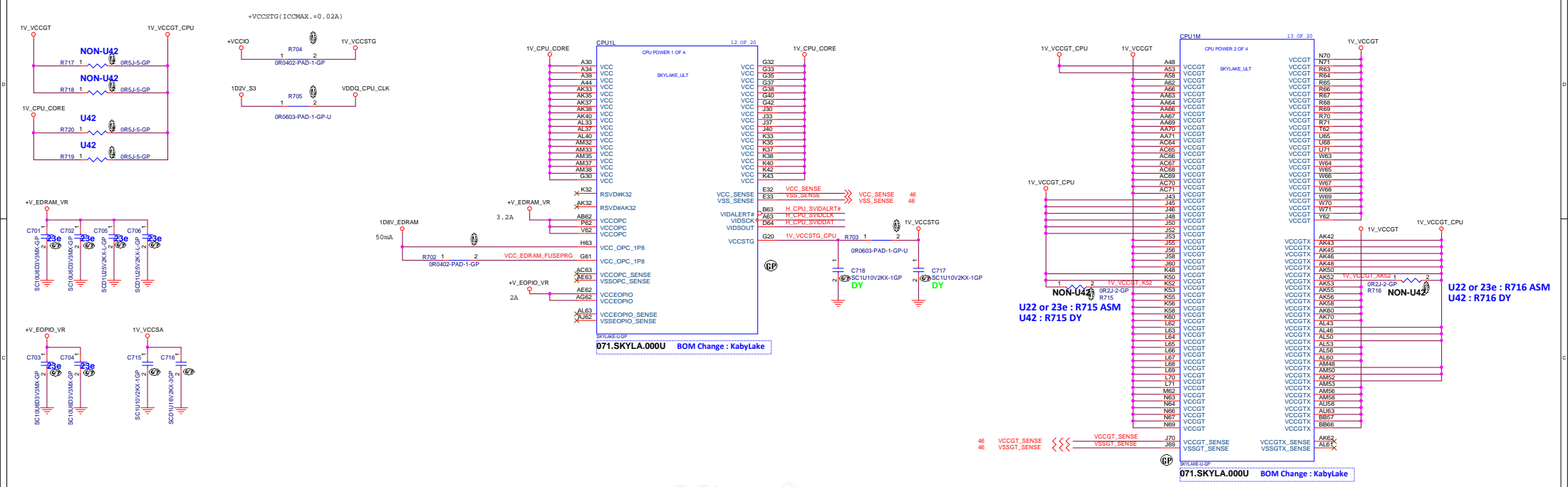


[559100]
 CFG[3]: Reserved configuration lane.
 CFG[4]: eDP enable:
 1 = Disabled.
 0 = Enabled.

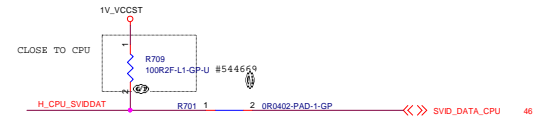
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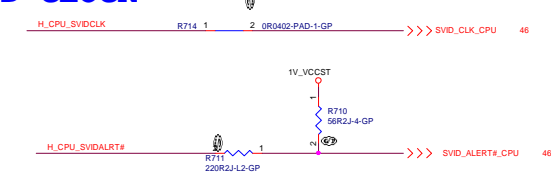
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CPU (CFG)		
Size	Document Number	Rev
Custom	Unicorn_LV530_KBL_MB14	SA
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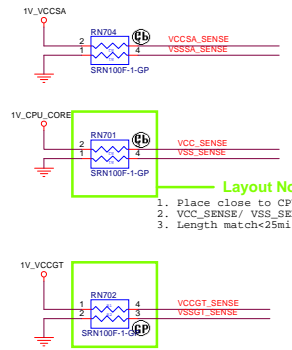
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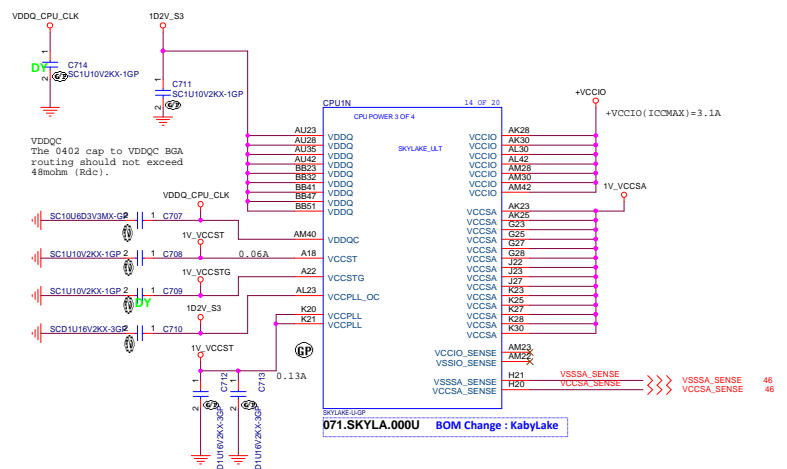
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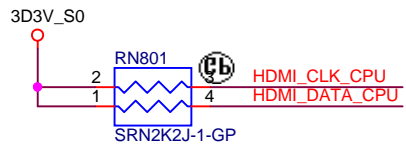
Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.



Layout Note:
1. Place close to CPU
2. VCC_SENSE / VSS_SENSE impedance=50 ohm
3. Length match<25mil



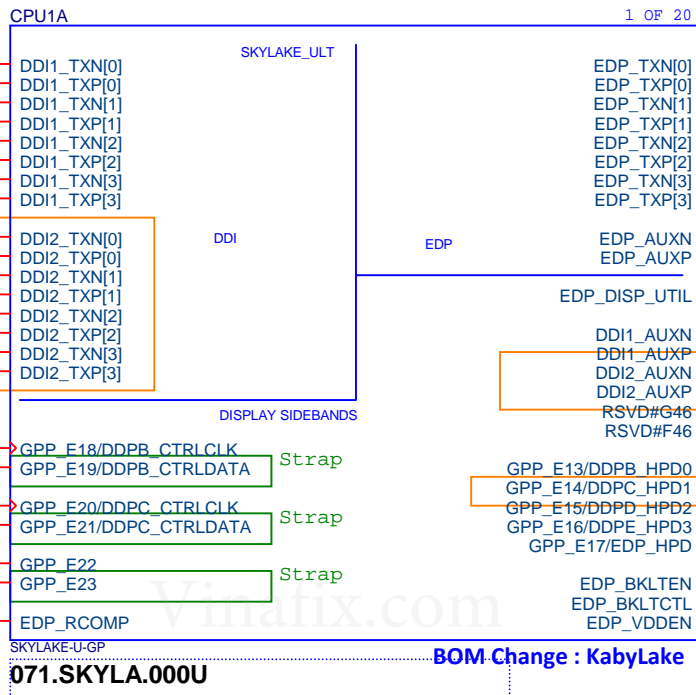
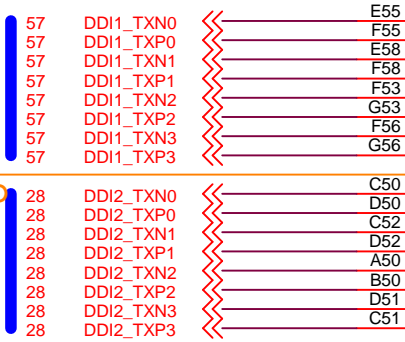
Main Func = CPU



HDMI

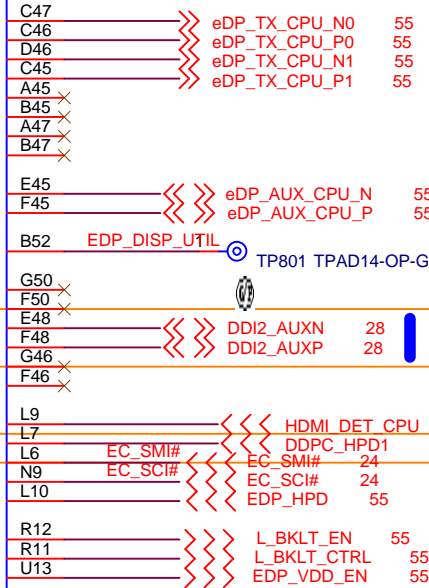
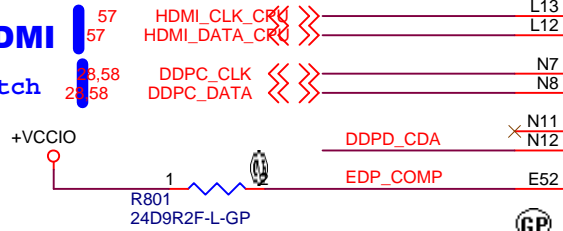
20170413
different with BOHO

DDI Switch Type C PD, DSUB



HDMI

DDI Switch



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different with BOHO

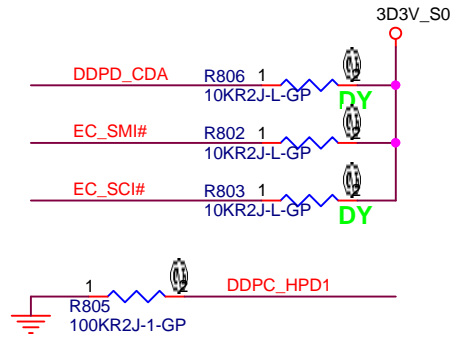
DDI Switch Type C PD, DSUB

[561280] eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	5 mils	25 mils	24.9 Ω ±1%	Max = 600 mils

[561280] DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC



<Variant Name>

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Title: **CPU (DDI/EDP)**

Size A4 Document Number: **Unicorn LV530_KBL_MB14** Rev: **SA**

Date: Friday, December 15, 2017 Sheet 8 of 105

Main Func = CPU

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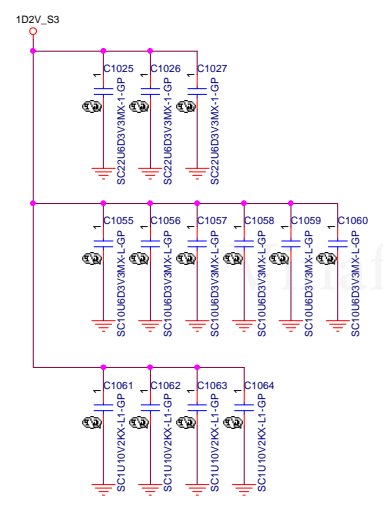
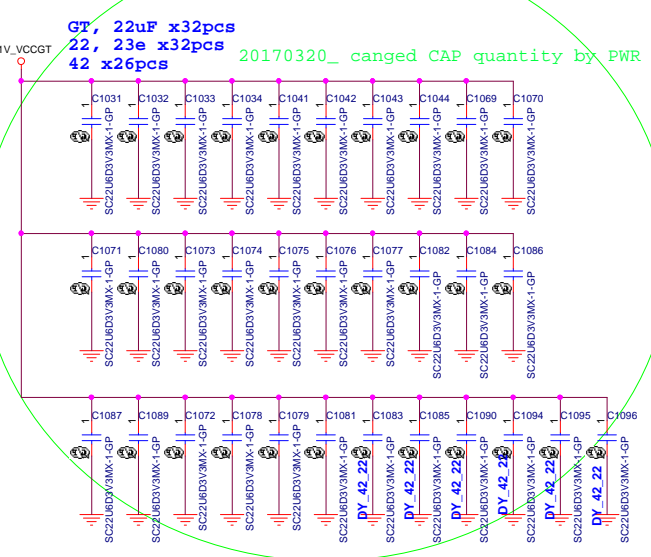
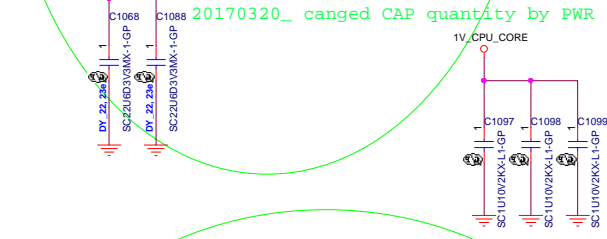
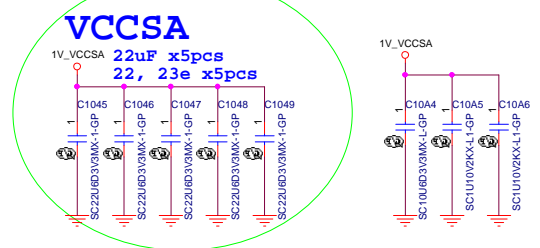
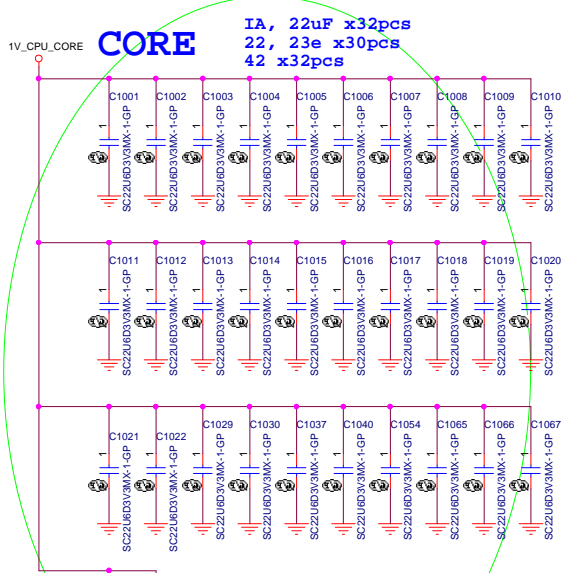
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Title **CPU (RESERVED)**

Size A4	Document Number Unicorn LV530 KBL MB GA	Rev GA
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20170320 changed CAP quantity by PWR



GT:

U-Line_22/23e

U-line 22/23e 15W/28W
 IccMax current-10ms max[A] = 64 A

22uF	PCS	Cap
Suggestion	32	330uF*1 (U22)
Suggestion	32	330uF*2 (U23e)
OPP	26	330uF*1 (U22)

U-Line_42

U-line 22/42 15W/28W
 IccMax current-10ms max[A] = 32 A

22uF	PCS	Cap
Suggestion	26	330uF*1

IA:

U-Line_22/23e

U-line 22/23e 15W/28W
 IccMax current-10ms max = 32 A

22uF	PCS	Cap
Suggestion	30	330uF*1
OPP	22	330uF*1

U-Line_42

U-line 42
 IccMax current-10ms max = 64 A

22uF	PCS	Cap
Suggestion	32	330uF*2

VCCSA:

U-Line

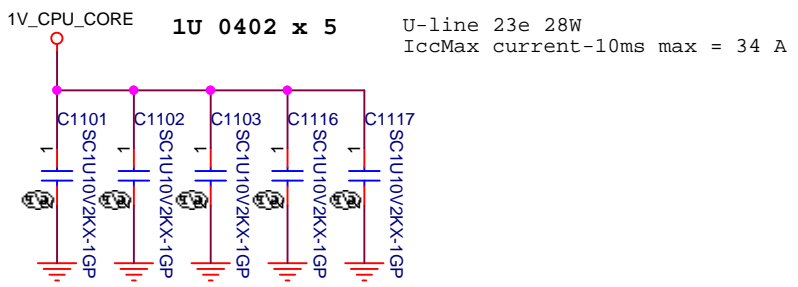
U-line 22/23e 15W/28W
 IccMax current-10ms max[A] = 5.1 A

22uF	PCS
Suggestion	5
OPP	5

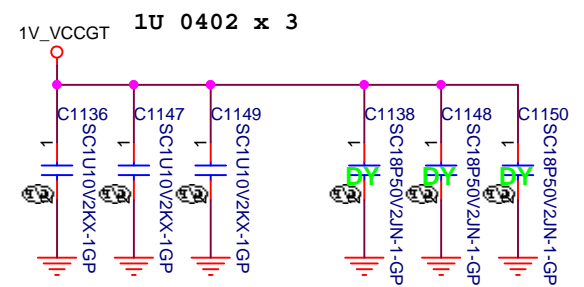
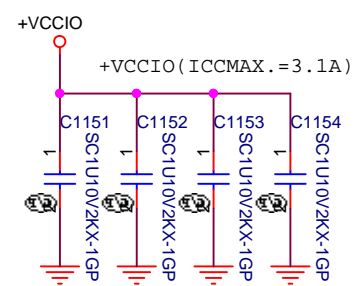
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CPU (POWER CAP1)	
Size Custom	Document Number Unicorn_LV530_KBL_MB15A
Date: Friday, December 15, 2017	Sheet 10 of 105

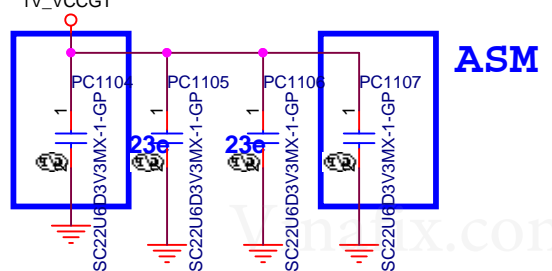
Main Func = CPU



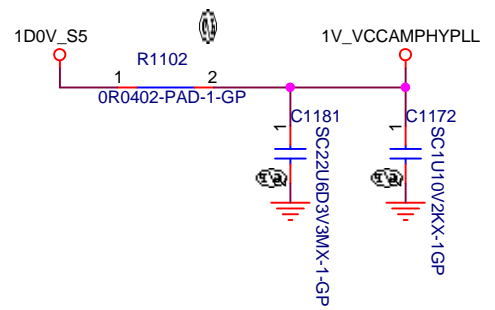
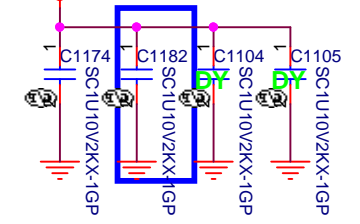
VCCIO



GTUS +V_VCCGTUS_VR can merge to +VCCGT

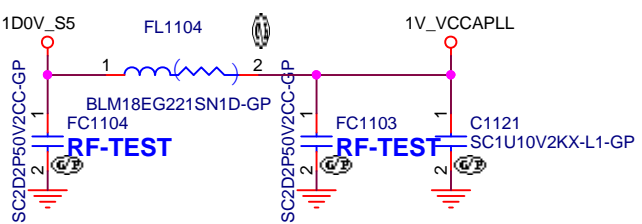
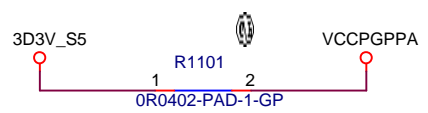
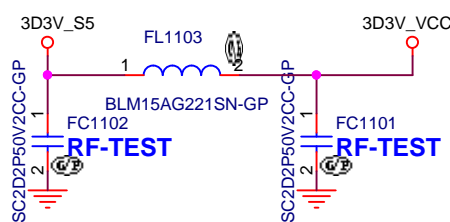


1D0V_S5 ASM 1UF



PCH DERIVED RAILS

VCCPGPPA(ICCMAX.=0.05A)



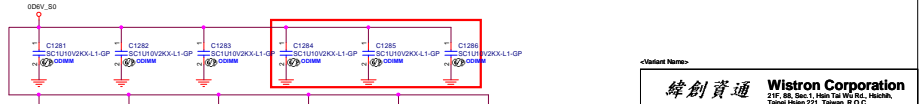
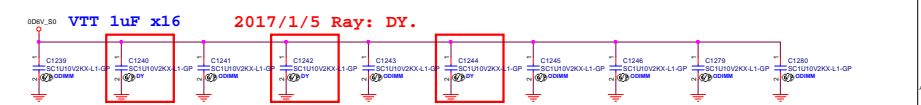
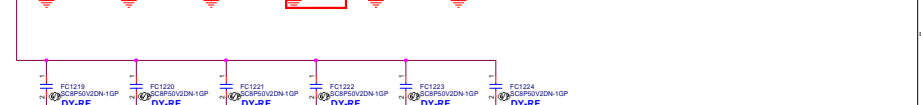
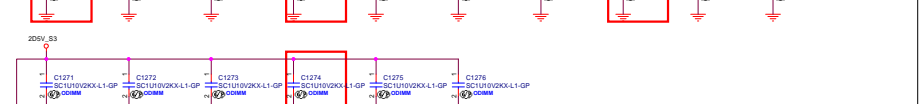
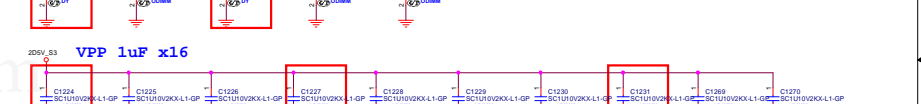
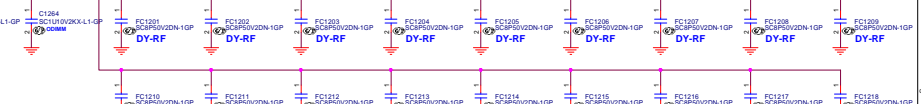
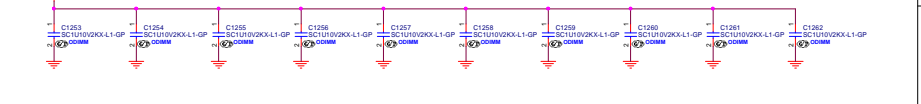
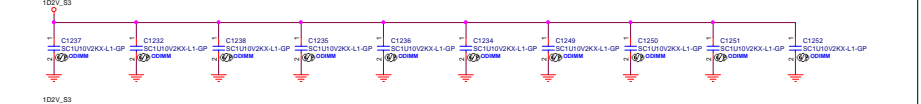
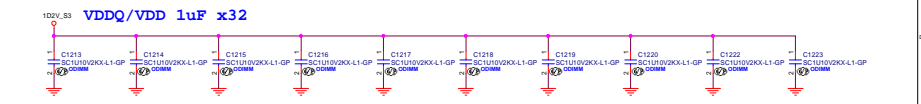
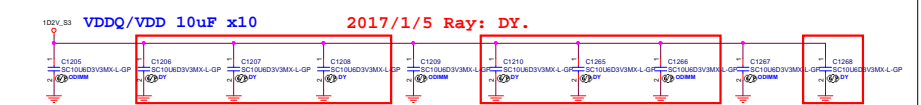
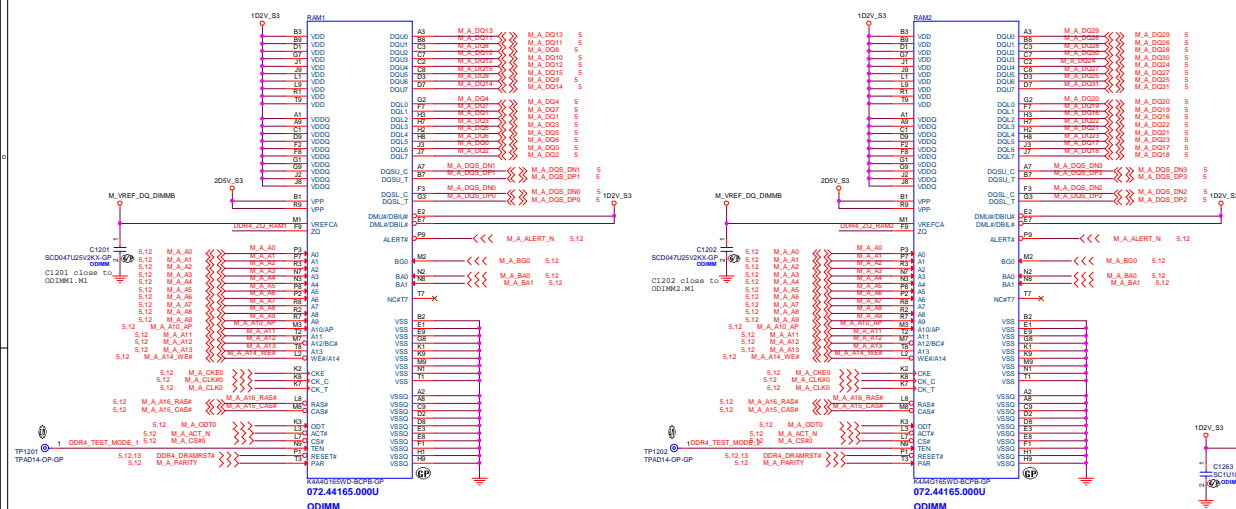
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

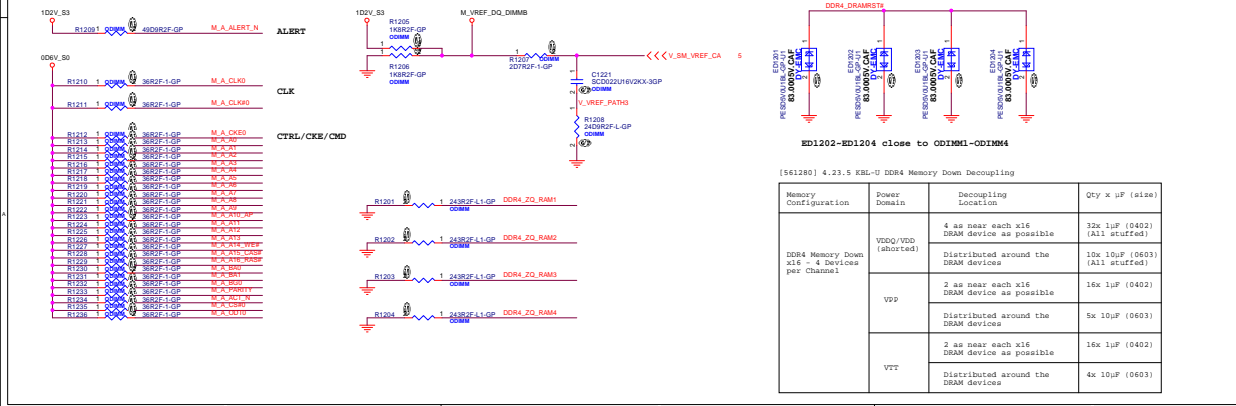
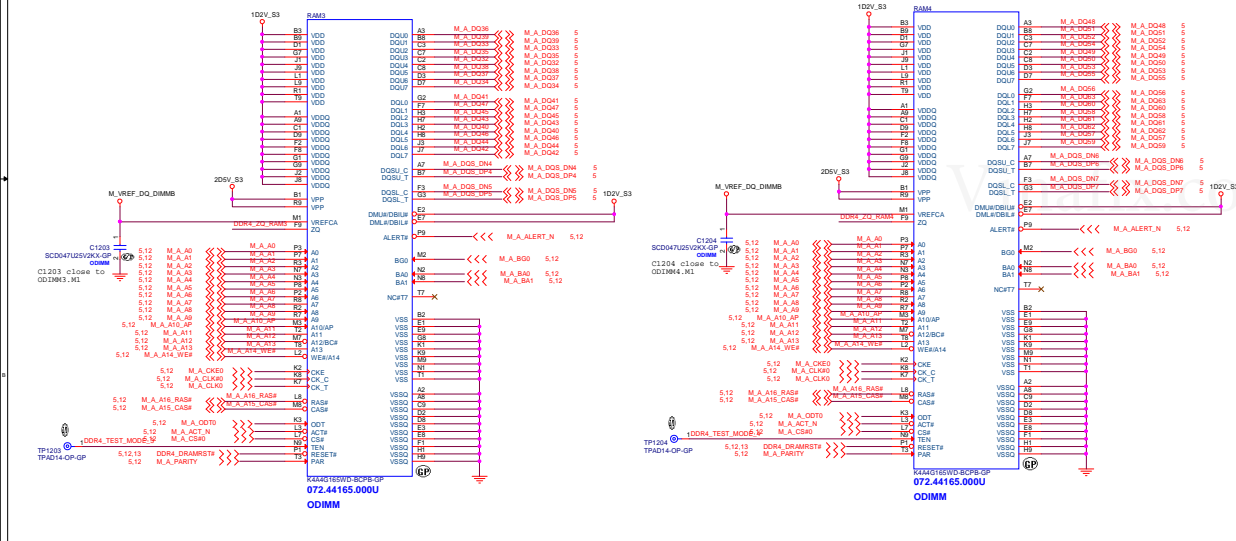
Title		
CPU (POWER CAP2)		
Size	Document Number	Rev
A4	Unicorn_LV530_KBL_MB14	SA
Date:	Friday, December 15, 2017	Sheet 11 of 105

Main Func = DDR4 On Board with Single Rank

DDR4 On Board RAM Power Decouple Cap

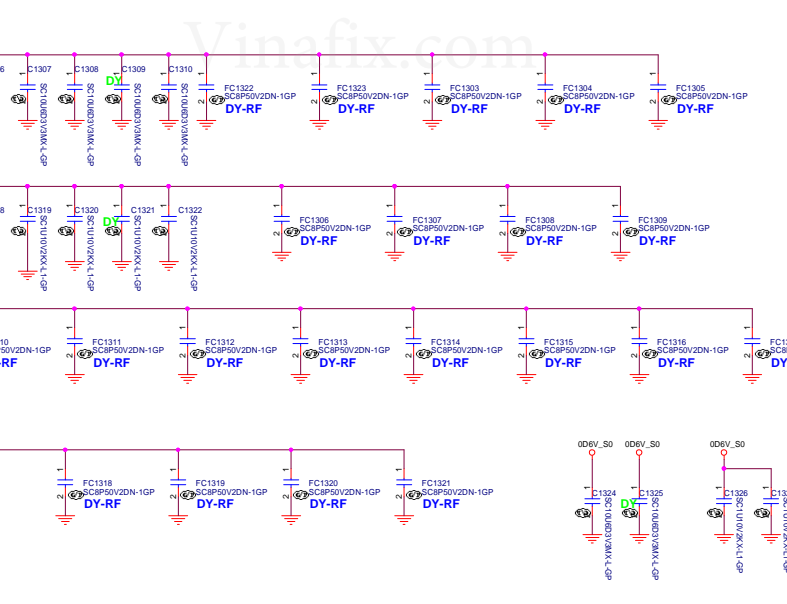
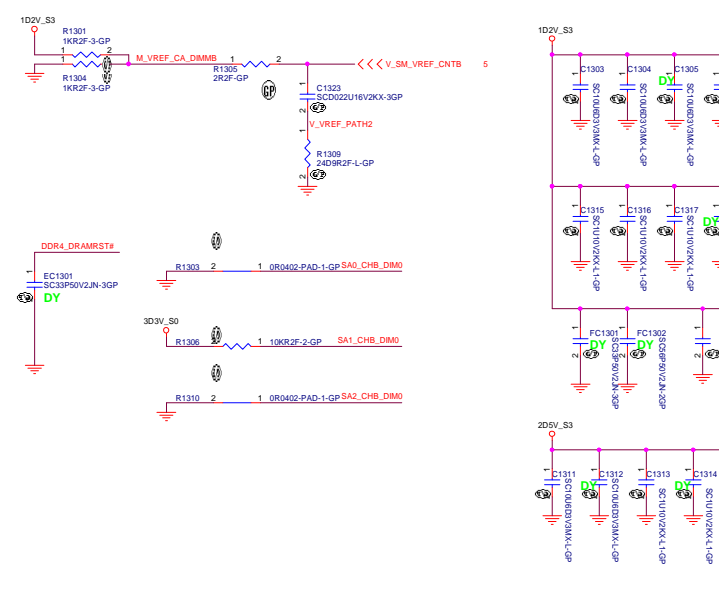
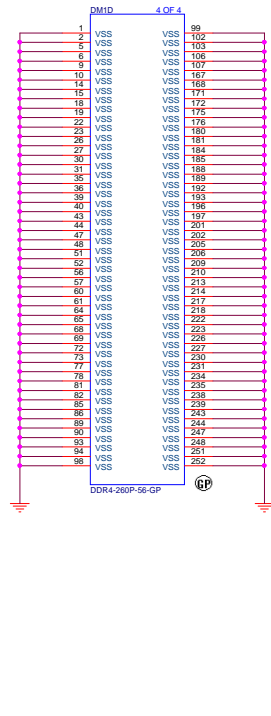
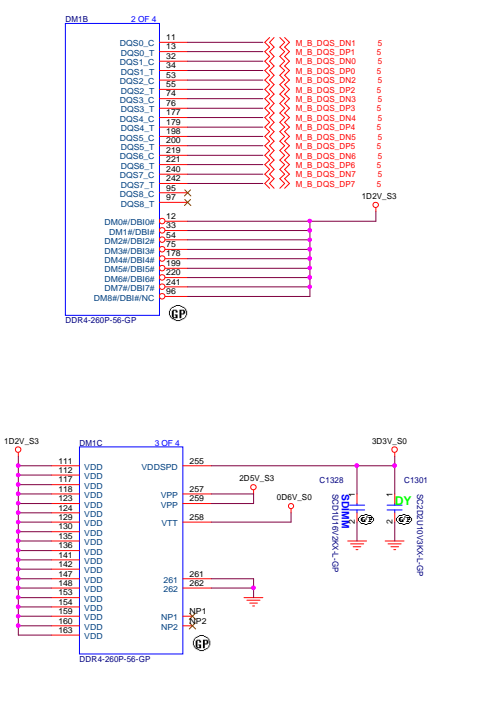
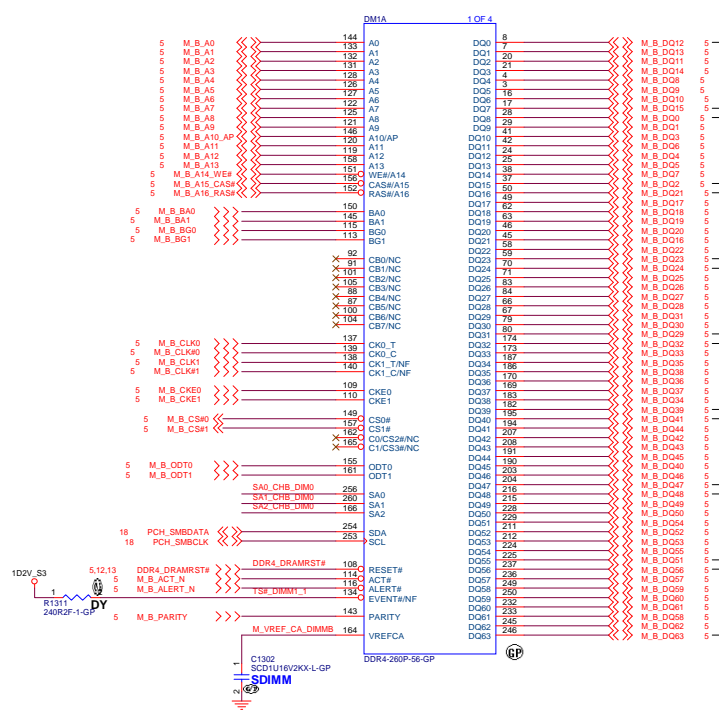


www.teknisi-indonesia.com



[61280] 4.23.5 KBL-U DDR4 Memory Down Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x uP (size)
	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1uF (0402) (All stuffed)
DDR4 Memory Down x16 - 4 Devices per Channel	VPP	Distributed around the DRAM devices	10x 10uF (0603) (All stuffed)
	VPP	2 as near each x16 DRAM device as possible	16x 1uF (0402)
	VTT	Distributed around the DRAM devices	5x 10uF (0603)
	VTT	2 as near each x16 DRAM device as possible	16x 1uF (0402)



12/09 Ray
Need to check property

[561280] 4.23.6 KBL-U DDR4 SODIMM Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)
DDR4 SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10 μ F (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1 μ F (0402)
	VTT	1 placeholder	1x 330 μ F (7343)
		Place these caps on the VTT plane close to SODIMM	1x 10 μ F (0805)
	VPP	Place these caps on the VTT plane close to SODIMM	1x 10 μ F (0402)
		Place these caps on the VTT plane close to SODIMM	4x 1 μ F (0402)
	VDDSPD	DRAM Side	2x 10 μ F (0603)
		DRAM Side	2x 1 μ F (0402)
		Place close to DIMM	1x 0.1 μ F (0402)
		Place close to DIMM	1x 2.2 μ F (0402)

(Blank)

<Variant Name>

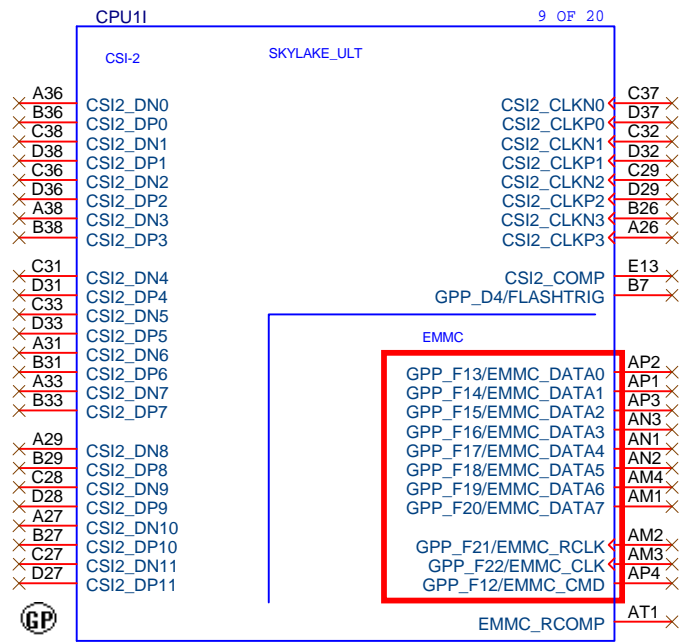
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **RESERVED**

Size A4	Document Number Unicorn LV530 KBL MB GA	Rev GA
------------	---	------------------

Date: Friday, December 15, 2017 Sheet 14 of 105

Main Func = PCH



GPP_F: VCCPGPPF = 1.8V Only



SKYLAKE-U-GP
071.SKYLA.000U BOM Change : KabyLake

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<Variant Name>

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title
CPU (CSI2/EMMC)

Size A4	Document Number Unicorn LV530 KBL MB GA	Rev
Date: Friday, December 15, 2017	Sheet 15 of 105	

[561280]
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.

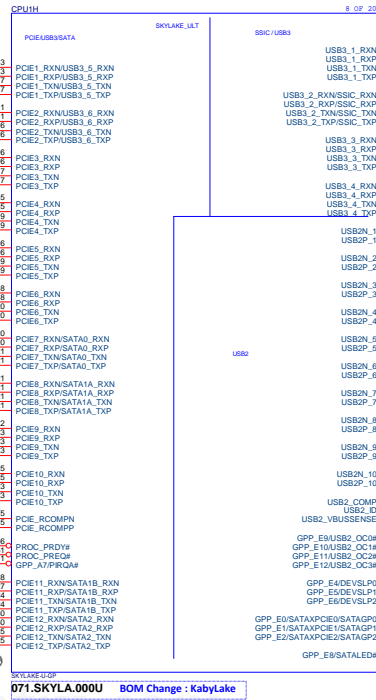
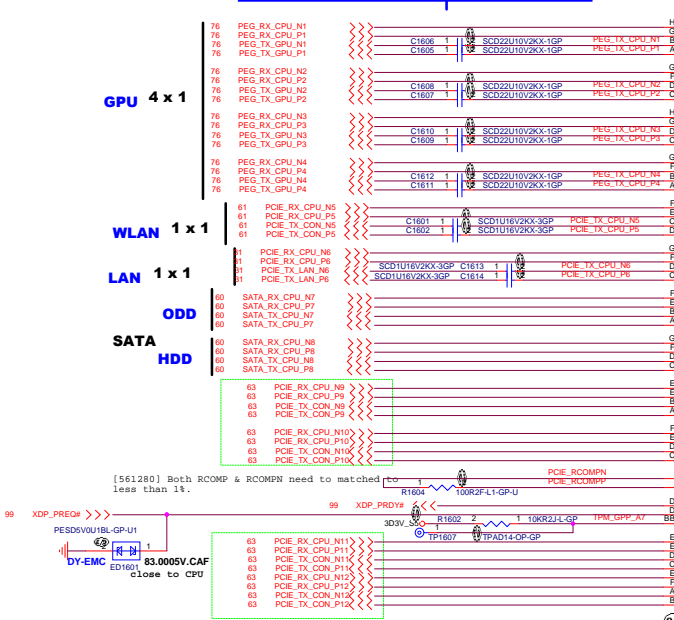
GPU 4 x 1
WLAN 1 x 1
LAN 1 x 1
SATA ODD
SATA HDD

M.2 SSD Optane
PCIe only

M.2 SSD Optane
PCIe/ SATA

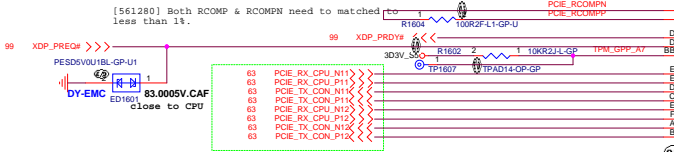
4 x 1

Share SATA



[561280] The xHCI controller provides a USB 3.0 debug port capability on all SuperSpeed ports.

- USB Port1, Type A USB3.0**
- USB Port2, Type A USB3.0 AOU**
- USB Port3, Type C USB3.0 only**
- USB Port4, Type C USB3.0, PD, DP**
- USB Port1, Type A USB2.0**
- USB Port2, Type A USB2.0 AOU**
- USB Port3, Type C USB2.0 only**
- USB Port4, Type C USB2.0, PD, DP**
- CAMERA USB Port5**
- CARD READER USB Port6**
- LCD Panel touch USB Port7**
- Bluetooth USB Port8**
- Finger Print USB Port9**



PCIe Table

Port	PCIe Device	Share BUS
1	GPU L0	
2	GPU L1	
3	GPU L2	
4	GPU L3	
5	M.2 SSD	
6	M.2 SSD	
7	M.2 SSD	SATA0
8	M.2 SSD	SATA1A
9	LAN	
10	WLAN	
11	ODD	SATA1B
12	HDD	SATA2

SATA Table

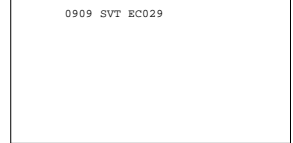
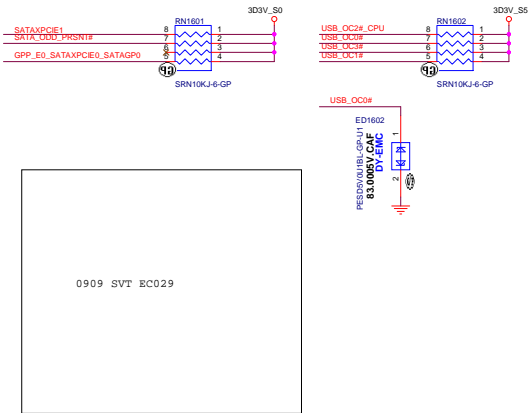
Pair	SATA Device	Share BUS
0	ODD	PCIe7
1A	HDD	PCIe8
1B	M.2 SSD	PCIe11
2	M.2 SSD	PCIe12

USB 3.0 Table

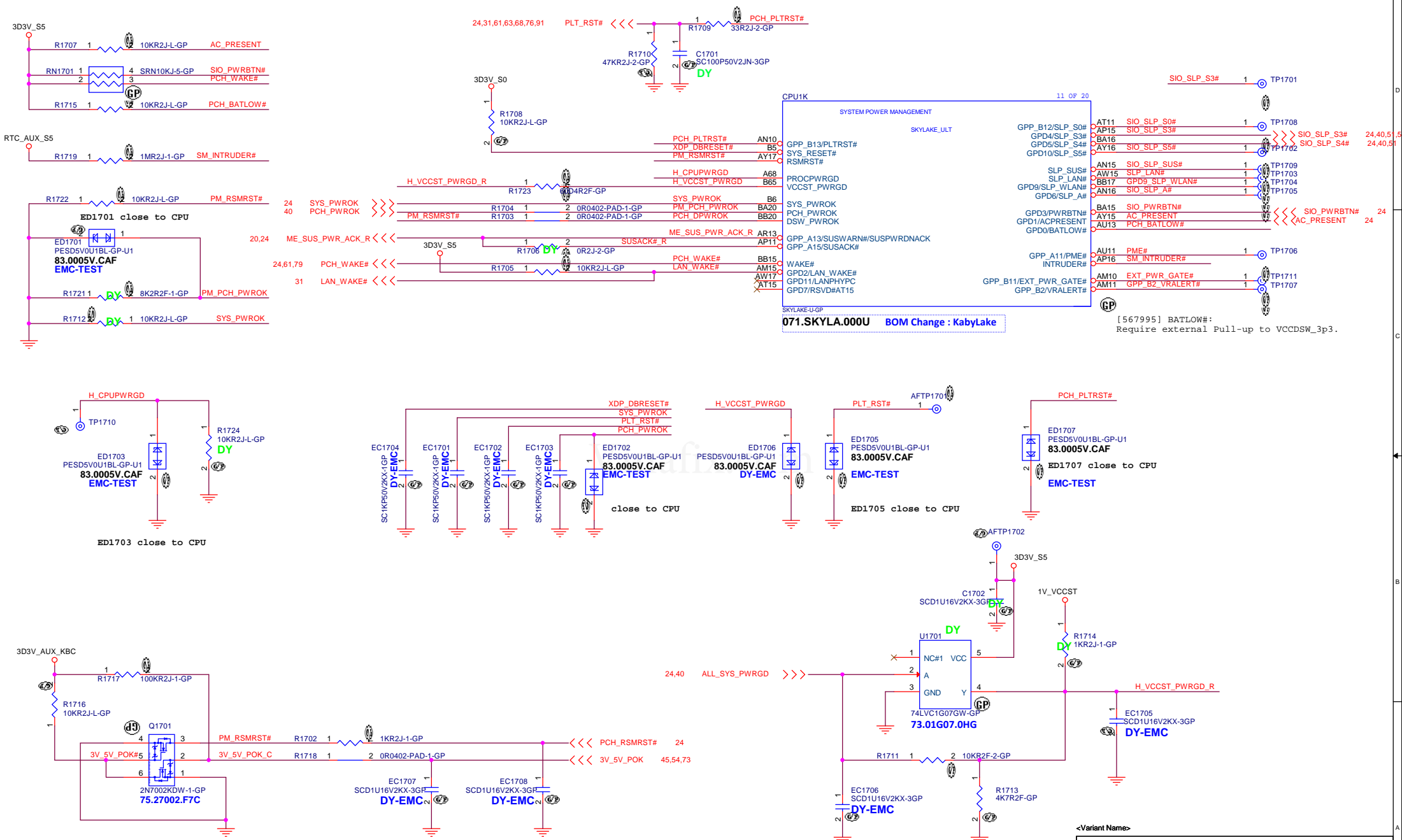
Pair	USB3.0 Device	Share BUS
1	USB3.0 port1 (Type A USB3.0)	
2	USB3.0 Port2 (Type A USB3.0_AOU)	
3	USB Port3, Type C USB3.0 only	
4	USB Port4, Type C USB3.0, PD, DP	
5	N/A	PCIe1 (GPU)
6	N/A	PCIe2 (GPU)

USB 2.0 Table

Pair	USB2.0 Device
1	USB Port1, Type A USB2.0
2	USB Port2, Type A USB2.0_AOU
3	USB Port3, Type C USB2.0 only
4	USB Port4, Type C USB2.0, PD, DP
5	CAMERA_USB Port5
6	CARD READER_USB Port6
7	LCD Panel touch_USB Port7
8	Bluetooth_USB Port8
9	Finger Print_USB Port9
10	Ultray bay_USB Port10



Main Func = PCH



<Variant Name>

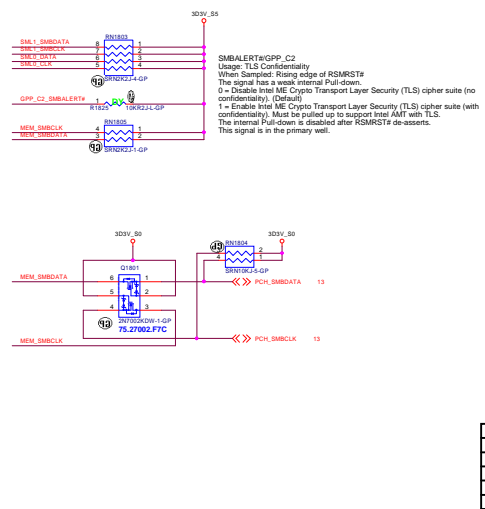
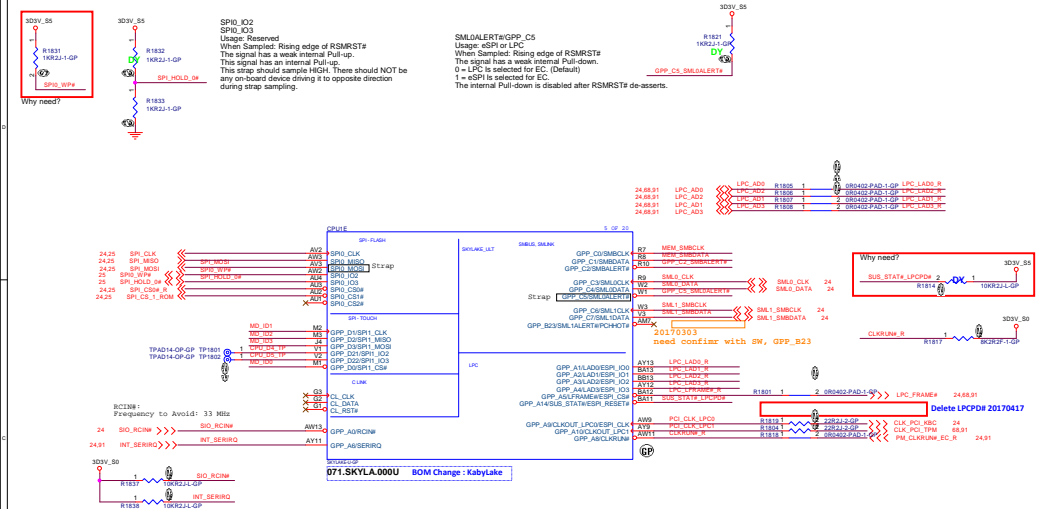
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (PM)**

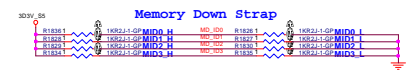
Size: A3 Document Number: **Unicorn LV530 KBL MB13A** Rev: 13A

Date: Friday, December 15, 2017 Sheet 17 of 105

Main PC = PCH

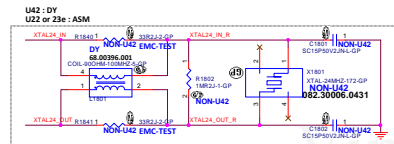
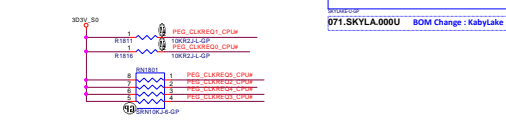
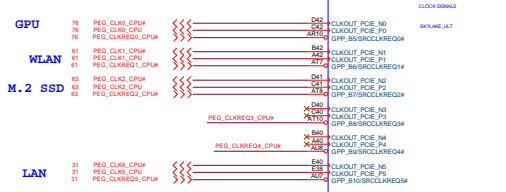


66A PIN	66B PIN	66C PIN	Location
SV20L77464	SV20L77465	SV20L77466	RAM1, RAM2, RAM3 RAM4
63 10534 L1L (1.0 MQ)	63 10234 L0L (1.0 KQ)	63 10534 L1L (1.0 MQ)	R1836
63 10234 L0L (1.0 KQ)	63 10534 L1L (1.0 MQ)	63 10234 L0L (1.0 KQ)	R1826
63 12534 1DL (1.2 MQ)	63 12534 1DL (1.2 MQ)	63 12234 1DL (1.2 KQ)	R1827
63 12234 1DL (1.2 KQ)	63 12234 1DL (1.2 KQ)	63 12234 1DL (1.2 KQ)	R1828
63 20534 1DL (2.0 MQ)	63 20534 1DL (2.0 MQ)	63 20534 1DL (2.0 MQ)	R1829
63 20234 1DL (2.0 KQ)	63 20234 1DL (2.0 KQ)	63 20234 1DL (2.0 KQ)	R1830
63 22534 1DL (2.2 MQ)	63 22534 1DL (2.2 MQ)	63 22534 1DL (2.2 MQ)	R1834
63 22234 L0L (2.2 KQ)	63 22234 L0L (2.2 KQ)	63 22234 L0L (2.2 KQ)	R1835
SAMSUNG 8GB	HYUNX 8GB	MICRON 8GB	
Memory ID : 0000	Memory ID : 0001	Memory ID : 0010	



RAM ID	MD_ID0	MD_ID1	MD_ID2	MD_ID3	MD_ID4	MD_ID5	MD_ID6	MD_ID7	MD_ID8	MD_ID9	MD_ID10	MD_ID11	MD_ID12	MD_ID13	MD_ID14	MD_ID15
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1										
2	0	0	0	1	0											
3	0	0	1	0	1											
4	0	1	0	0												
5	0	1	0	1												
6	0	1	1	0												
7	0	1	1	1												
8	1	0	0	0												
9	1	0	0	0	1											
10	1	0	0	1	0											
11	1	0	1	1												
12	1	1	0	0												
13	1	1	1	0	1											
14	1	1	1	1	0											
15	1	1	1	1	1											

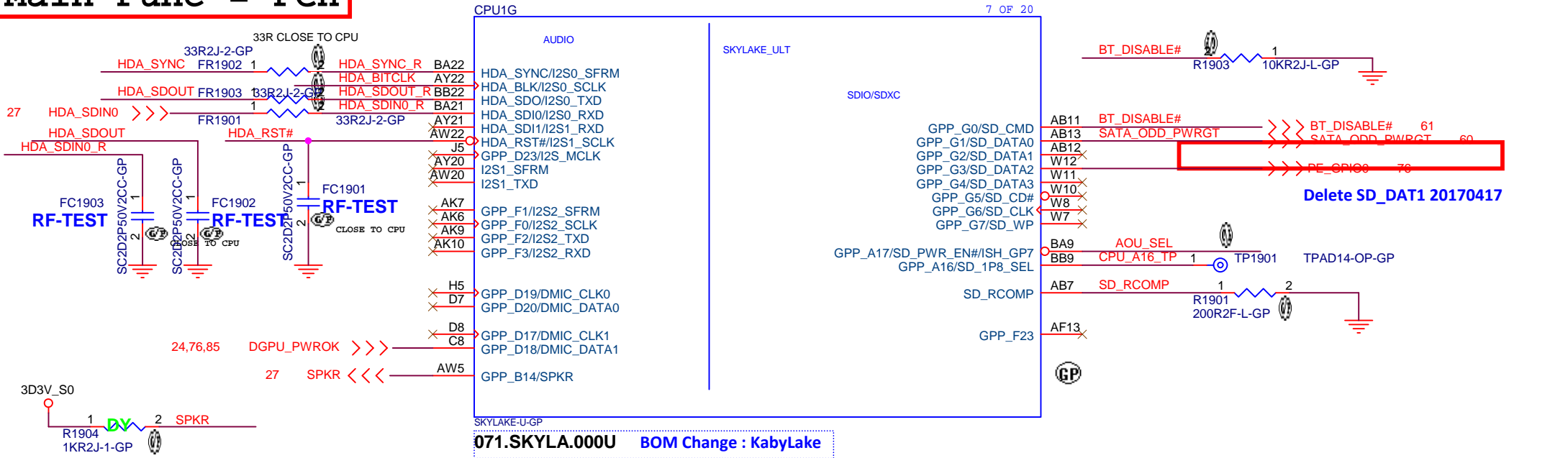
Check Clock Mapping



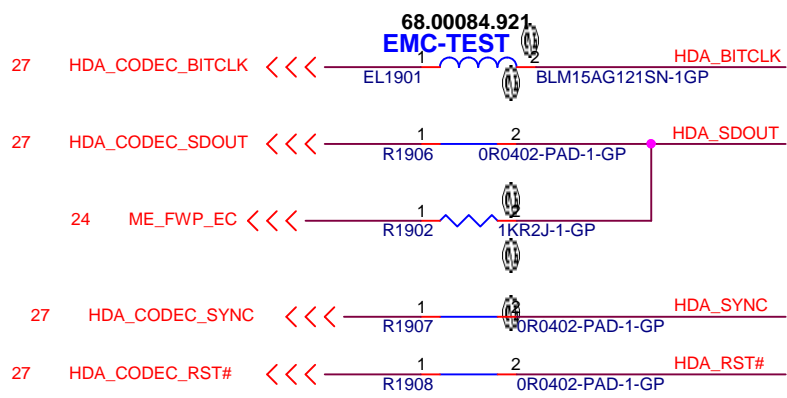
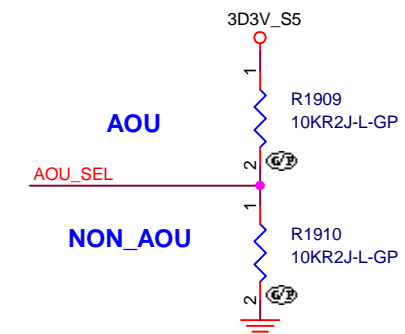
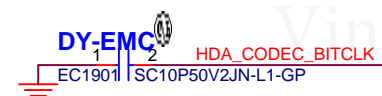
12/09 Ray
X1801, check 082.30019.0101



Main Func = PCH



SPKR/GPP_B14
 Usage: Top Swap Override
 When Sampled: Rising edge of PCH_PWROK
 The signal has a weak internal Pull-down.
 0 = Disable "Top Swap" mode. (Default)
 1 = Enable "Top Swap" mode.
 The internal Pull-down is disabled after PCH_PWROK de-asserts.
 This signal is in the primary well.

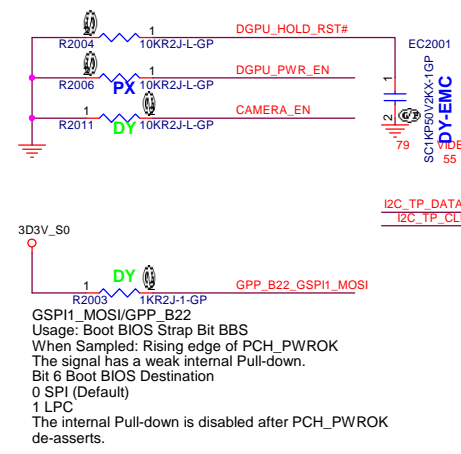


HDA_SDO /I2S_TXD0
 Usage: Flash Descriptor Security Override
 When Sampled: Rising edge of PCH_PWROK
 The signal has a weak internal Pull-down.
 0 = Enable security measures defined in the Flash Descriptor. (Default)
 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.
 The internal Pull-down is disabled after PCH_PWROK de-asserts.

<Variant Name>

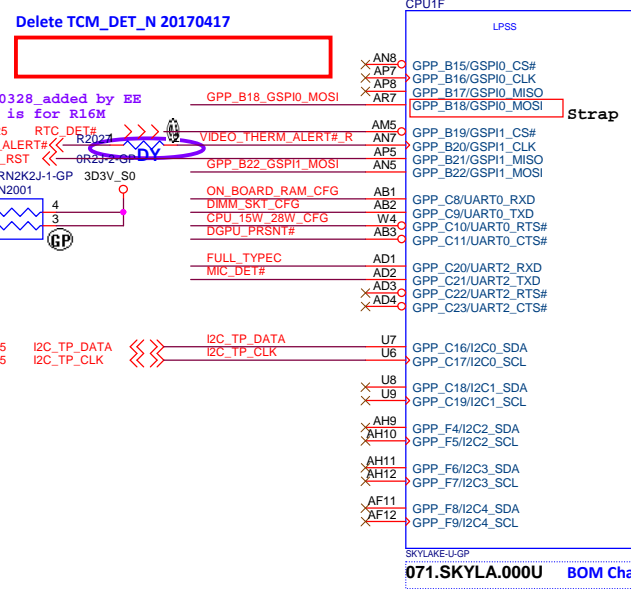
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
CPU (HDA/SDIO/SDXC)			
Size A4	Document Number		Rev
Unicorn LV530_KBL_MB14		SA	
Date: Friday, December 15, 2017	Sheet 19 of		105

Main Func = PCH



GSP11_MOSI/GPP_B22
Usage: Boot BIOS Strap Bit BBS
When Sampled: Rising edge of PCH_PWROK
The signal has a weak internal Pull-down.
Bit 6 Boot BIOS Destination
0 SPI (Default)
1 LPC
The internal Pull-down is disabled after PCH_PWROK de-asserts.

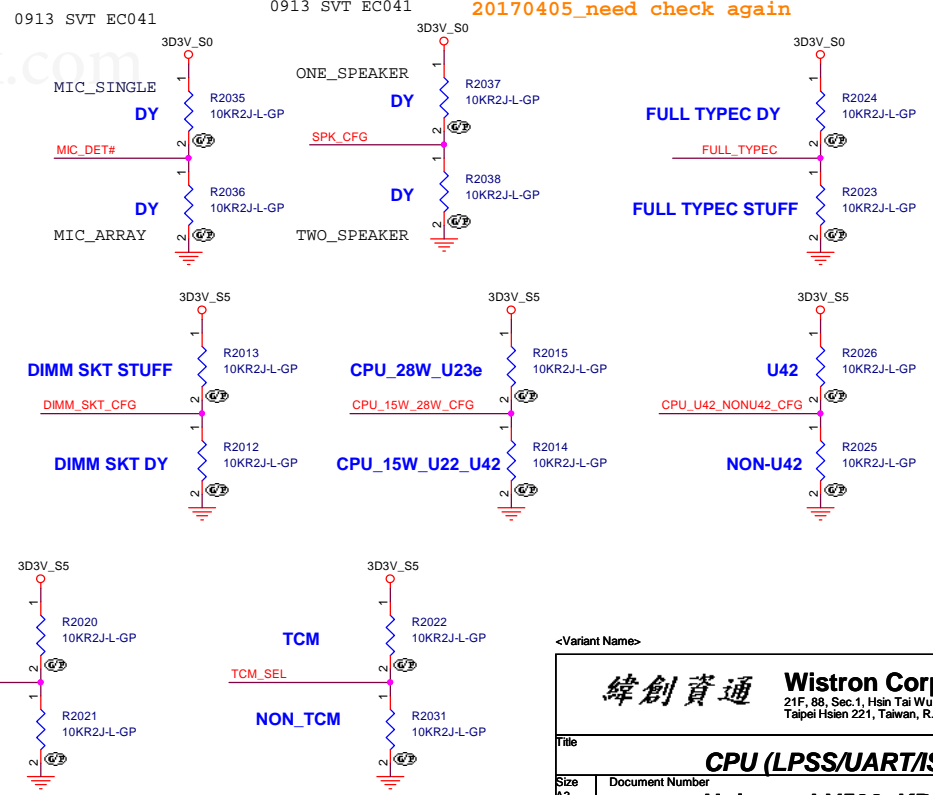
GSP10_MOSI/GPP_B18
Usage: No Reboot
When Sampled: Rising edge of PCH_PWROK
The signal has a weak internal Pull-down.
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
The internal Pull-down is disabled after PCH_PWROK de-asserts.



Delete TCM_DET_N 20170417

20170328 added by EE that is for R16M

071.SKYLA.000U BOM Change : KabyLake



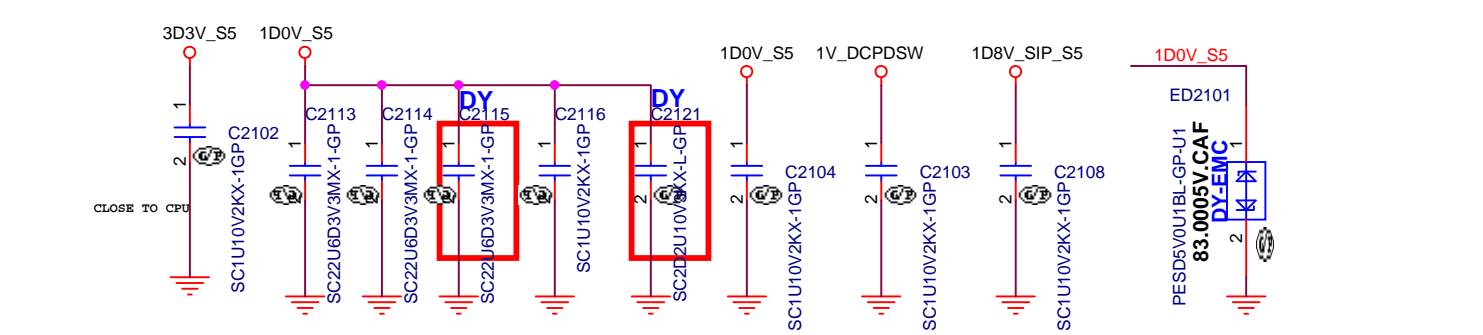
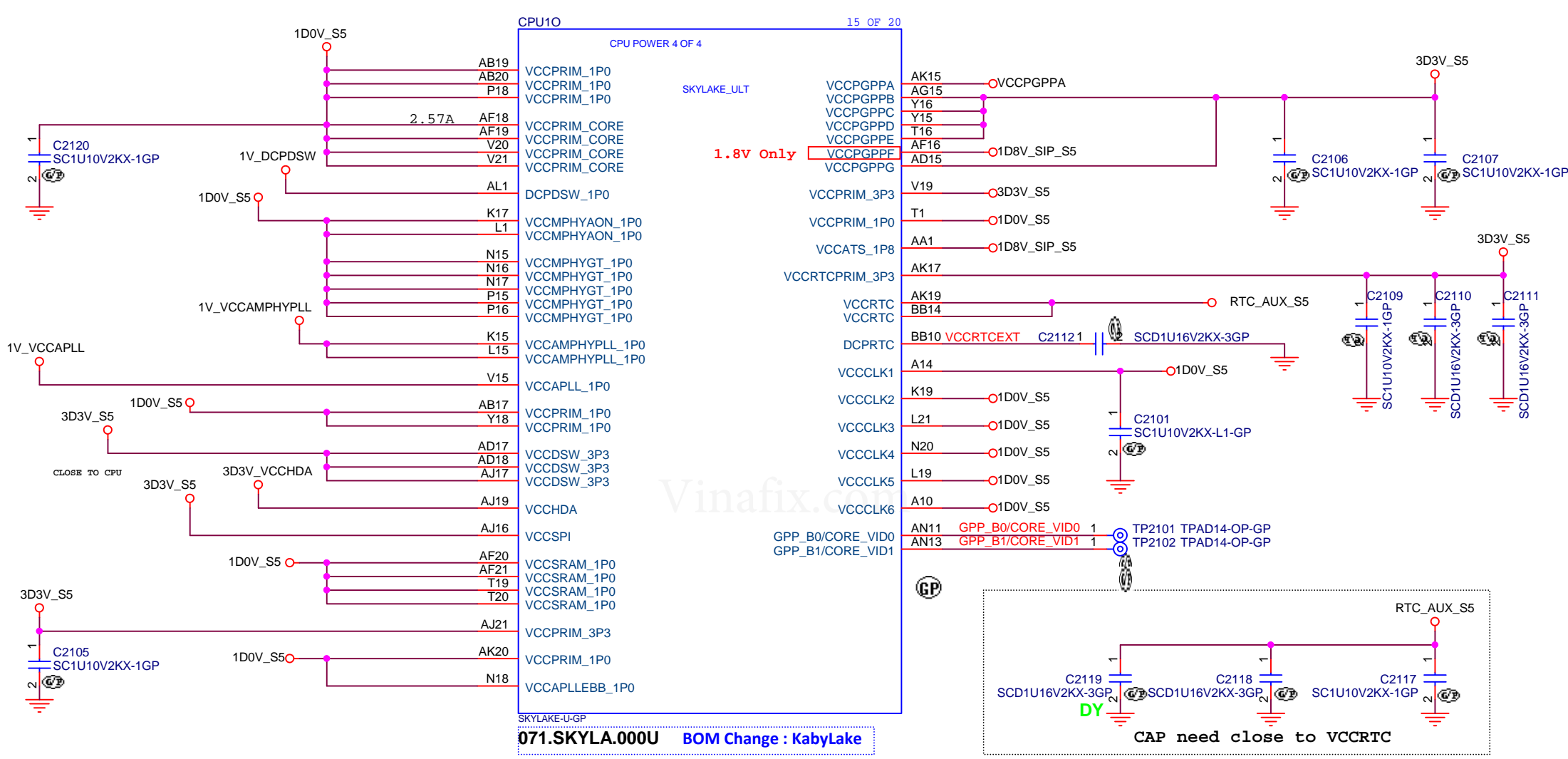
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

CPU (LPSS/UART/ISH)

Document Number: **Unicorn LV530 KBL MB11A**

Date: Friday, December 15, 2017 Sheet 20 of 105

Main Func = PCH



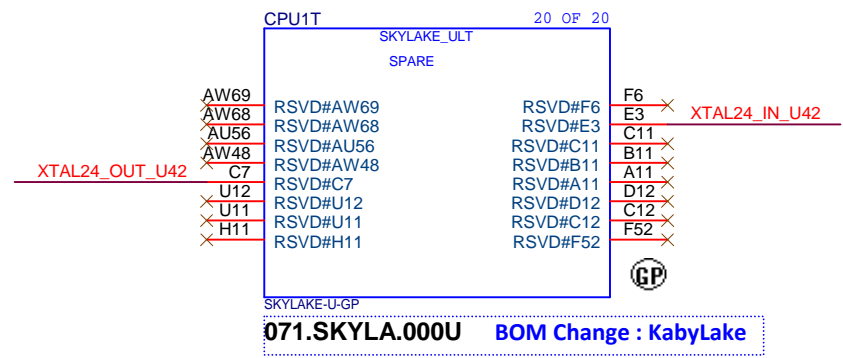
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緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

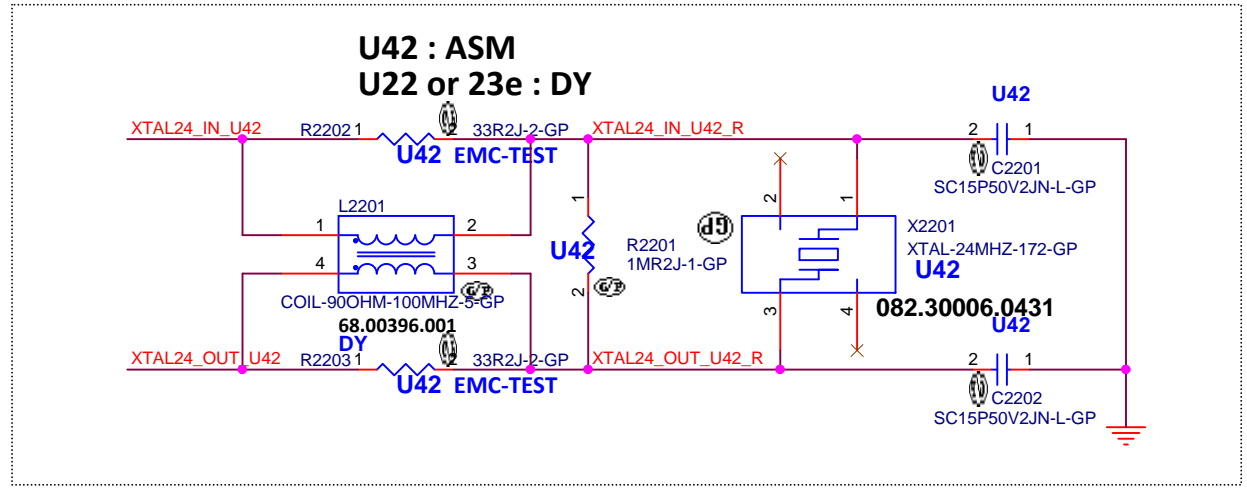
Title: **CPU (POWER1)**

Size A4	Document Number	Rev
Unicorn LV530 KBL MB 6A		
Date: Friday, December 15, 2017	Sheet 21 of 105	

Main Func = PCH



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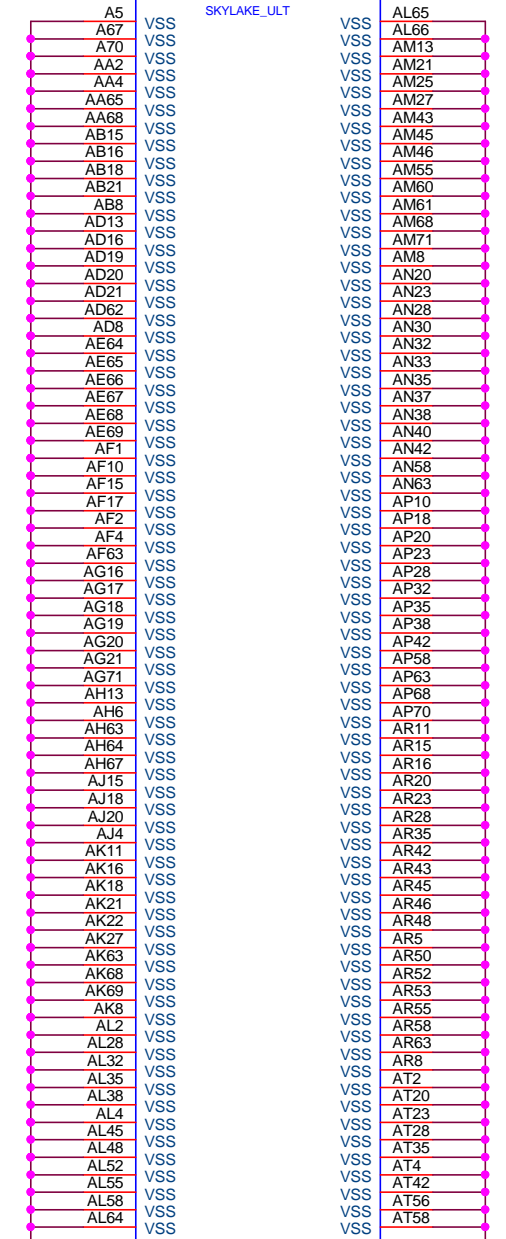
<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU (RSVD)			
Size	Document Number	Rev	
A4		Unicorn LV530 KBL MB GA	
Date:	Friday, December 15, 2017	Sheet	22 of 105

Main Func = PCH

CPU1P 16 OF 20

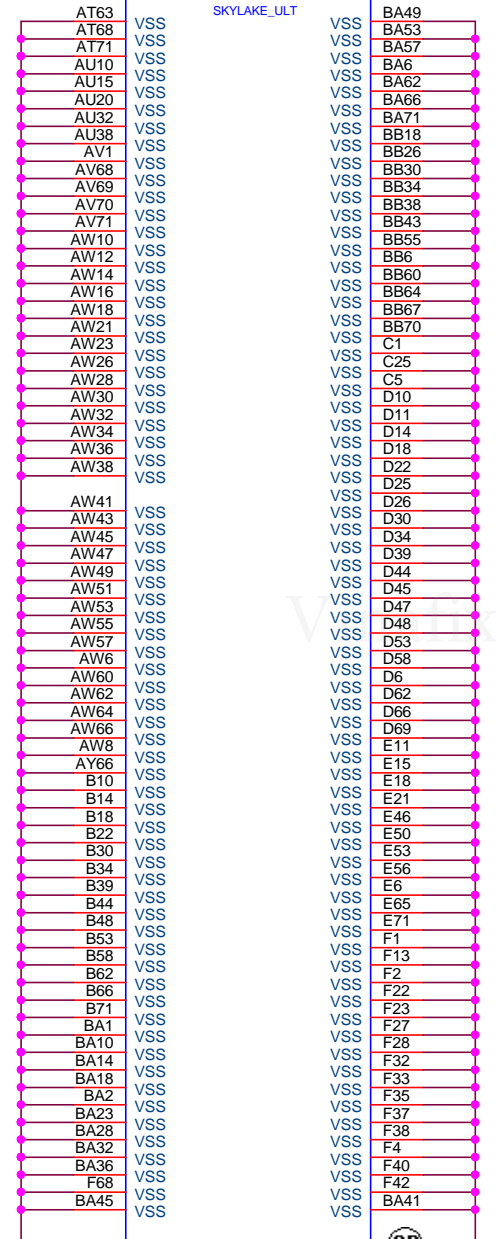
GND 1 OF 3



SKYLAKE-U-GP
071.SKYLA.000U BOM Change : KabyLake

CPU1Q 17 OF 20

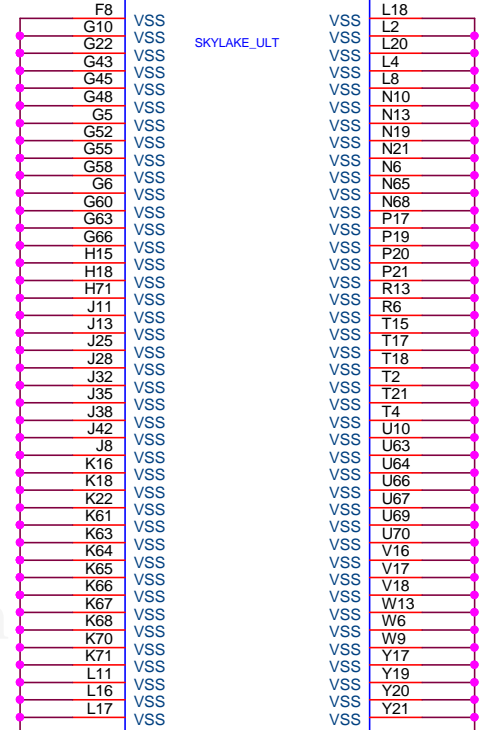
GND 2 OF 3



SKYLAKE-U-GP
071.SKYLA.000U BOM Change : KabyLake

CPU1R 18 OF 20

GND 3 OF 3



SKYLAKE-U-GP
071.SKYLA.000U BOM Change : KabyLake

<Variant Name>

 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
CPU (VSS)	
Size Custom	Document Number
Unicorn LV530 KBL MB 6A	
Date: Friday, December 15, 2017	Rev 1
Sheet 23 of 105	

20170707_need check

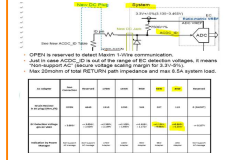
Model ID BOM Ctrl

PCB VERSION AD(PIN#)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
E51_KBL	100.0K	18.0K 64.10025.L0L	3.0V
E53_KBL	100.0K	20.0K 64.20025.L0L	2.75V
V30_KBL	100.0K	33.0K 64.33025.L0L	2.8V
V30_KBL	100.0K	47.0K 64.47025.A0L	2.34V
NA	100.0K	64.9K 64.64925.A0L	2.8V
V110-15KB V110 EC001	100.0K	76.8K 64.76825.A0L	1.8V
NA	100.0K	215.0K 64.21535.A0L	1.048V

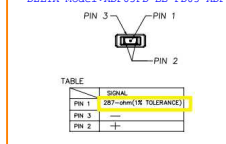
PCB VERSION

PCB VERSION AD(PIN#)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
NA	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.8V
SD	100.0K	47.0K	2.34V
-1	100.0K	64.9K	2.8V
-1M	100.0K	76.8K	1.8V
PVT BC051	-2	NA	NA
-3	100.0K	180.0K	1.64V
-2	100.0K	133.8K(133.85.A0L)	1.71V
-4	100.0K	174.8K(174.83.A0L)	1.30V

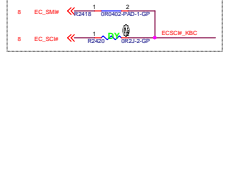
SPIC: ADT PWR Detection Function V1.3



DELTA Model:ADP65FD BB-FD03 ADP



Prevent BIOS data loss solution

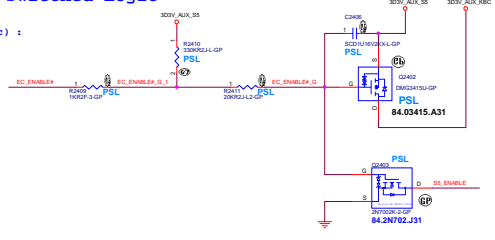


Nuvoton KBC PSL Power Switched Logic

1. Enter PSL mode (Entry S5 after 10sec) : 3D3V_AUX_KBC : OFF (KBC PWR supply)
2. At PSL mode (SPEC: S5<10mV)

PSL mode (AC or DC) :	PSL	
RC_ENABLE_G	SS_ENABLE	3D3V_AUX_KBC
HL	Low	OFF

PSL Wake (AC or DC) :	PSL	
RC_ENABLE_G	SS_ENABLE	3D3V_AUX_KBC
Low	HL	ON



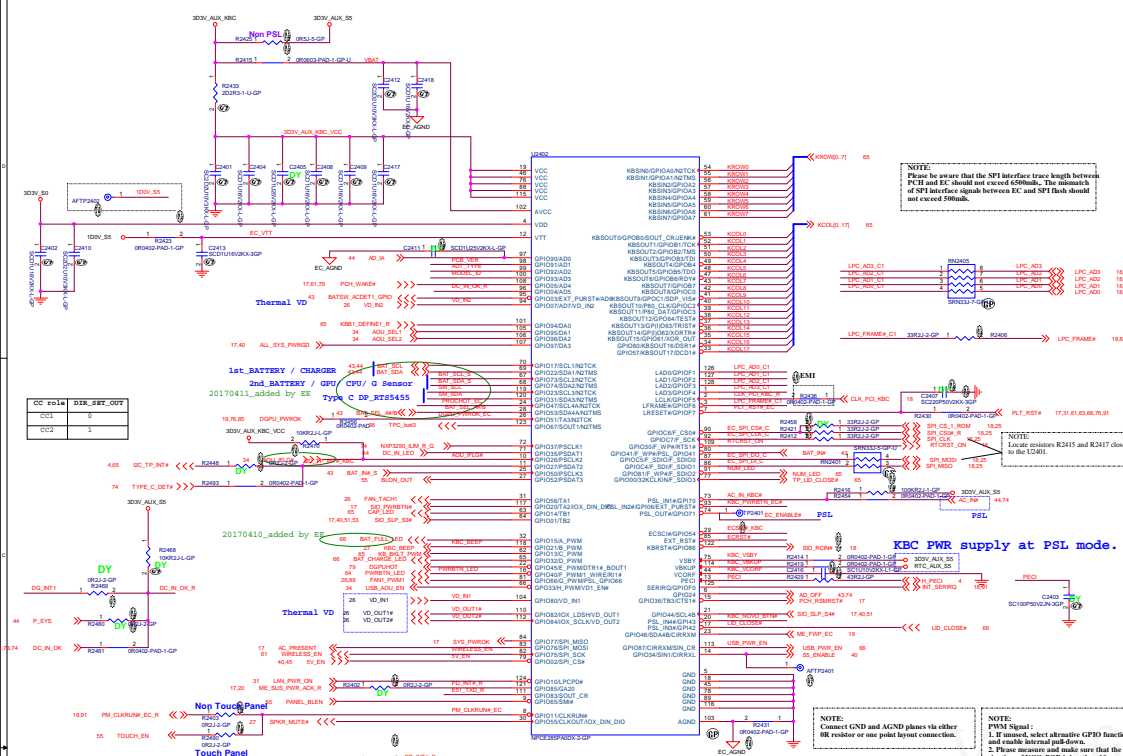
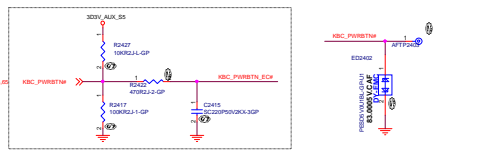
EC GPIO4 High Active



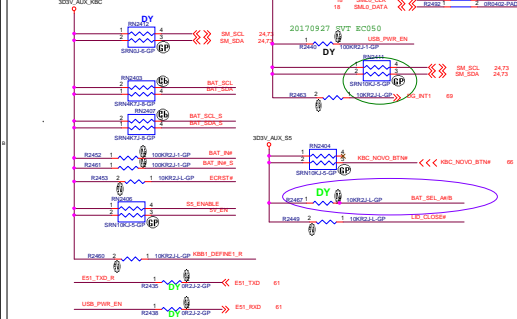
NOVO button Fun define: one key to recover OS.

NOVO button wake KBC at PSL mode.	KBC_NOVO_BTN	ESC_PWRBTN_EC0
Low	Low	Low

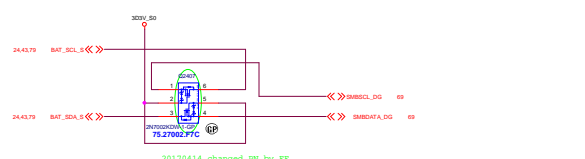
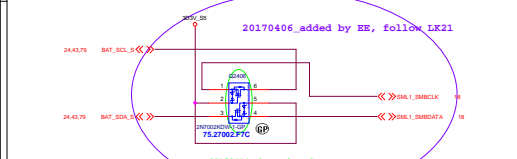
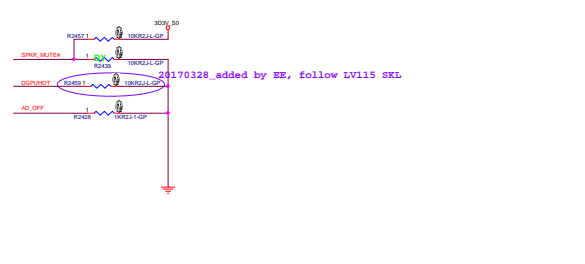
KBC_PWRBTN_EC# : Low
 (1) 4sec: PWR
 Button shut down
 (2) 8sec: KBC reset



EC GPIO PH



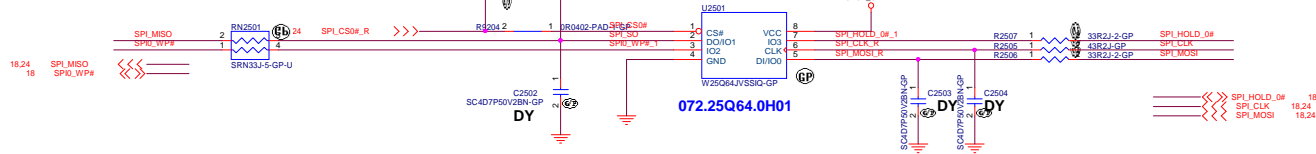
EC GPIO PL



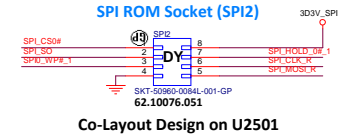
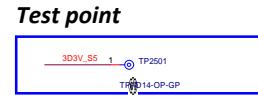
SSID = Flash.ROM

SPI ROM Equal length need to less than 500mil

1ST	MXIC	8MB	072.25647.000D
2ND	WINBOND	8MB	072.25Q64.0H01
3RD	GIGA DEVICE	8MB	072.25864.0C01

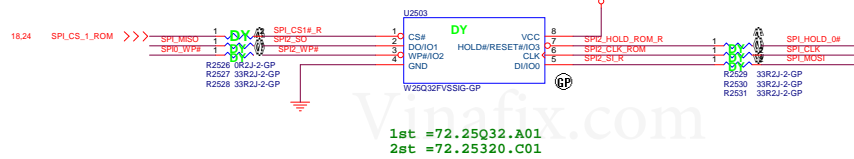


- 16MB SOIC8
- WINBOND W25Q128FVSIQ/ 72.25128.0E1
- WINBOND W25Q128FVSIQ/ 072.25128.0AC1
- MACRONIX MX25L12873FM2I-10G/ 72.12873.001
- MACRONIX MX25L12873FM2I-10G/ 072.25128.0B11



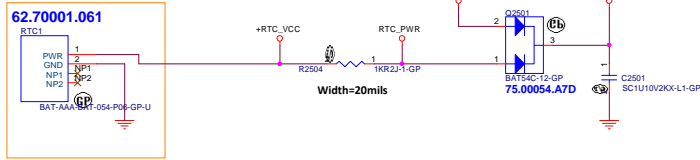
Co-Layout Design on U2501

SPI FLASH ROM 4M byte

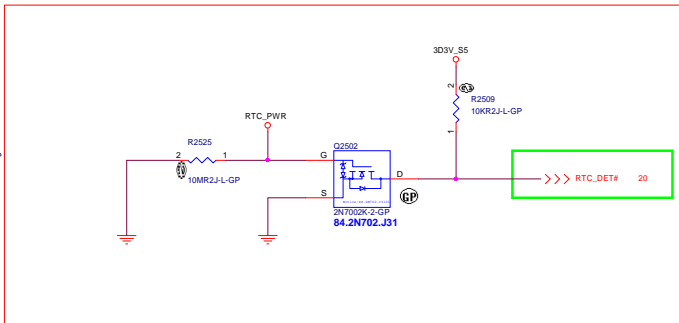
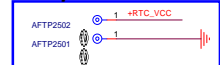


SSID = RBATT

20170320_need check pin define with ME



Test point

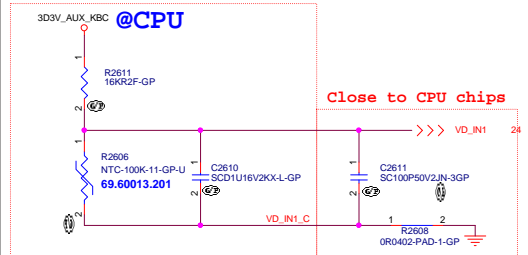


High Detect
Need to Check whether to PD in PCH Side

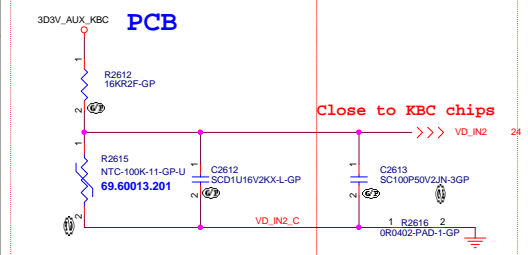
<-Variant Name-

Main Func = Thermal Sensor

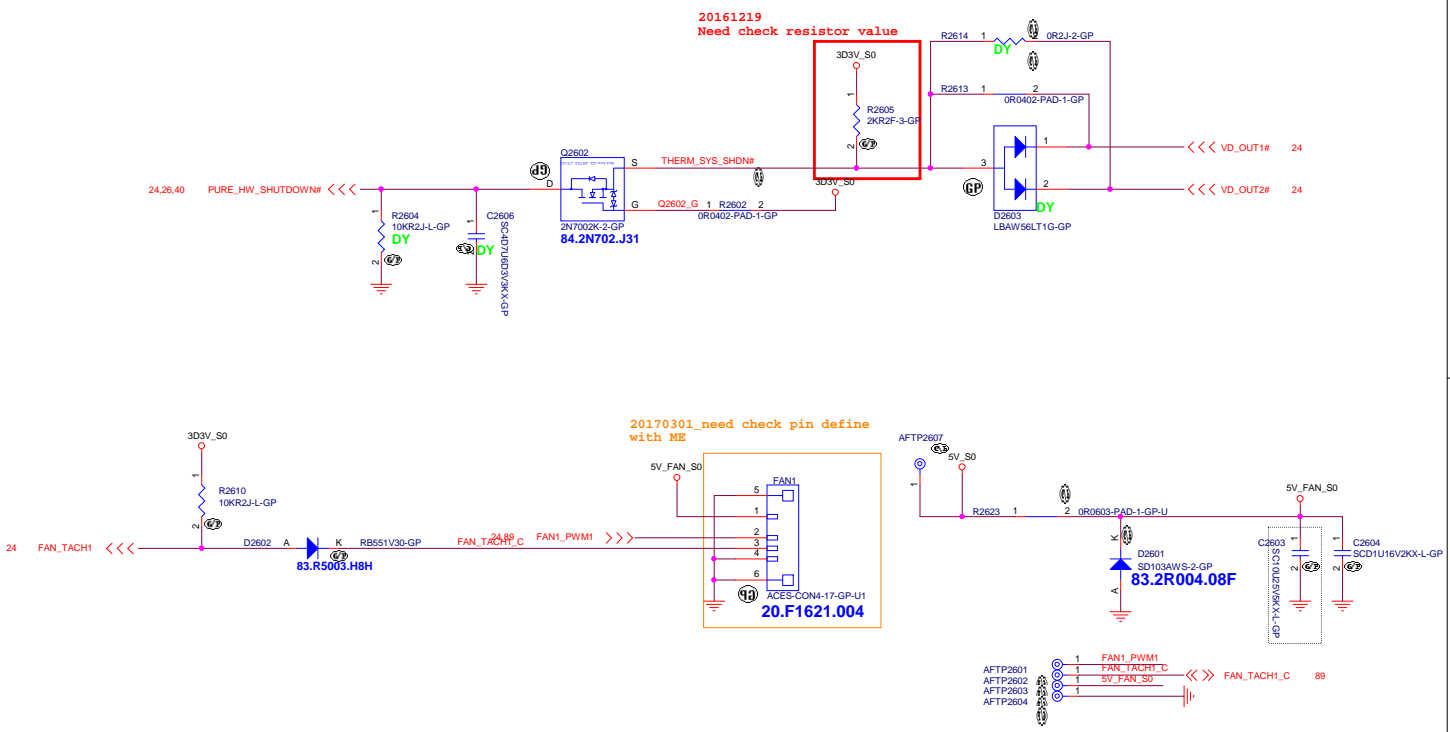
Close to Thermal sensor



Close to CPU chips



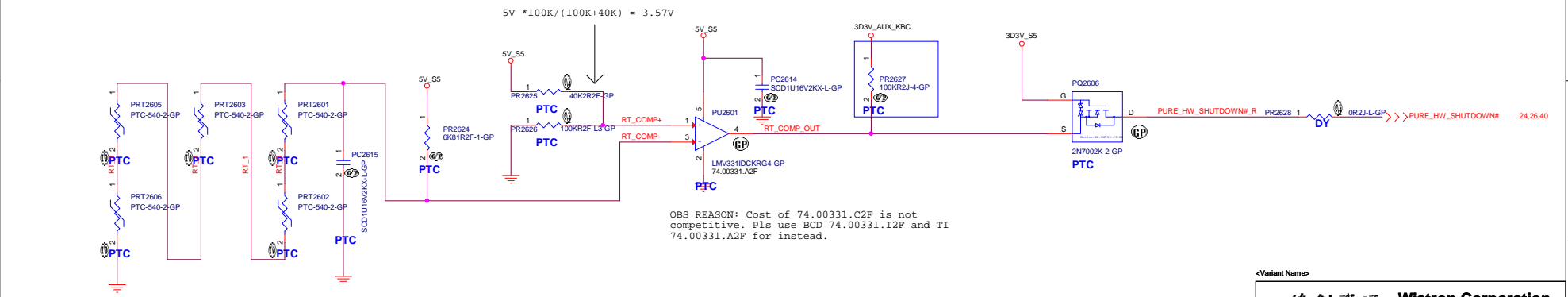
Close to KBC chips



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PURE_HW_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low



OBS REASON: Cost of 74.00331.C2F is not competitive. Pls use BCD 74.00331.I2F and TI 74.00331.A2F for instead.

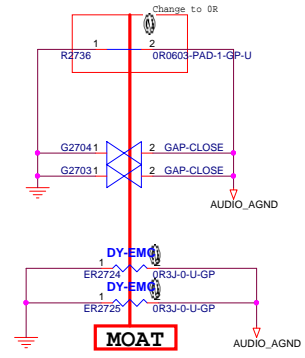
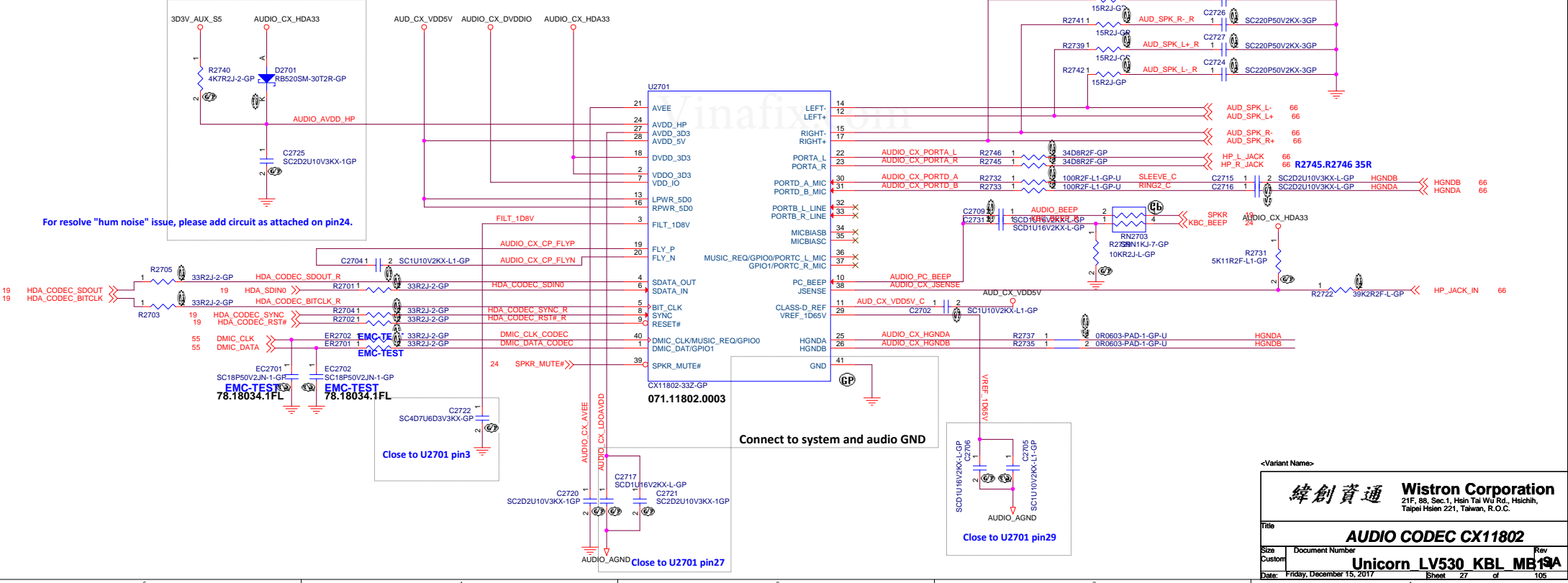
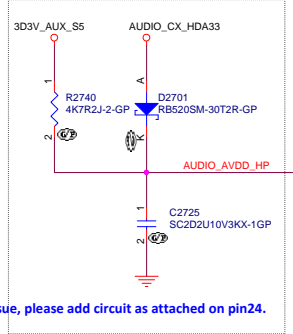
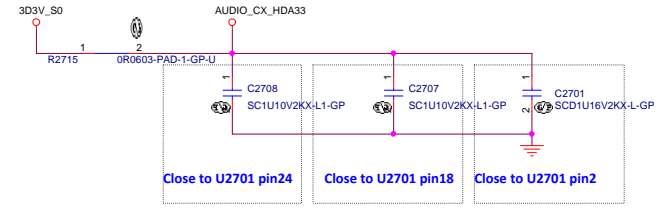
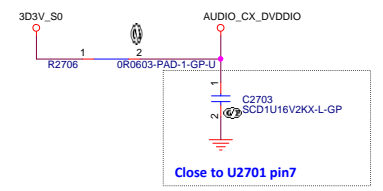
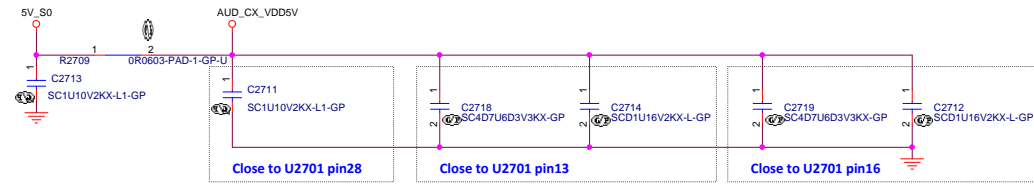
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緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hei Tai Wu Rd., Hsichih, Taipei Heien 221, Taiwan, R.O.C.

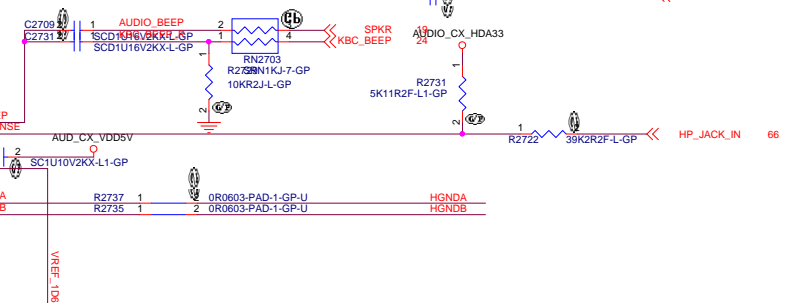
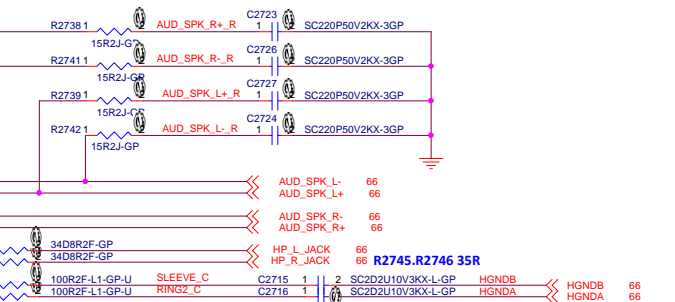
Title: **THERMAL/FAN**

Size: Custom Document Number: **Unicorn LV530 KBL ME19A** Rev: **ME19A**

Date: Friday, December 15, 2017 Sheet: 26 of 105



Install snubber networks on each net of SPKs helps control the overshoot/undershoot at the class-D outputs.



<p>緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title: AUDIO CODEC CX11802</p>	
<p>Spec: Custom</p>	<p>Document Number: Unicorn LV530 KBL MB19A</p>
<p>Date: Friday, December 15, 2017</p>	<p>Rev: 19A Sheet 27 of 105</p>

TABLE : Automatic Switching Mode (CFG0 = H)

SW (DDI_PRIORITY2)

L Port 1 has higher priority when both ports are plugged
 H Port 2 has higher priority when both ports are plugged

For Automatic Switching Mode (CFG0 = H):

SW = L: Port1 has higher priority when both ports are plugged (default)

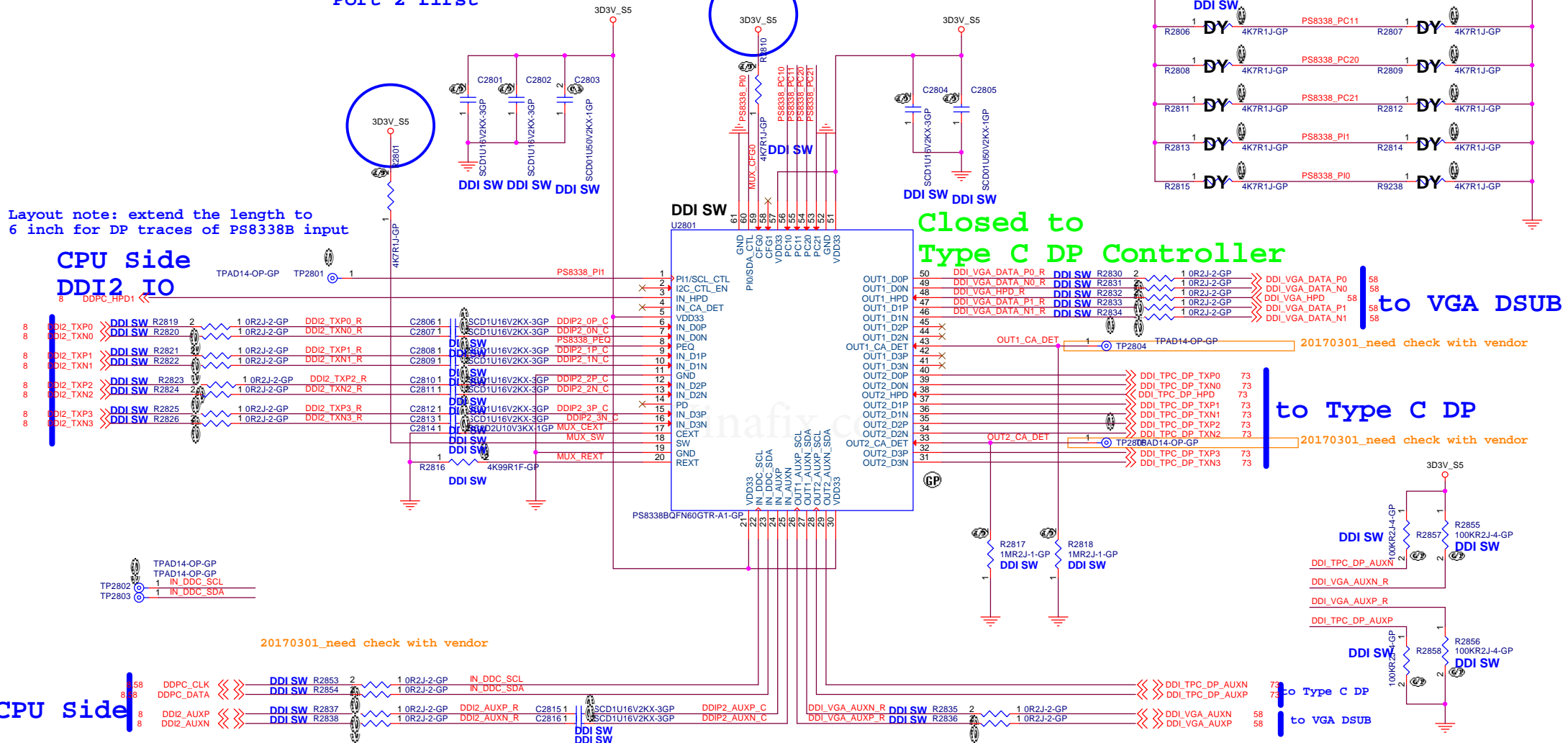
SW = H: Port2 has higher priority when both ports are plugged

Overwritten by I2C register in I2C Control Mode

Port 2 first

Layout note: extend the length to 6 inch for DP traces of PS8338B input

CPU side
DDI2 IO



20170301_need check with vendor

CPU side

Bypass DDI SW

DDI2_TXP0	VGA	R2839	2	1 0R2J-2-GP	DDI2_TXP0 BYPASS	VGA	R2840	2	1 0R2J-2-GP	DDI_VGA_DATA_P0
DDI2_TXN0	VGA	R2841	2	1 0R2J-2-GP	DDI2_TXN0 BYPASS	VGA	R2842	2	1 0R2J-2-GP	DDI_VGA_DATA_N0
DDI2_TXP1	VGA	R2843	2	1 0R2J-2-GP	DDI2_TXP1 BYPASS	VGA	R2844	2	1 0R2J-2-GP	DDI_VGA_DATA_P1
DDI2_TXN1	VGA	R2845	2	1 0R2J-2-GP	DDI2_TXN1 BYPASS	VGA	R2846	2	1 0R2J-2-GP	DDI_VGA_DATA_N1
DDI2_AUXN	VGA	R2847	2	1 0R2J-2-GP	DDI2_AUXN BYPASS	VGA	R2848	2	1 0R2J-2-GP	DDI_VGA_AUXN
DDI2_AUXP	VGA	R2849	2	1 0R2J-2-GP	DDI2_AUXP BYPASS	VGA	R2850	2	1 0R2J-2-GP	DDI_VGA_AUXP
DDPC_HPD1	VGA	R2851	2	1 0R2J-2-GP	DDPC_HPD1 BYPASS	VGA	R2852	2	1 0R2J-2-GP	DDI_VGA_HPD

<Variant Name>

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **DDI Switch**

Size A3 Document Number: **Unicorn LV530 KBL MB13A** Rev

Date: Friday, December 15, 2017 Sheet 28 of 105

**INTERNAL STEREO SPEAKERS
MOVE TO SMALL BOARD**

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<Variant Name>		
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title AUDIO SPEAKER		
Size A3	Document Number Unicorn LV530 KBL MB13A	Rev 13A
Date: Friday, December 15, 2017	Sheet 29	of 105

Vinafix.com

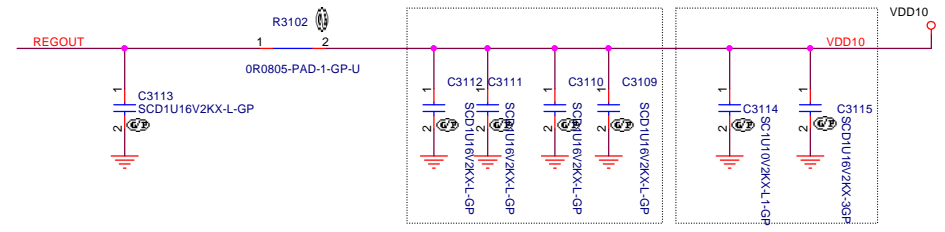
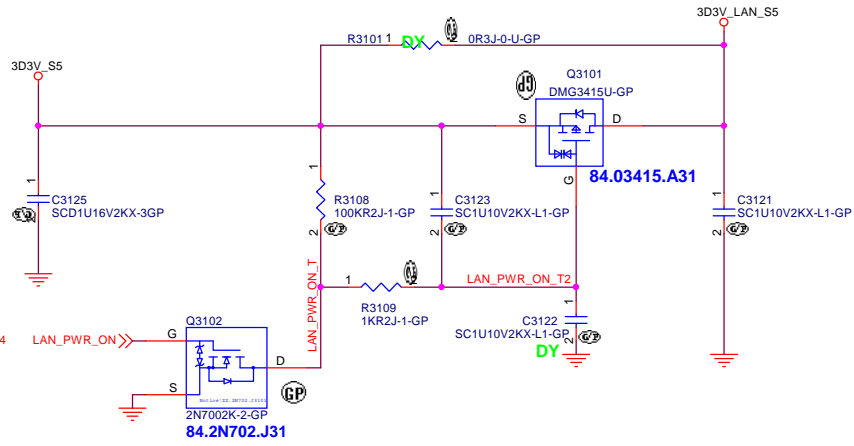
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

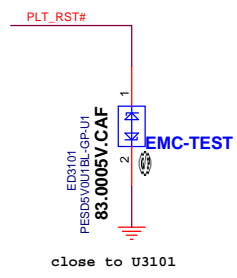
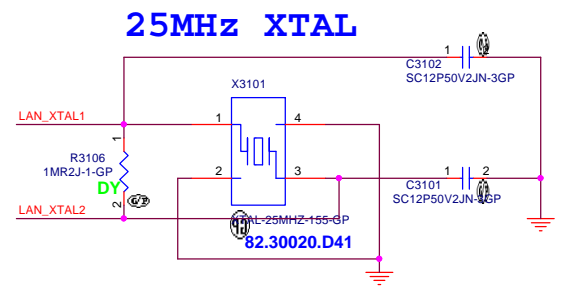
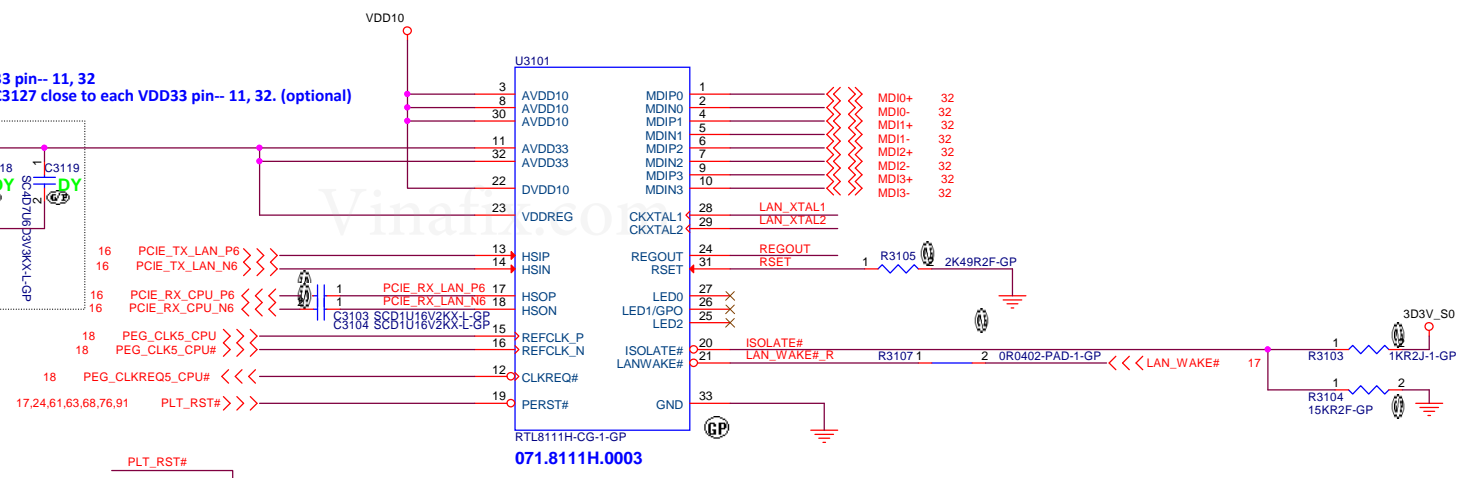
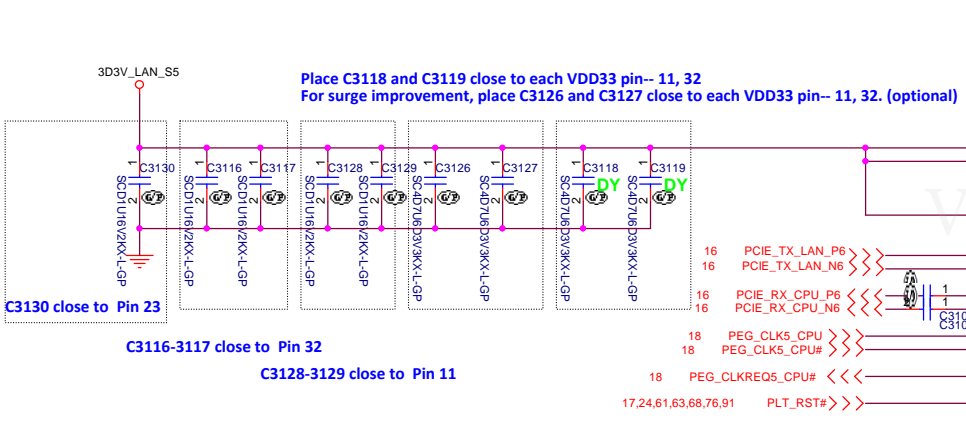
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(RESERVED)

Size A4	Document Number Unicorn_LV530_KBL_MB14BOHOL	Rev SA
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Date: Friday, December 15, 2017 Sheet 30 of 105

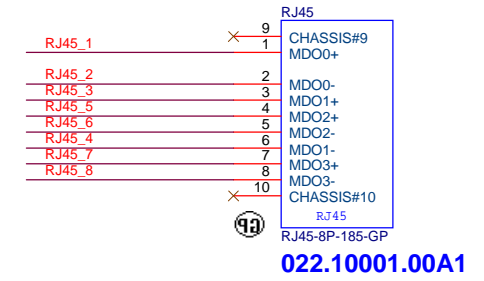
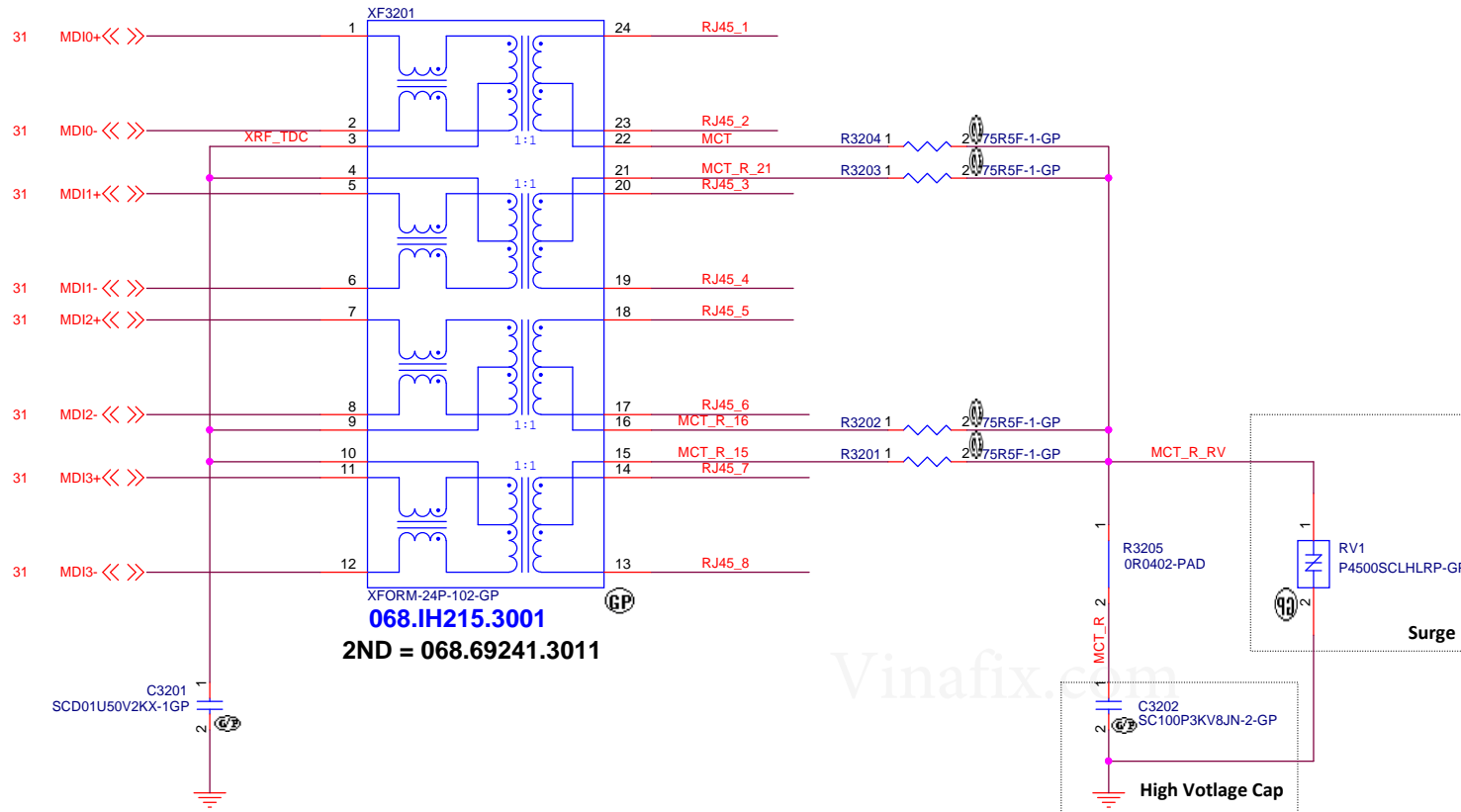


For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
 *Place C3109 to C3112 close to each VDD10 pin-- 3, 8, 22, 30
 For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
 *Place C3114 and C3115 close to each VDD10 pin-- 22 (Reserved)

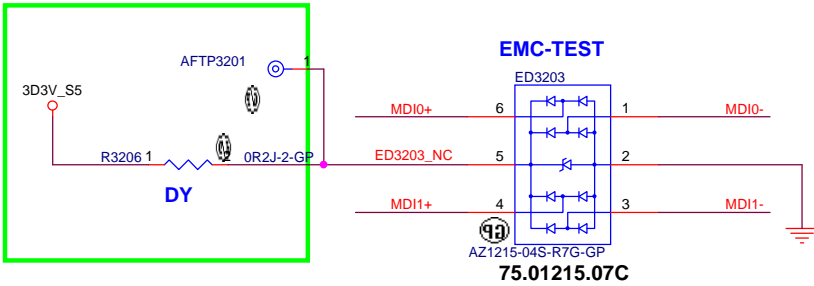


10/100M/1000M Lan Transformer

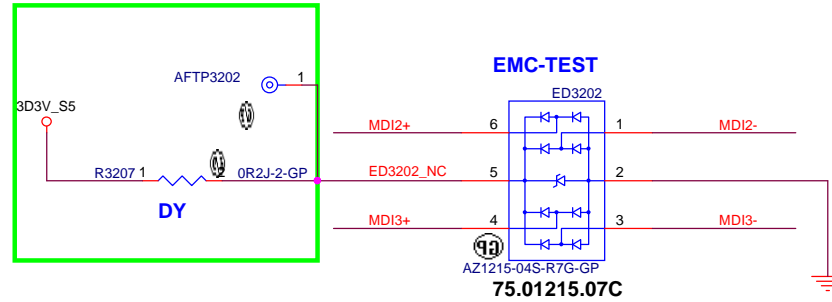
LAN Connector



20170606
EMC Tim Lee requirement



20170606
EMC Tim Lee requirement



<Variant Name>

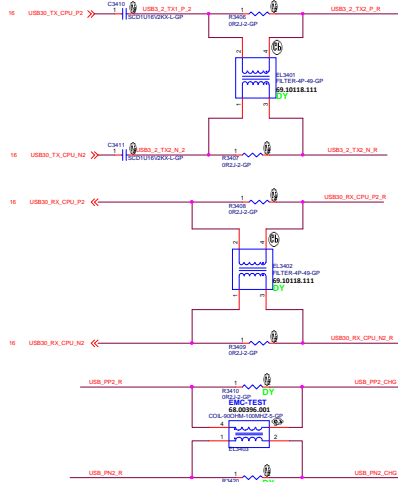
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
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RJ45			
Size	Document Number	Rev	
Custom	Unicorn LV530 KBL MB13A		
Date:	Friday, December 15, 2017	Sheet	32 of 105

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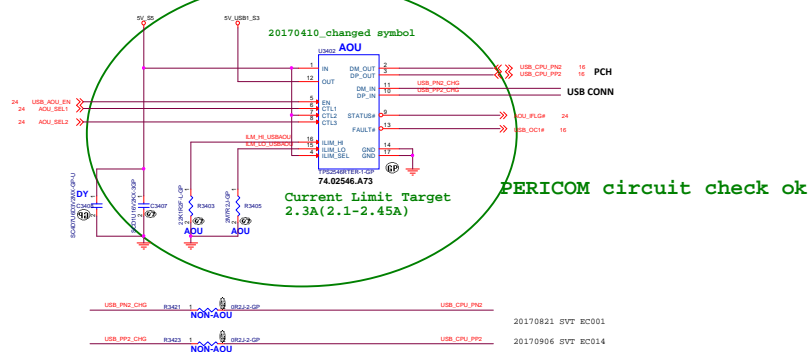
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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Size A3	Document Number Unicorn_LV530_KBL_MB14V530	Rev SA	SA
Date: Friday, December 15, 2017		Sheet 33	of 105

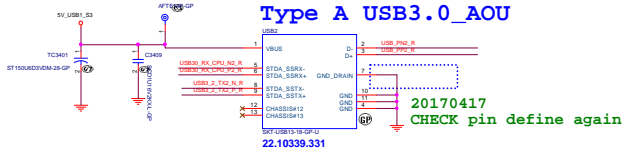
needReserve USB2.0 by pas AOU



AOU
 1ST,
 TI, 74.02546.A73
 IC PWR SW TPS2546RTER QFN 16P(REV 1.1)
 2ND
 PERICOM, 074.52546.0A73
 IC PWR SW PI5USB2546ZHEX TQFN 16P REV.X

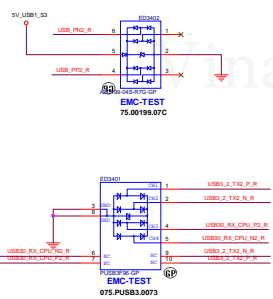


USB Port2
 Type A USB3.0_AOU



20170417
 CHECK pin define again

USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	St-dA_SSRX-	SuperSpeed RX
6	St-dA_SSRX+	
7	GND	
8	St-dA_SSTX-	SuperSpeed TX
9	St-dA_SSTX+	



1. When AOU function is N.A., need added USB Current limite /SY6288C20AAC
 2. circuit of AOU and USB Current limite /SY6288C20AAC need BOM control, added by symbol

RESERVED

<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB30 RE-DRIVER			
Size	Document Number	Rev	
A3	Unicorn_LV530_KBL_MB13A	1.0	
Date: Friday, December 15, 2017		Sheet	35 of 105

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<Variant Name>		
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(RESERVED)		
File	Document Number	Rev
	Unicorn LV530 KBL MB SA	6A
Size A2	Date: Friday, December 15, 2017	Sheet 36 of 105

5

4

3

2

1

D

D

C

C

B

B

A

A

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<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
TYPEC USB3.1-1			
Size	Document Number		Rev
A4	Unicorn LV530 KBL MB SA		1A
Date: Friday, December 15, 2017		Sheet 37	of 105

5

4

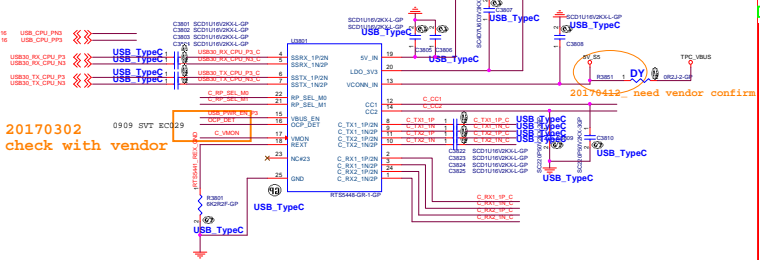
3

2

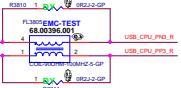
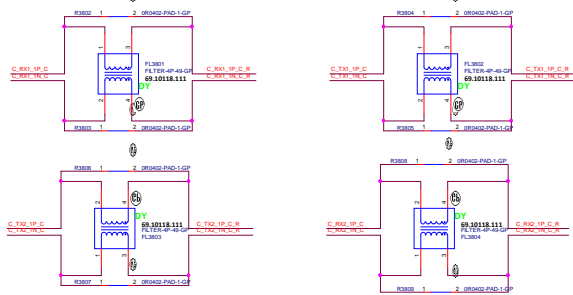
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USB Port3, Type C USB3.0 only

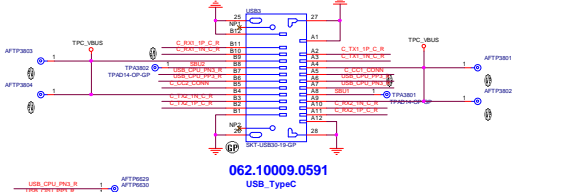
Type C controller_MUX



20170302 check with vendor

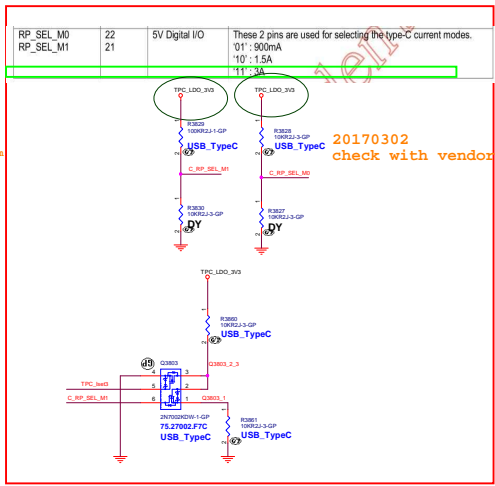
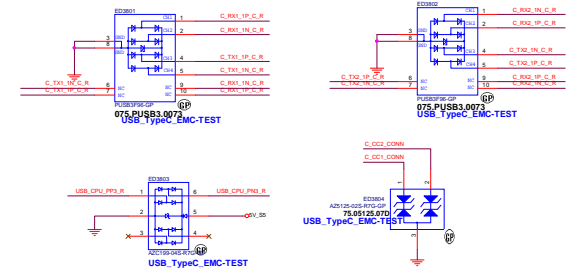


USB Port3, Type C USB3.0 only

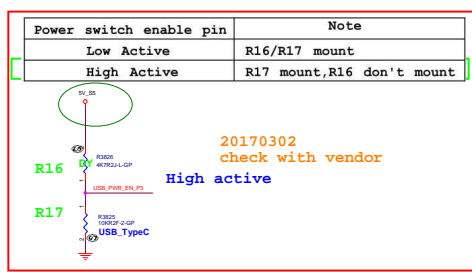


062.10009.0591 USB_TypeC

Close to CONN



20170302 check with vendor

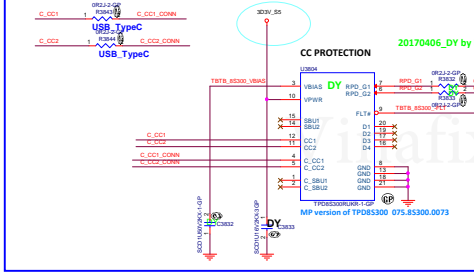


Power switch enable pin	Note
Low Active	R16/R17 mount
High Active	R17 mount, R16 don't mount

20170302 check with vendor High active

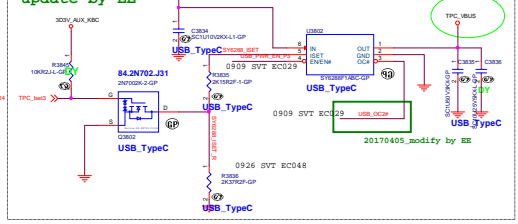
Power switch enable pin	Note
Low Active	R3826/R3825 mount
High Active	R3825 mount, R3826 don't mount

CC Protect Function



20170406_DY by EE

CC Limit_3A



20170322 update by EE

- 1. AC: 15W / 3A, 系統功耗不足降至4.5W / 0.9A
- 2. DC: 4.5W / 0.9A

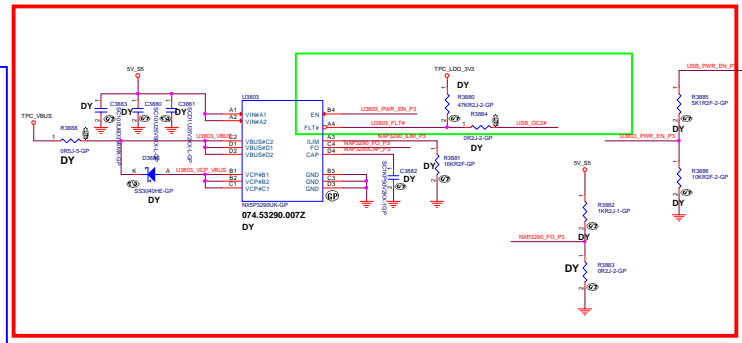
Over-current protection

The SY6288F1/F2 supports Current limit programming. Connect a resistor R_{SET} from ISET pin to ground to program the current limit:

$$I_{LIM} (A) = 6800 / R_{SET} (\Omega)$$

The minimum current limit is 0.4A. Current limit beyond 4A is not recommended.

- R3835/ 2.15K >> 3.16A
- R3835/ 2.15K + R3836/ 5.1K >> 0.94A



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<Variant Name>

<Title>

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Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Size

A

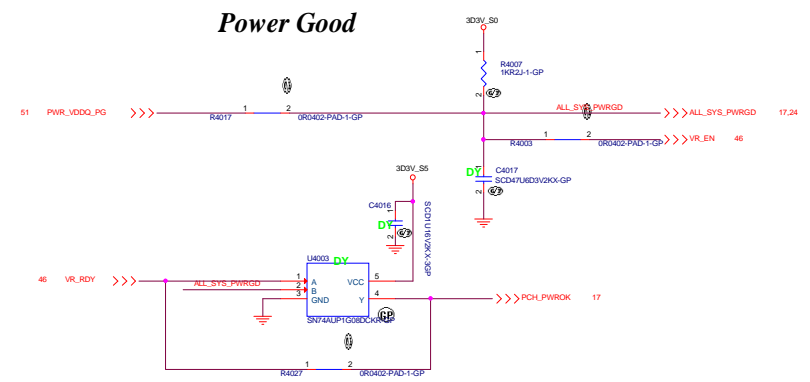
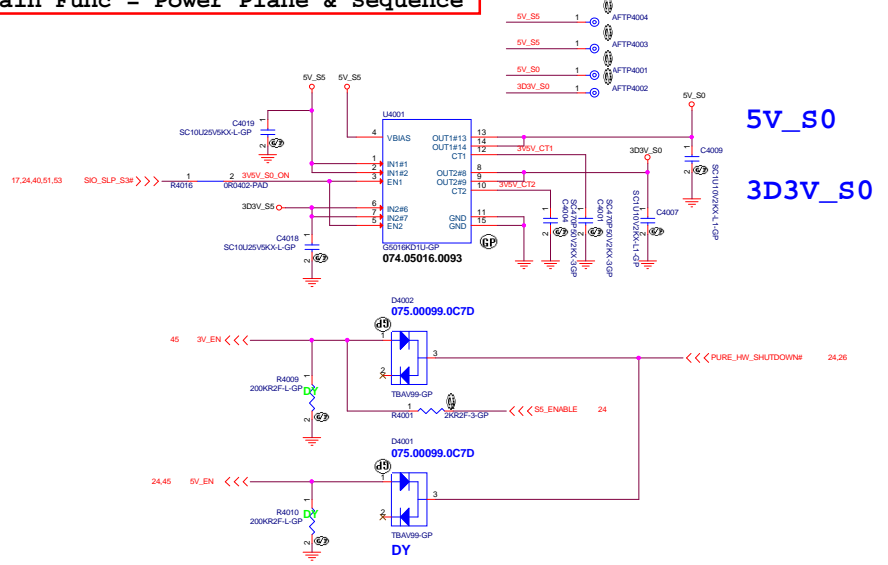
Document Number

Unicorn_LV530_KBL_MB14BOH01SA

Rev

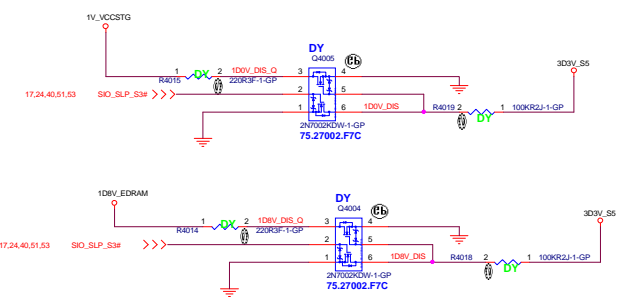
Date: Friday, December 15, 2017

Sheet 39 of 105

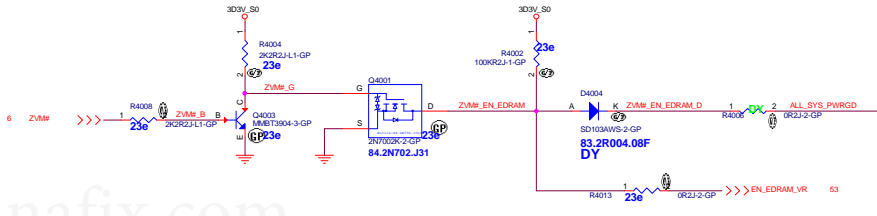


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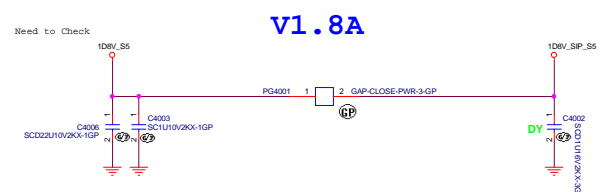
Discharge circuit



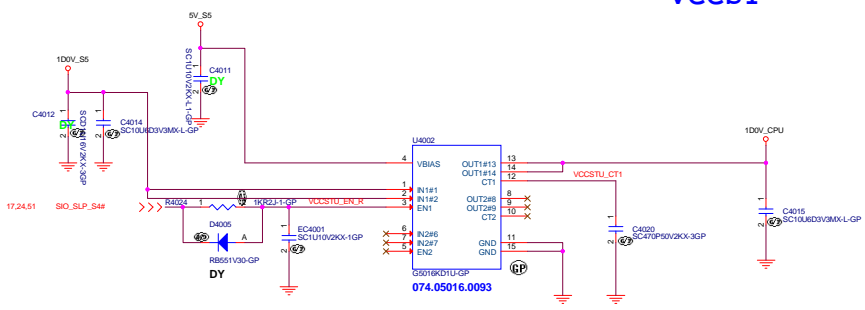
GT3 Low Power Circuit (ZVM)



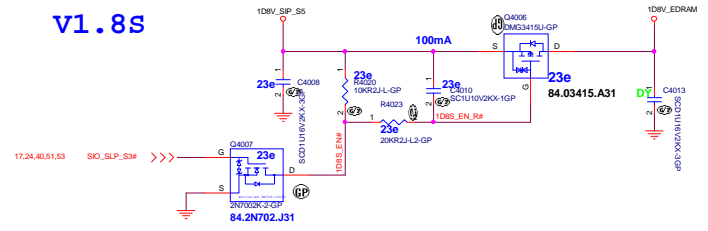
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VCCST



V1.8S



V1L > 0.7 V, V1M < 2 V
 Rds(on) = 11 mΩ @ VDD = 4 V
 Ids(max) 1.0 A

561280 KBL UY PDG Rev2.0 Notes:
 On power up sequence, VCC0PC_lpb8 must never ramp up after VCC0PC/VCC0PIO under any circumstance.
 There are no ramp down requirements between VCC0PC_lpb8 and VCC0PC/VCC0PIO.
 Platform must guarantee VCC0PC/VCC0PIO falls do not start ramping back up for any reason while VCC0PC_lpb8 is ramping down or off.

5

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<Variant Name>

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Title

<Title>

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Document Number

Rev

A

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<RevCode>

Date:

Friday, December 15, 2017

Sheet

41

of

105

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(Blank)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size
A4

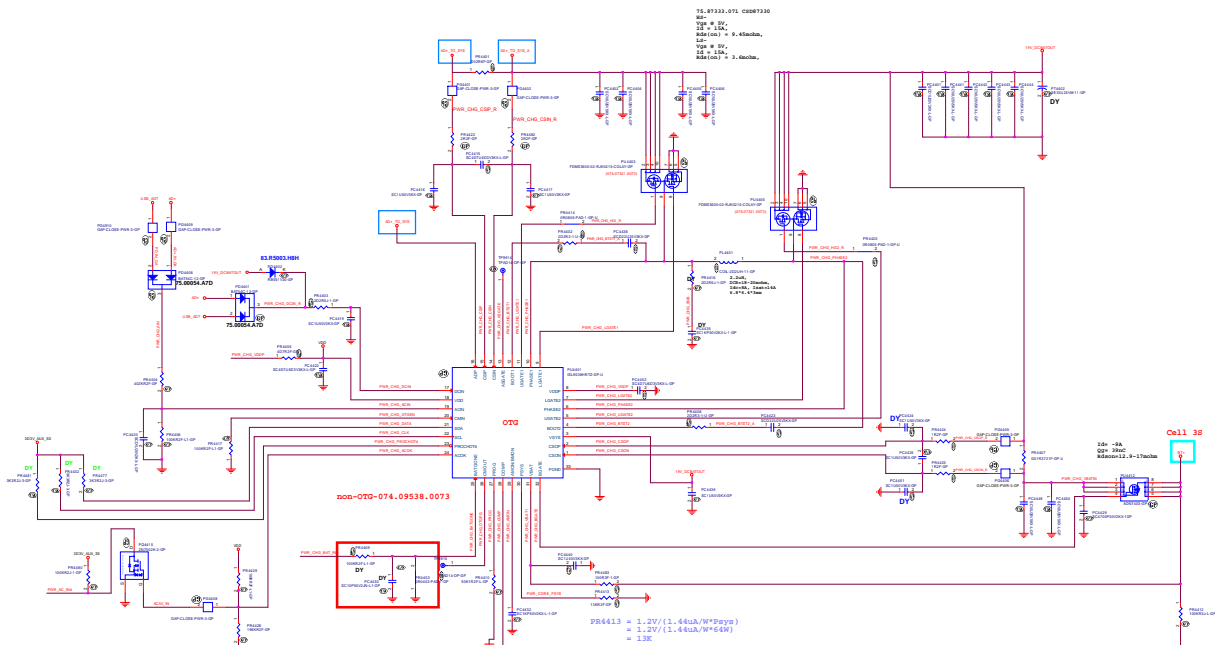
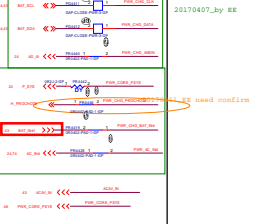
Document Number

Unicorn LV530 KBL MB SA

Rev

Date: Friday, December 15, 2017

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21_01221_071 C0087330
 V_{CC} = 5V
 V_{DD} = 1.8V
 V_{DDIO} = 1.8V
 V_{DDIO2} = 1.8V
 V_{DDIO3} = 1.8V
 V_{DDIO4} = 1.8V
 V_{DDIO5} = 1.8V
 V_{DDIO6} = 1.8V
 V_{DDIO7} = 1.8V
 V_{DDIO8} = 1.8V
 V_{DDIO9} = 1.8V
 V_{DDIO10} = 1.8V
 V_{DDIO11} = 1.8V
 V_{DDIO12} = 1.8V
 V_{DDIO13} = 1.8V
 V_{DDIO14} = 1.8V
 V_{DDIO15} = 1.8V
 V_{DDIO16} = 1.8V
 V_{DDIO17} = 1.8V
 V_{DDIO18} = 1.8V
 V_{DDIO19} = 1.8V
 V_{DDIO20} = 1.8V
 V_{DDIO21} = 1.8V
 V_{DDIO22} = 1.8V
 V_{DDIO23} = 1.8V
 V_{DDIO24} = 1.8V
 V_{DDIO25} = 1.8V
 V_{DDIO26} = 1.8V
 V_{DDIO27} = 1.8V
 V_{DDIO28} = 1.8V
 V_{DDIO29} = 1.8V
 V_{DDIO30} = 1.8V
 V_{DDIO31} = 1.8V
 V_{DDIO32} = 1.8V
 V_{DDIO33} = 1.8V
 V_{DDIO34} = 1.8V
 V_{DDIO35} = 1.8V
 V_{DDIO36} = 1.8V
 V_{DDIO37} = 1.8V
 V_{DDIO38} = 1.8V
 V_{DDIO39} = 1.8V
 V_{DDIO40} = 1.8V
 V_{DDIO41} = 1.8V
 V_{DDIO42} = 1.8V
 V_{DDIO43} = 1.8V
 V_{DDIO44} = 1.8V
 V_{DDIO45} = 1.8V
 V_{DDIO46} = 1.8V
 V_{DDIO47} = 1.8V
 V_{DDIO48} = 1.8V
 V_{DDIO49} = 1.8V
 V_{DDIO50} = 1.8V
 V_{DDIO51} = 1.8V
 V_{DDIO52} = 1.8V
 V_{DDIO53} = 1.8V
 V_{DDIO54} = 1.8V
 V_{DDIO55} = 1.8V
 V_{DDIO56} = 1.8V
 V_{DDIO57} = 1.8V
 V_{DDIO58} = 1.8V
 V_{DDIO59} = 1.8V
 V_{DDIO60} = 1.8V
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 V_{DDIO62} = 1.8V
 V_{DDIO63} = 1.8V
 V_{DDIO64} = 1.8V
 V_{DDIO65} = 1.8V
 V_{DDIO66} = 1.8V
 V_{DDIO67} = 1.8V
 V_{DDIO68} = 1.8V
 V_{DDIO69} = 1.8V
 V_{DDIO70} = 1.8V
 V_{DDIO71} = 1.8V
 V_{DDIO72} = 1.8V
 V_{DDIO73} = 1.8V
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 V_{DDIO76} = 1.8V
 V_{DDIO77} = 1.8V
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 V_{DDIO79} = 1.8V
 V_{DDIO80} = 1.8V
 V_{DDIO81} = 1.8V
 V_{DDIO82} = 1.8V
 V_{DDIO83} = 1.8V
 V_{DDIO84} = 1.8V
 V_{DDIO85} = 1.8V
 V_{DDIO86} = 1.8V
 V_{DDIO87} = 1.8V
 V_{DDIO88} = 1.8V
 V_{DDIO89} = 1.8V
 V_{DDIO90} = 1.8V
 V_{DDIO91} = 1.8V
 V_{DDIO92} = 1.8V
 V_{DDIO93} = 1.8V
 V_{DDIO94} = 1.8V
 V_{DDIO95} = 1.8V
 V_{DDIO96} = 1.8V
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 V_{DDIO99} = 1.8V
 V_{DDIO100} = 1.8V

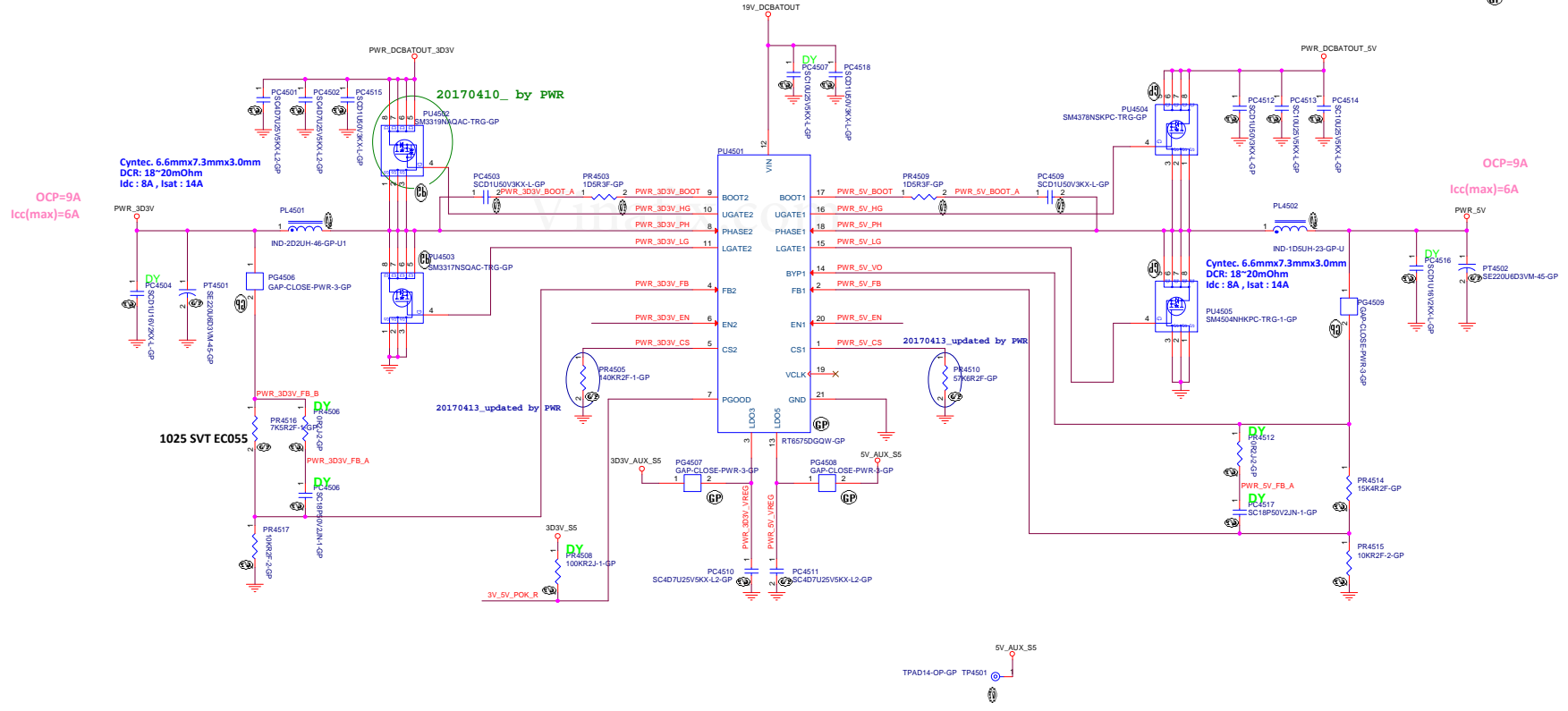
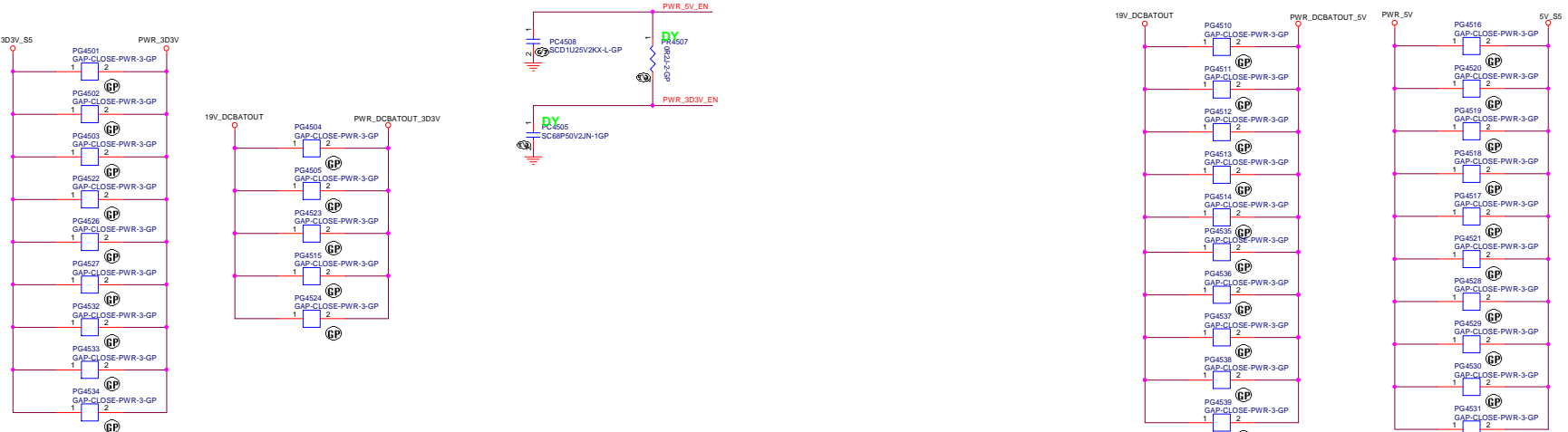
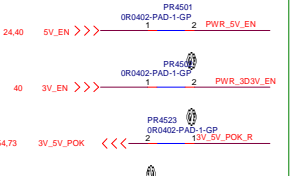
non-OTG-074.09538.0073

PR4413 = 1.2V / (1.44uA / (V_{DDIO} - V_{DDIO2}))
 = 1.2V / (1.44uA / (1.8V - 1.8V))
 = 1.32

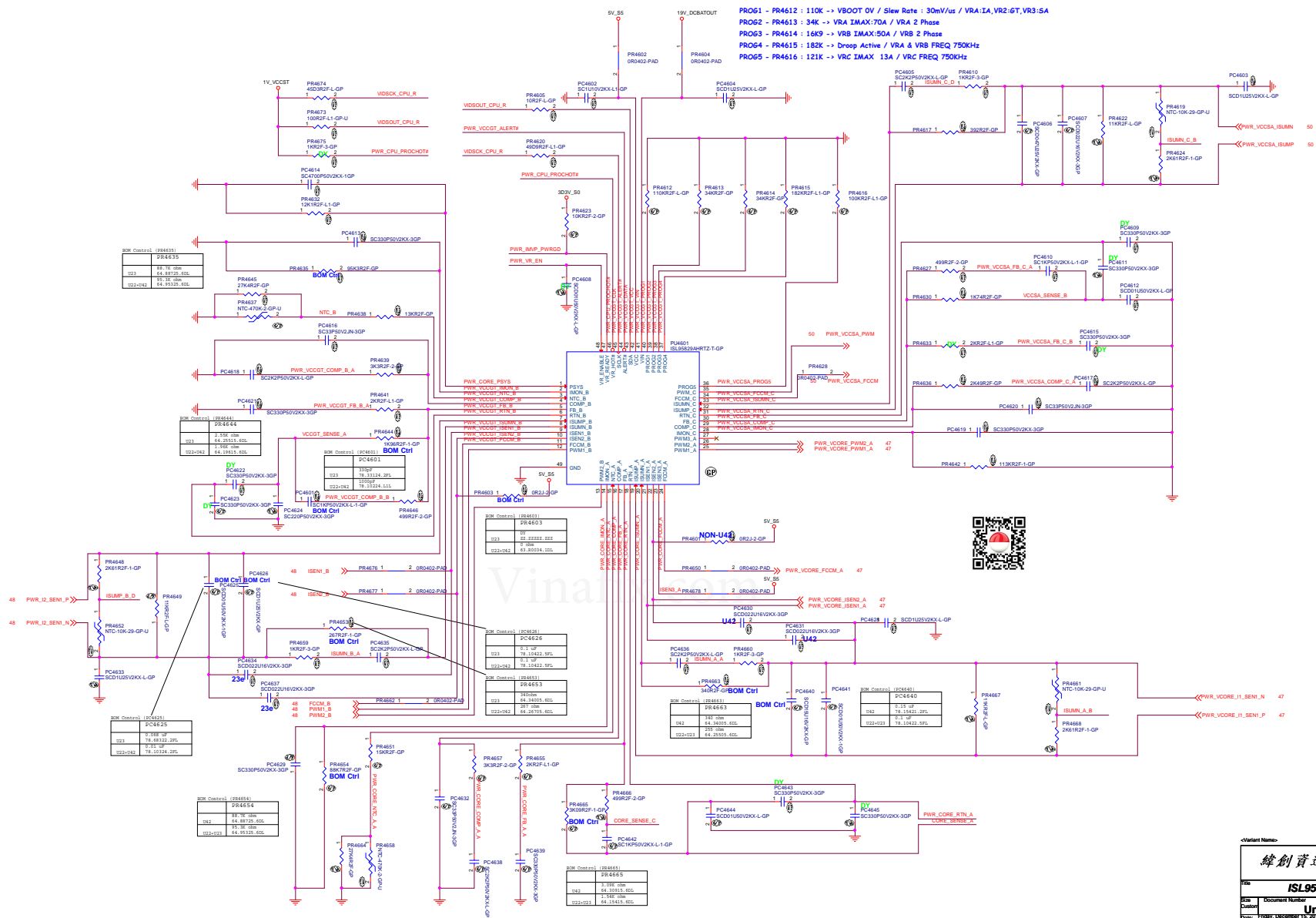
TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG PIN	RESISTANCE (Ω)	DEFAULT	DEFAULT	
MIN	MAX	BITSTREAM FREQUENCY	ACQ. TIME (μs)	
0	1	7.33MHz	No	0.476
8.65		7.33MHz	No	2.5
14.7		1MHz	No	2.5
21.0		1MHz	No	0.476
26.0		7.33MHz	Yes	0.476
35.7		7.33MHz	Yes	2.5
43.2	2	7.33MHz	Yes	2.5
52.3		7.33MHz	Yes	0.476
62.5		7.33MHz	No	2.5
62.9		1MHz	No	0.476
72.5		1MHz	No	2.5
82.5		7.33MHz	No	2.5
93.2		7.33MHz	No	0.476
106	3	7.33MHz	No	0.476
118		7.33MHz	No	2.5
130		1MHz	No	2.5
147		1MHz	No	0.476
162		7.33MHz	Yes	0.476
178		7.33MHz	Yes	2.5
196	4	7.33MHz	Yes	2.5
215		7.33MHz	Yes	0.476
237		1MHz	No	0.476
261		1MHz	No	2.5
287		7.33MHz	No	2.5
308		7.33MHz	No	0.476
348	1	7.33MHz	No	0.476

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 CHARGESENSE42M0727
 Unicorn LV530 KBL MS1500L



4	H_PROCHOT#	<<<	PR4656 1	2	PWR_CPU_PROCHOT#
7	SVD_ALERT#_CPU	<<<<	PR4608 1	2	PWR_VCCGT_ALERT#
7	SVD_CLK_CPU	<<<<	PR4621 1	2	VDSBCK_CPU_R
7	SVD_DATA_CPU	<<<<	PR4618 1	2	VDSOUT_CPU_B
40	VR_RDY	<<<<	PR4640 1	2	PWR_MVP_PWROD
40	VR_EN	<<<<	PR4641 1	2	PWR_VR_EN
7	VBS_SENSE	<<<<	PR4629 1	2	PWR_CORE_RTN_A
7	VCC_SENSE	<<<<	PR4671 1	2	CORE_SENSE_A
7	VCCGT_SENSE	<<<<	PR4606 1	2	VCCGT_SENSE_A
7	VBSGT_SENSE	<<<<	PR4607 1	2	PWR_VCCGT_RTN_B
7	VSSA_SENSE	<<<<	PR4629 1	2	PWR_VCCSA_RTN_C
7	VCCSA_SENSE	<<<<	PR4681 1	2	VCCSA_SENSE_B
44	PWR_CORE_PSYS	<<<<	PR4639 1	2	PWR_CORE_PSYS



PROG1 - PR4612 : 110K -> VBOOT 0V / Slew Rate : 30mV/us / VRA-1A,VR2-GT,VR3-5A
 PROG2 - PR4613 : 34K -> VRA IMAX:70A / VRA 2 Phase
 PROG3 - PR4614 : 16K9 -> VRB IMAX:50A / VRB 2 Phase
 PROG4 - PR4615 : 182K -> Droop Active / VRA & VRB FREQ 750KHz
 PROG5 - PR4616 : 121K -> VRC IMAX 13A / VRC FREQ 750KHz

BOM Callout: (284553)

Q1	81.76.026	PR4653
Q2	64.48775.05L	
Q3	91.16.026	
Q22-Q24	24.19127.05L	

BOM Callout: (284544)

Q1	81.76.026	PR4653
Q2	64.48775.05L	
Q3	91.16.026	
Q22-Q24	24.19127.05L	

BOM Callout: (284601)

Q1	81.76.026	PR4653
Q2	64.48775.05L	
Q3	91.16.026	
Q22-Q24	24.19127.05L	

BOM Callout: (284625)

Q1	81.76.026	PR4653
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Q3	91.16.026	
Q22-Q24	24.19127.05L	

BOM Callout: (284654)

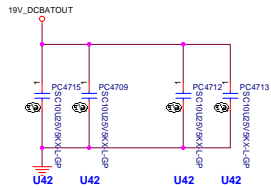
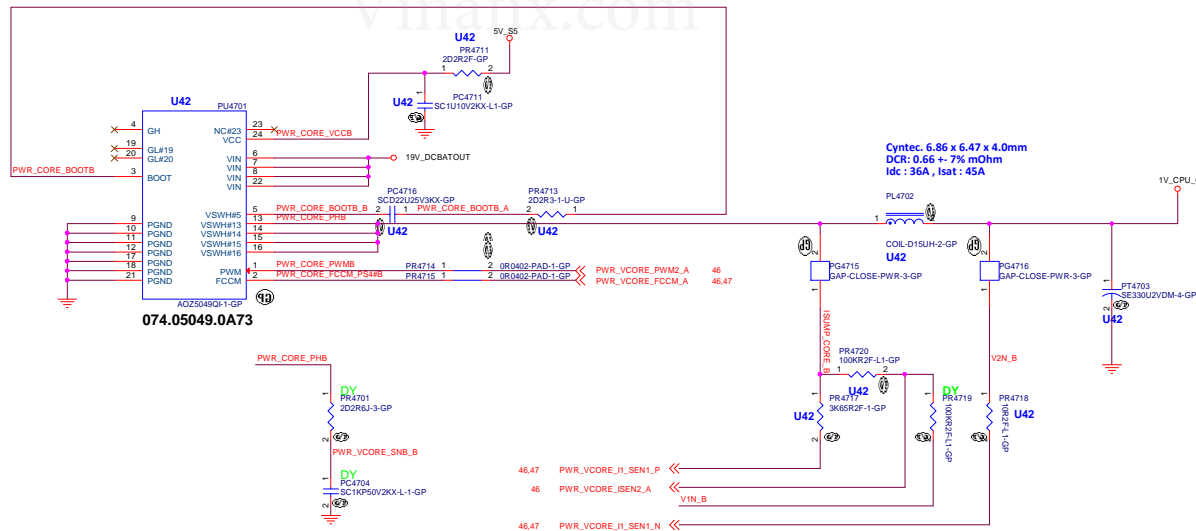
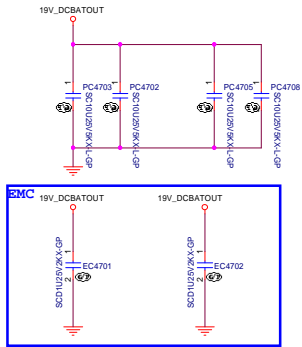
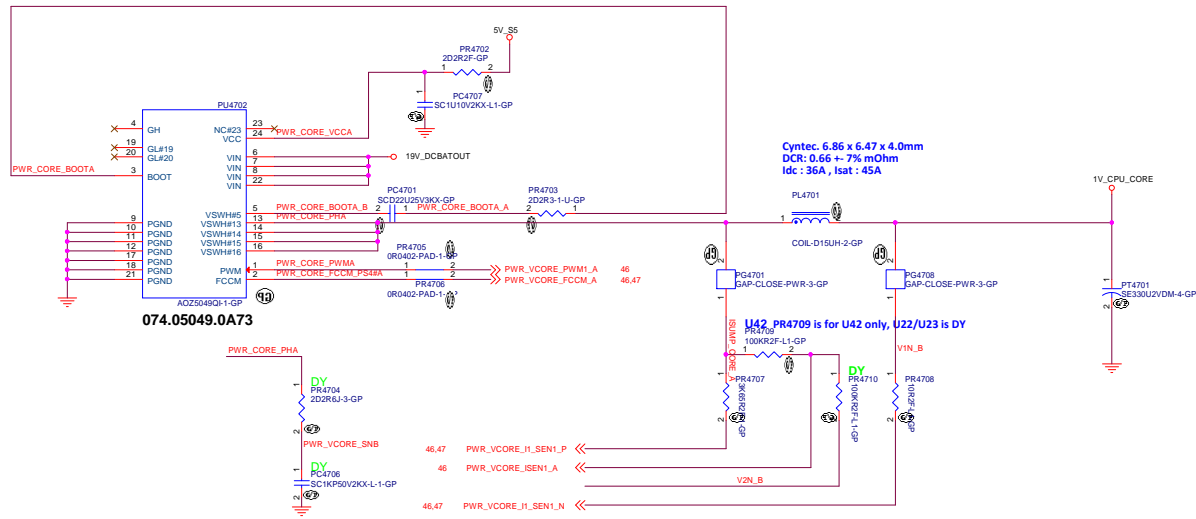
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Q2	64.48775.05L	
Q3	91.16.026	
Q22-Q24	24.19127.05L	

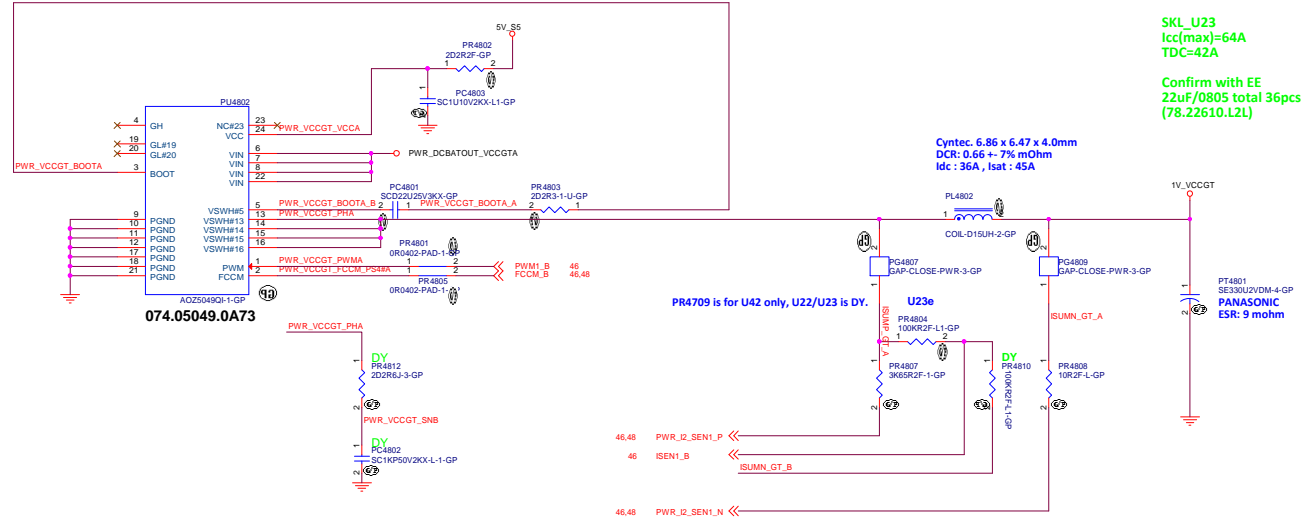
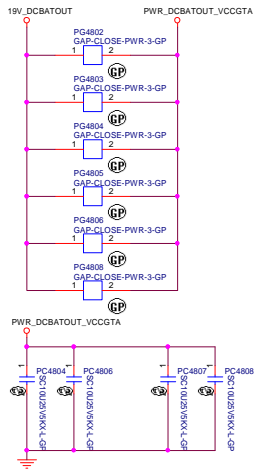
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Q2	64.48775.05L	
Q3	91.16.026	
Q22-Q24	24.19127.05L	

BOM Callout: (284655)

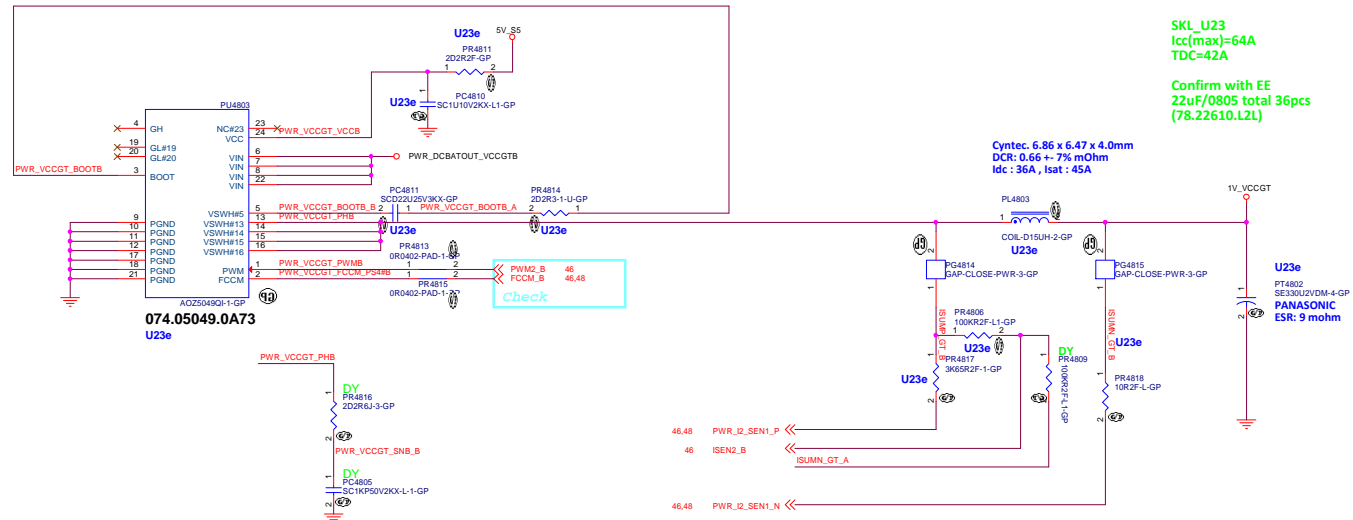
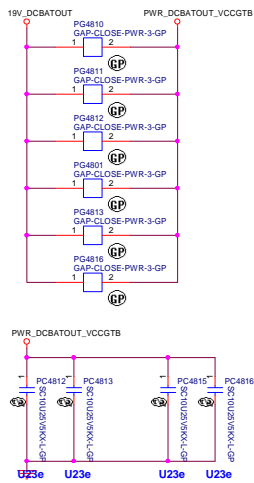
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Q2	64.48775.05L	
Q3	91.16.026	
Q22-Q24	24.19127.05L	





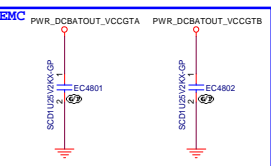
SKL_U23
Icc(max)=64A
TDC=42A

Confirm with EE
22uF/0805 total 36pcs
(78.22610.L2L)



SKL_U23
Icc(max)=64A
TDC=42A

Confirm with EE
22uF/0805 total 36pcs
(78.22610.L2L)



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<Variant Name>

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Title **CPU_VCCGTUS**

Size
A4

Document Number

Rev

Unicorn LV530 KBL MB GA

Date: Friday, December 15, 2017

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Main Func = CPU_CORE

20170417_modify by PWR

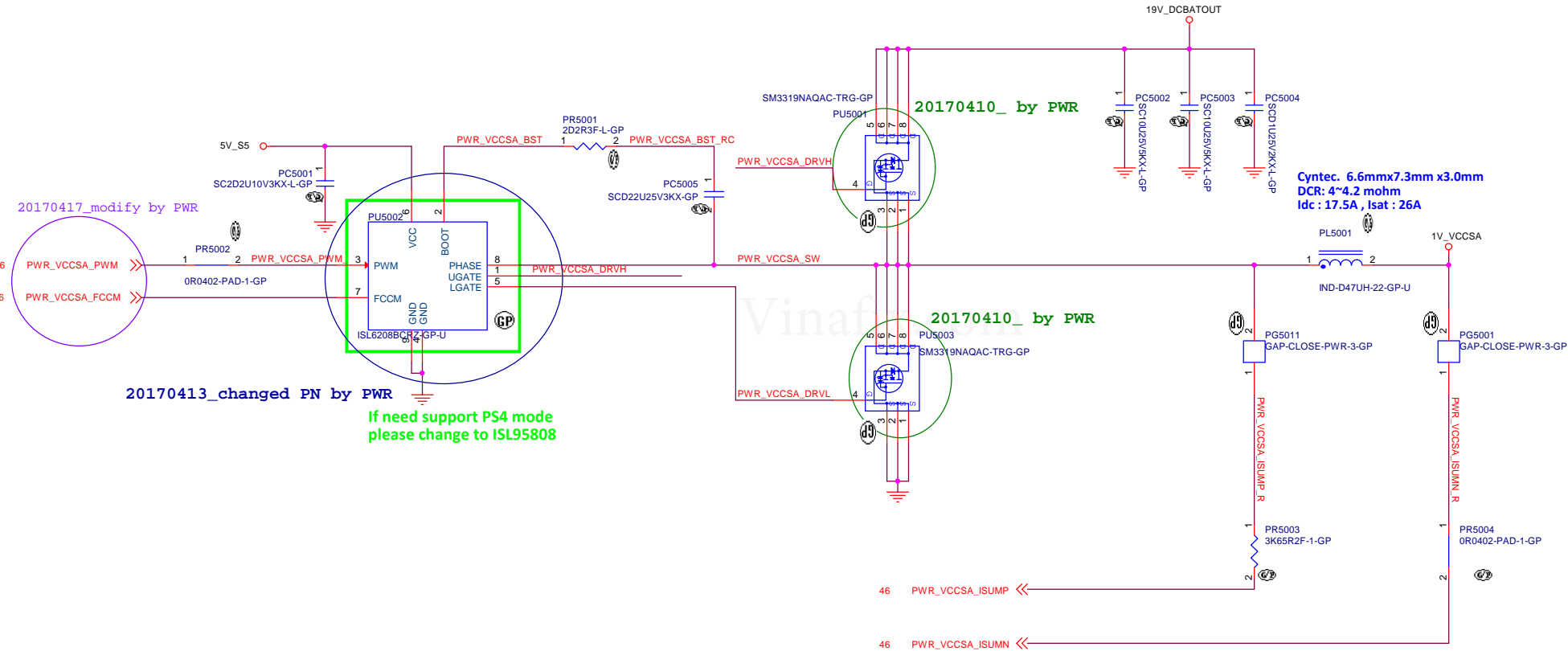
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If need support PS4 mode
please change to ISL95808

20170410_ by PWR

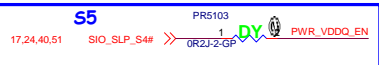
20170410_ by PWR

Cyntec. 6.6mmx7.3mm x3.0mm
DCR: 4~4.2 mohm
I_{dc}: 17.5A, Isat: 26A

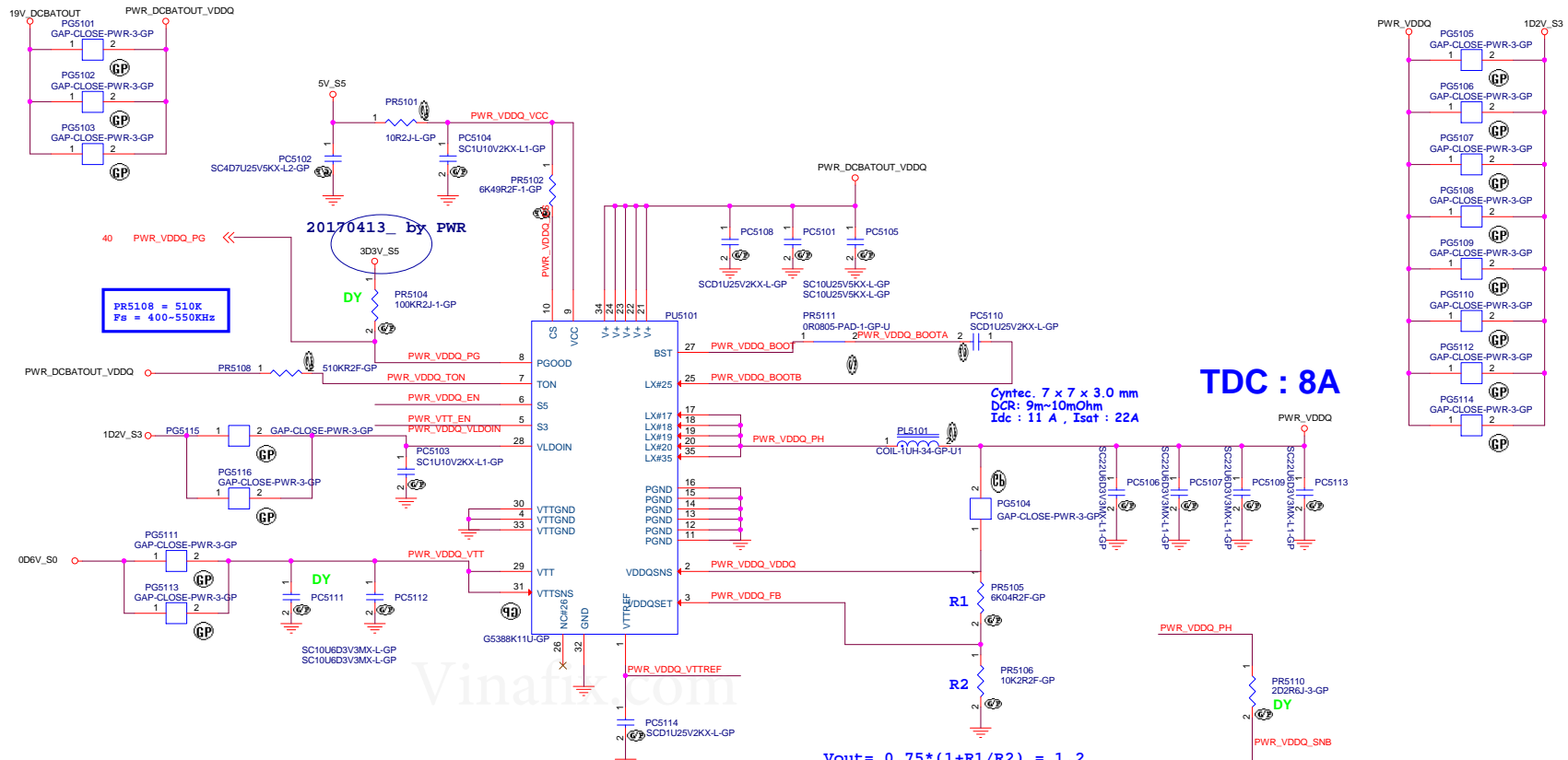
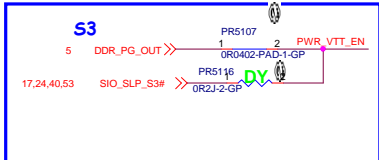


OFFPAGE

S5



S3



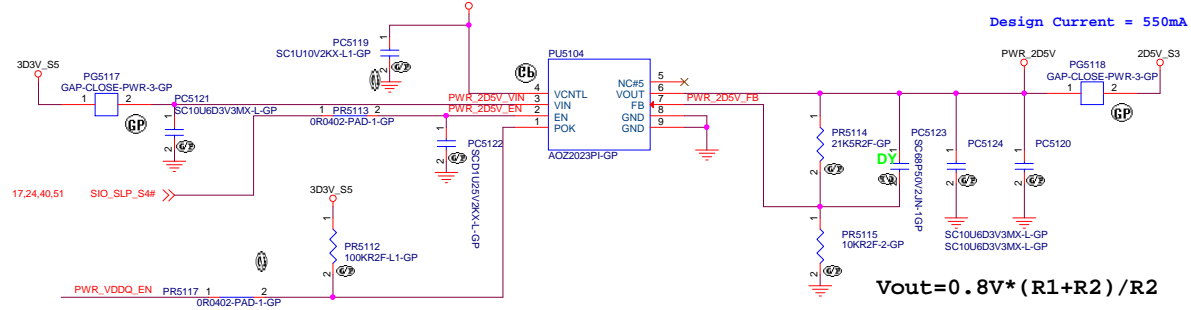
20170413 by PWR

PR5108 = 510K
Fs = 400-550KHz

TDC : 8A

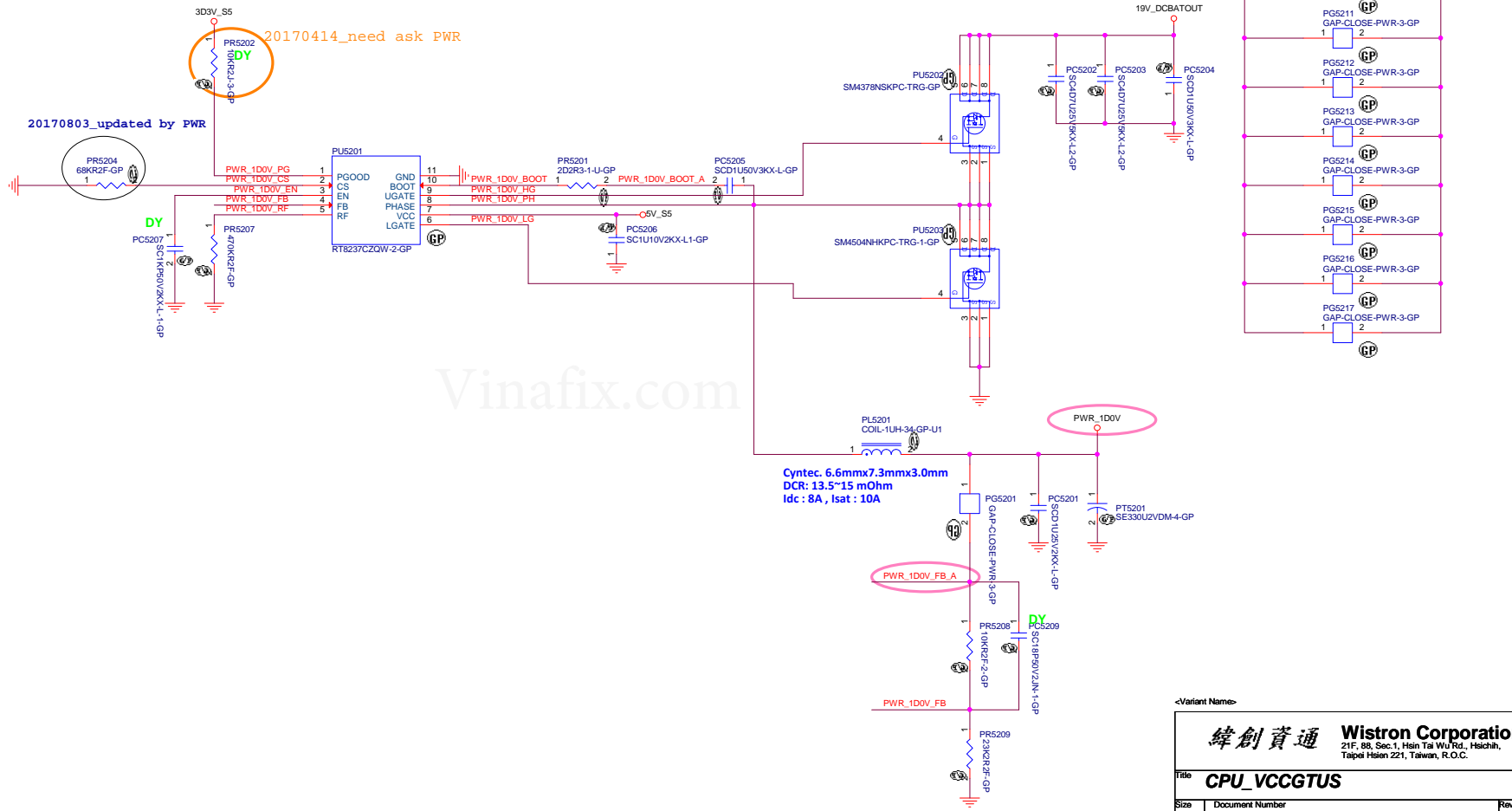
$$V_{out} = 0.75 * (1 + R1/R2) = 1.2$$

RT9025 for 2D5V



$$V_{out} = 0.8V * (R1 + R2) / R2$$

BOM1	
緯創資通 Wistron Corporation	
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Title G5388_VDDQ	
Size Custom	Document Number Unicorn LV530 KBL MB14A
Date: Friday, December 15, 2017	Rev 105
Sheet 51	of 105



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<Variant Name>

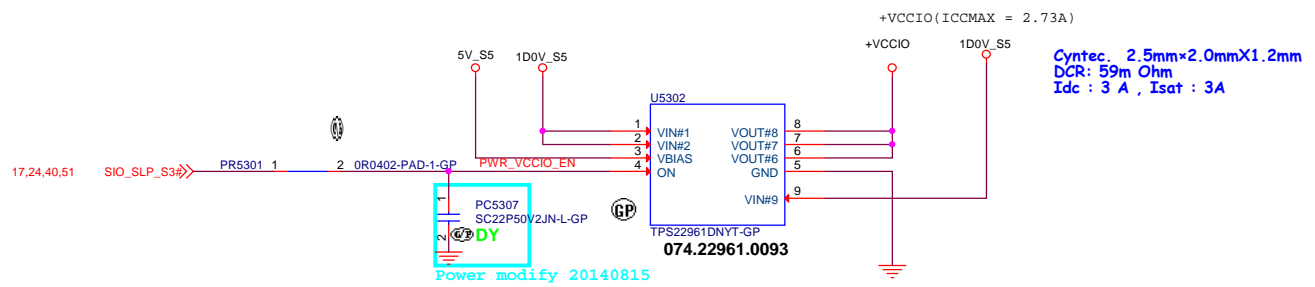
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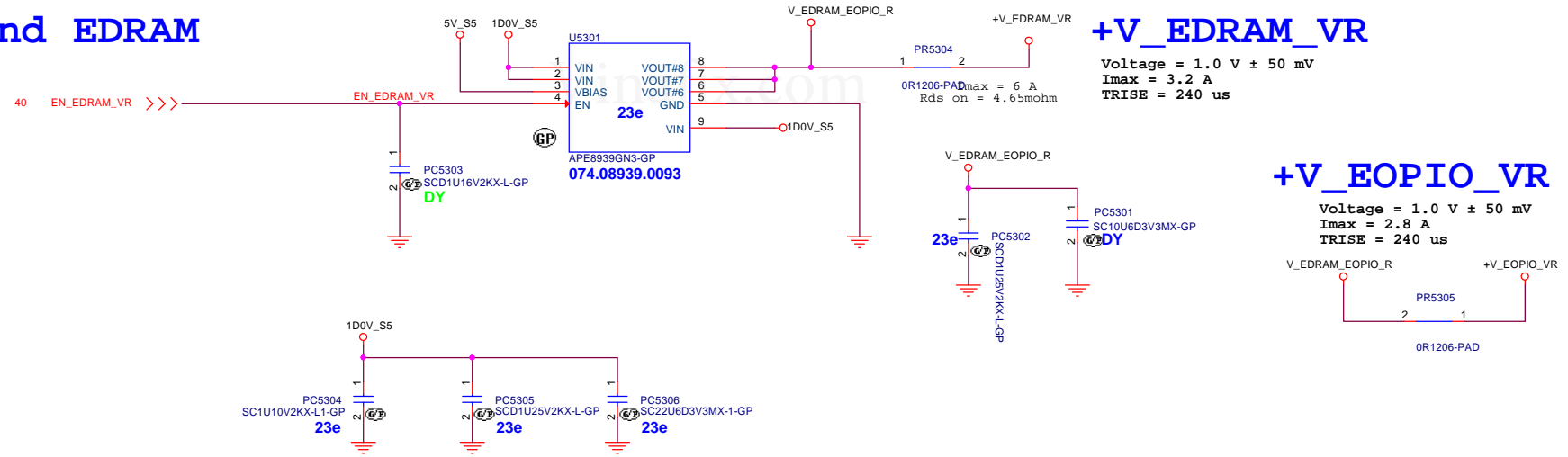
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Date: Friday, December 15, 2017 Sheet 52 of 105

VCCIO



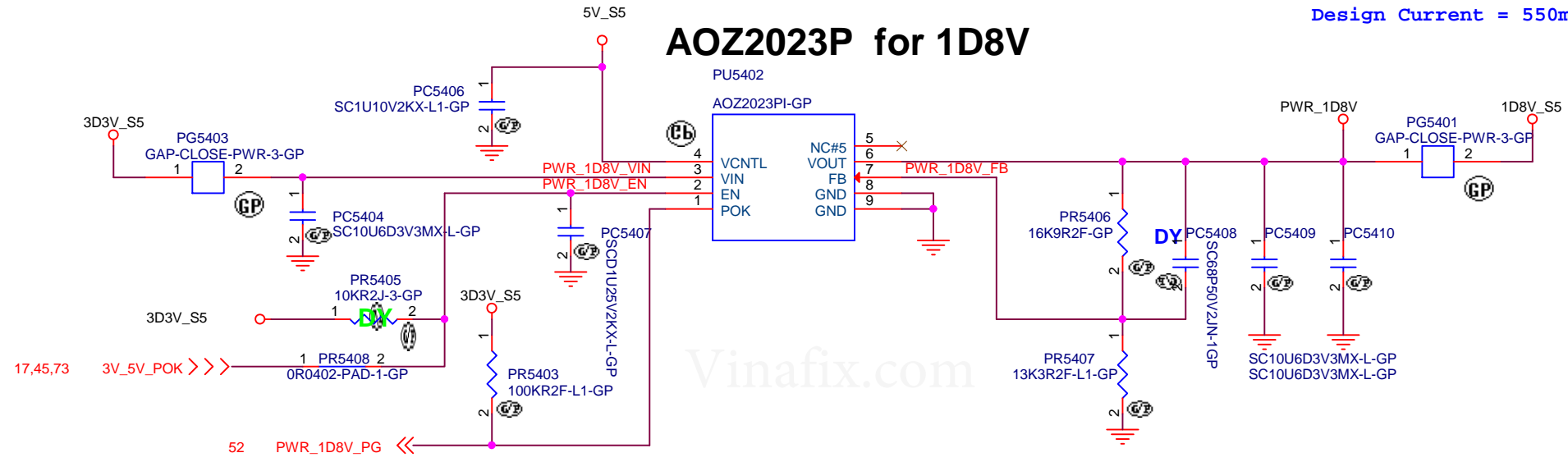
EOPIO and EDRAM



Main Func = 1D8V

Design Current = 550mA

AOZ2023P for 1D8V



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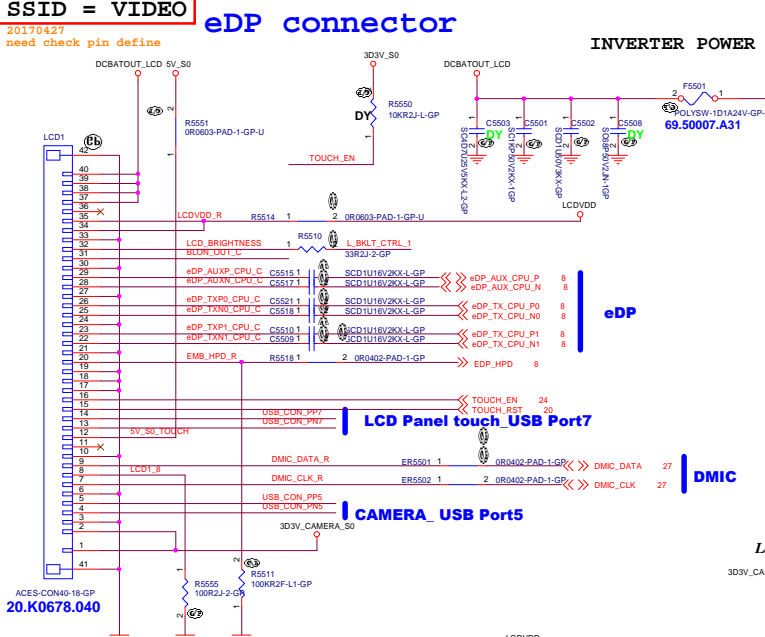
$$V_{out} = 0.8V * (R1 + R2) / R2$$

<Variant Name>

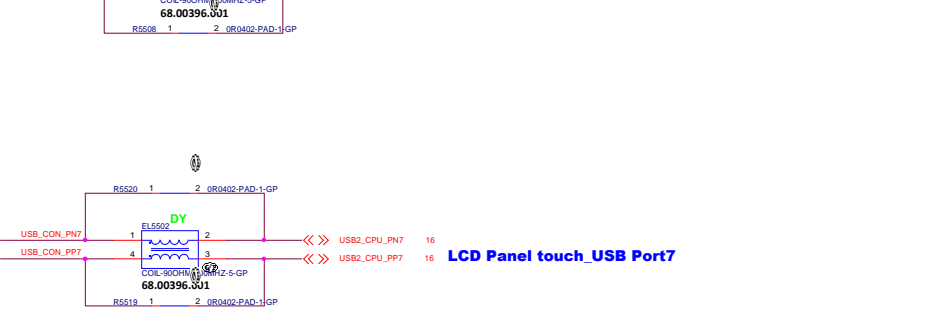
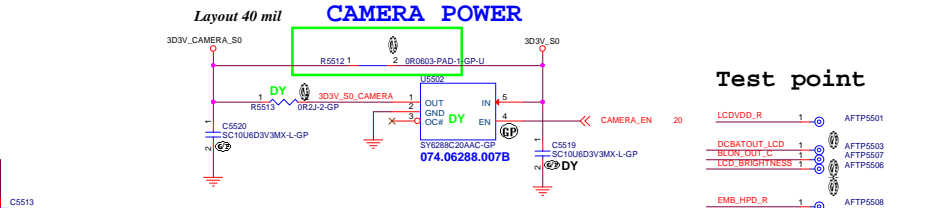
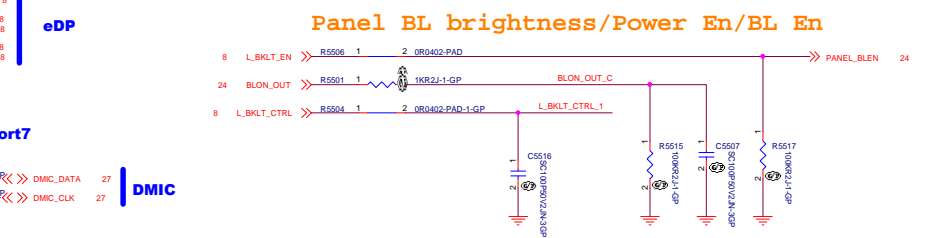
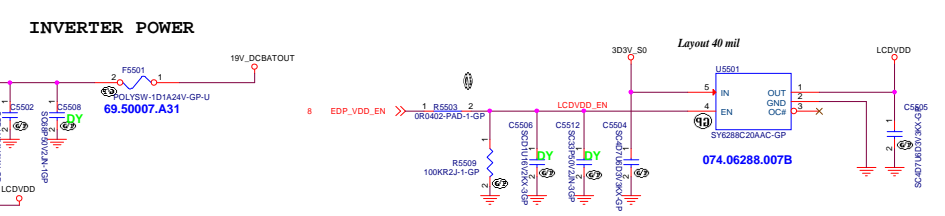
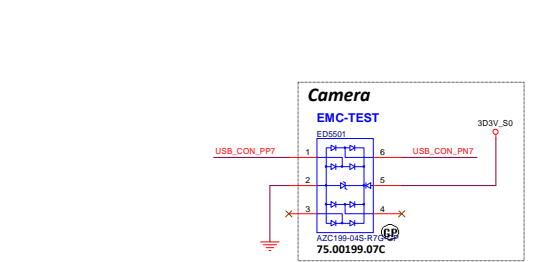
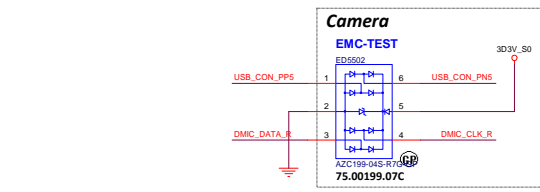
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Title		
RT9025 1D8V		
Size	Document Number	Rev
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SSID = VIDEO
 20170427
 need check pin define



2) 3 empty-pins between wire cable(MIC, camera, or other control signals) & coaxial cable(LCD panel usage). (Apply to LNB only)



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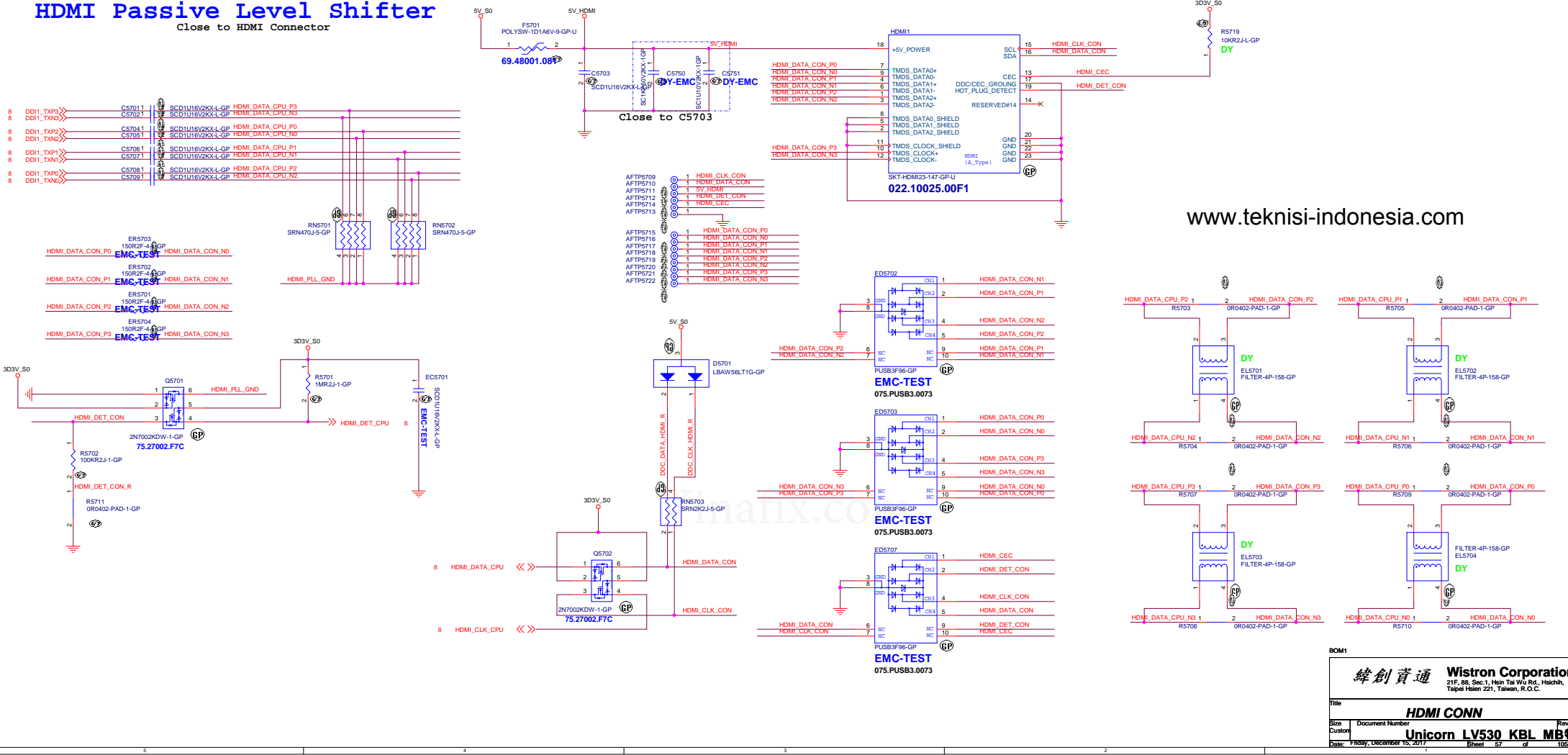
Shark Bay SV

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Title			
ODD(Reserved)			
Size	Document Number	Rev	
A3		Unicorn LV530 KBL MB13A	
Date:	Friday, December 15, 2017	Sheet	56 of 105

HDMI CONNECTOR

HDMI Passive Level Shifter

Close to HDMI Connector



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BOM1

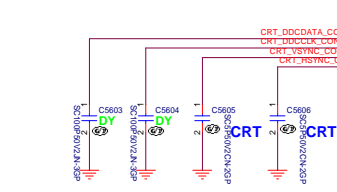
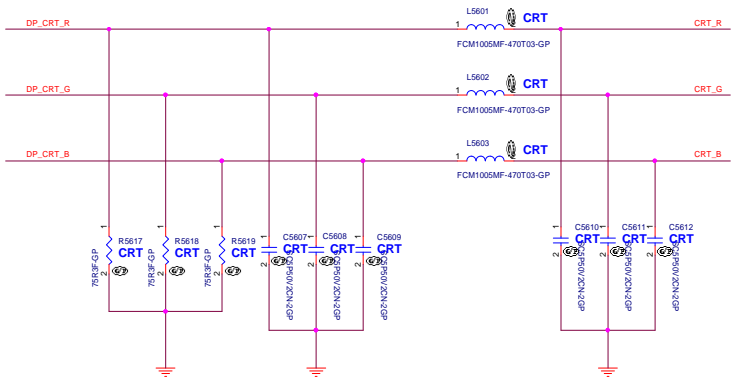
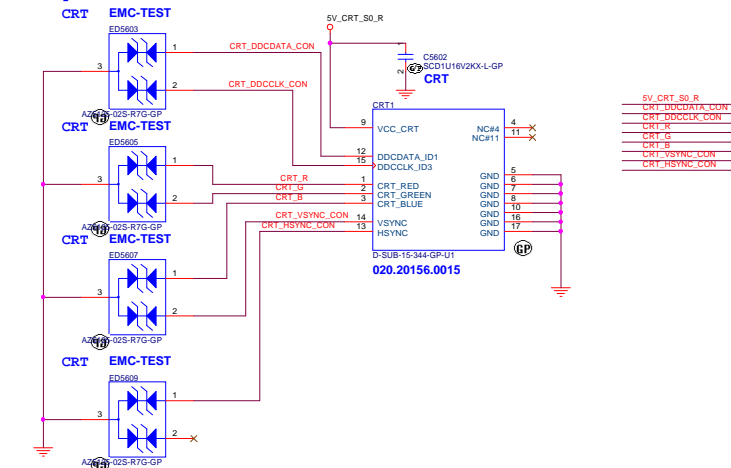
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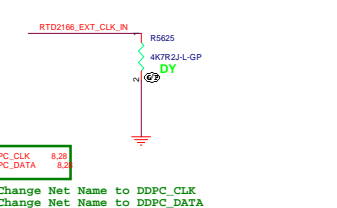
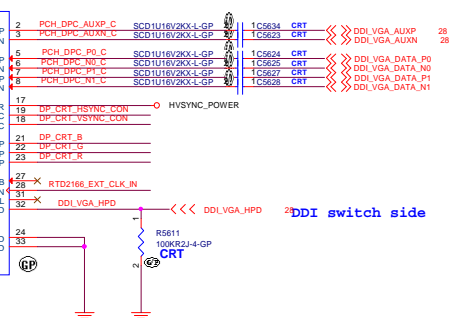
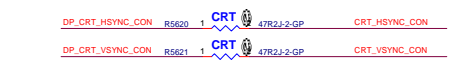
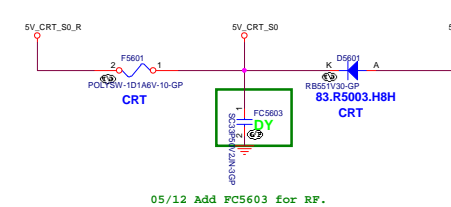
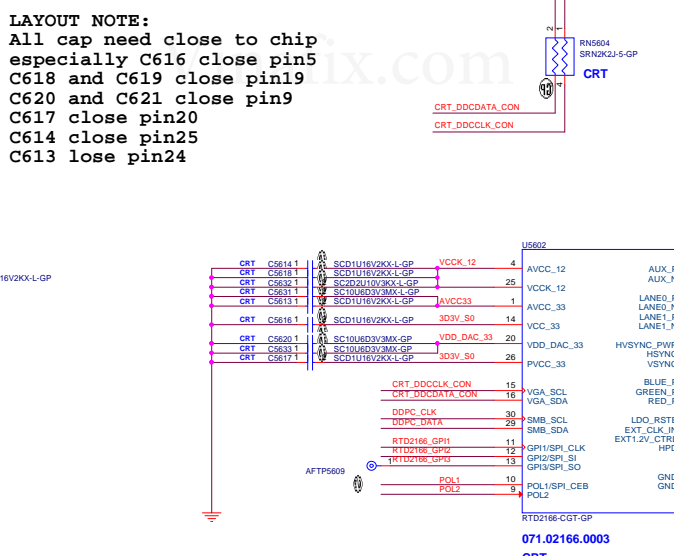
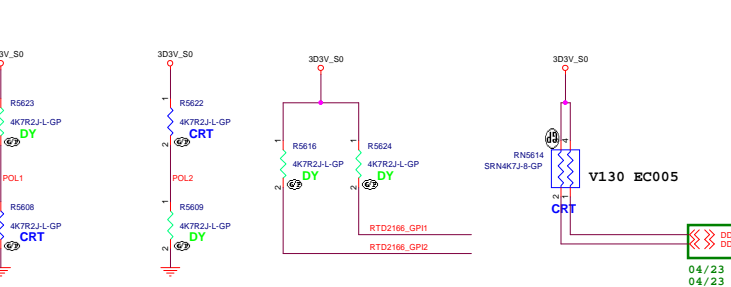
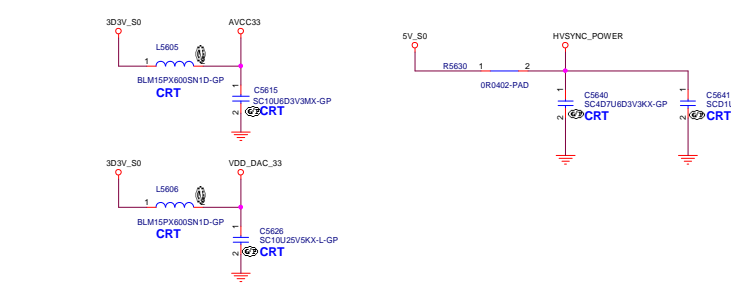
Size: Document Number: **Unicorn LV530 KBL MB4** Rev: **1**

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EMI Request



LAYOUT NOTE:
 All cap need close to chip
 especially C616 close pin5
 C618 and C619 close pin19
 C620 and C621 close pin9
 C617 close pin20
 C614 close pin25
 C613 lose pin24



DDI switch side

DDI_VGA_HPD

(Blank)

BOM1

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Title

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Size
A4

Document Number

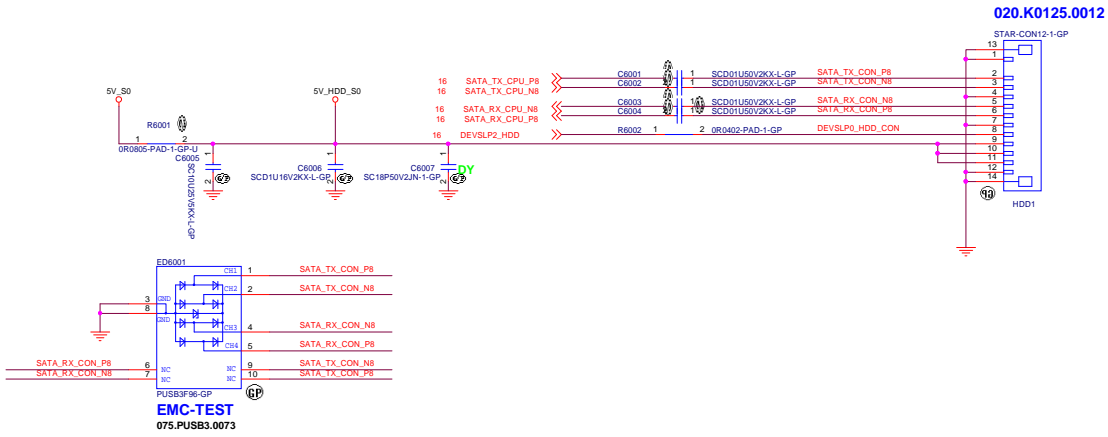
Unicorn LV530 KBL MB SA

Rev

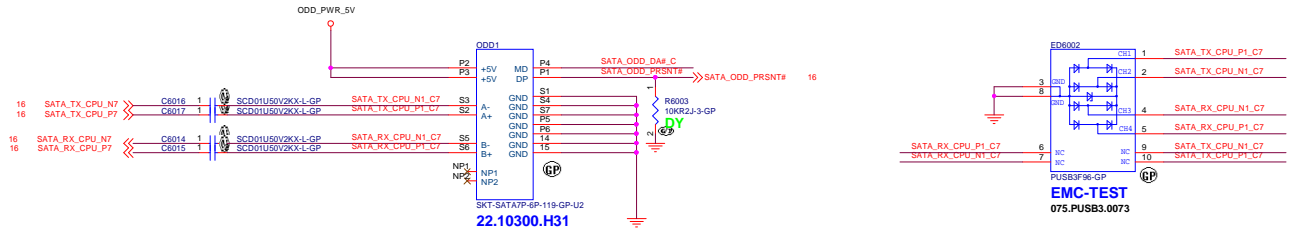
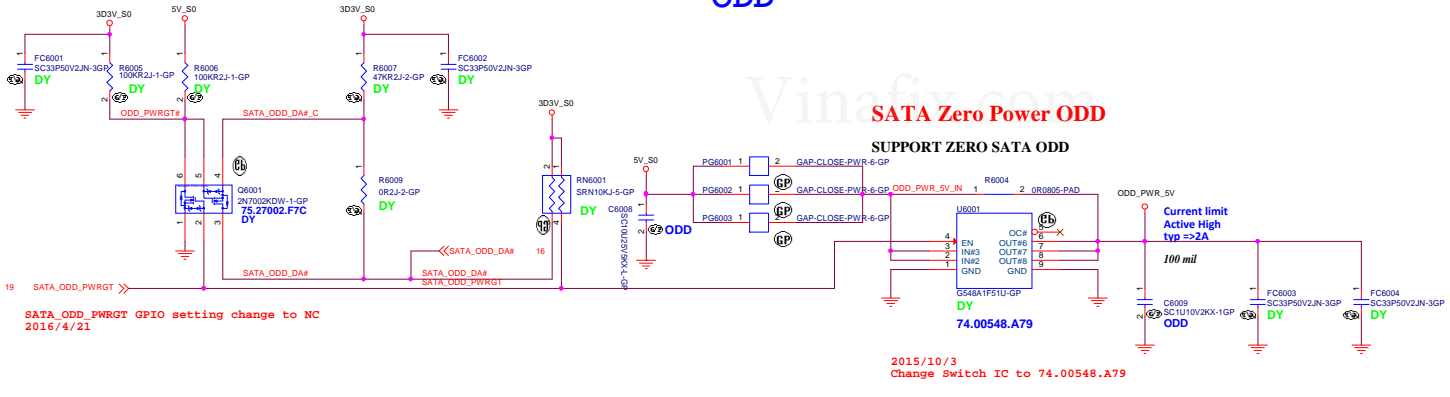
Date: Friday, December 15, 2017

Sheet 59 of 105

HDD 20170427
 Cnhange pin define follow LV315ST(NC) but pn 1 different

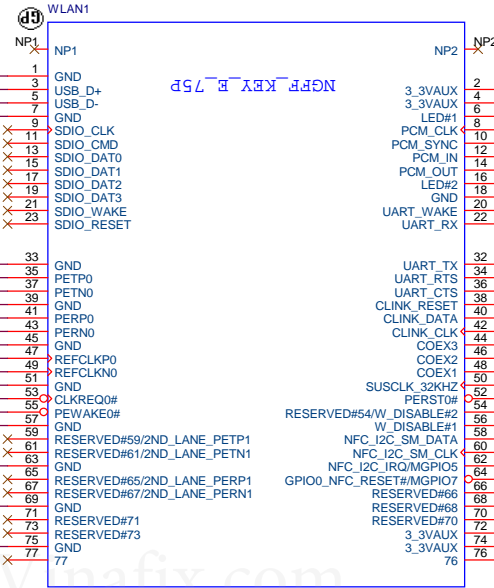
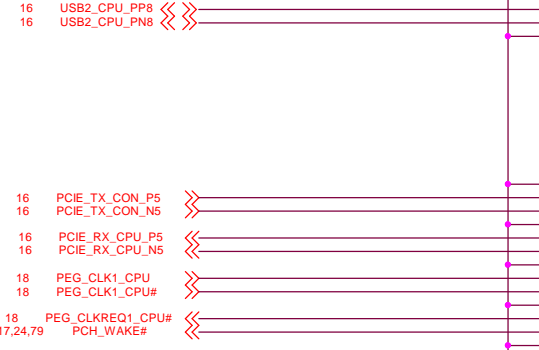
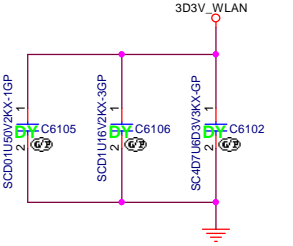
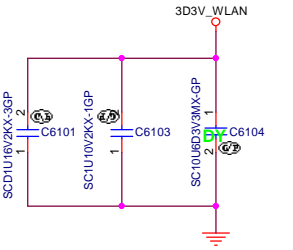
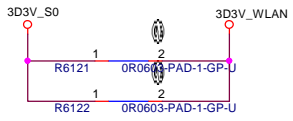


ODD
 SATA Zero Power ODD
 SUPPORT ZERO SATA ODD

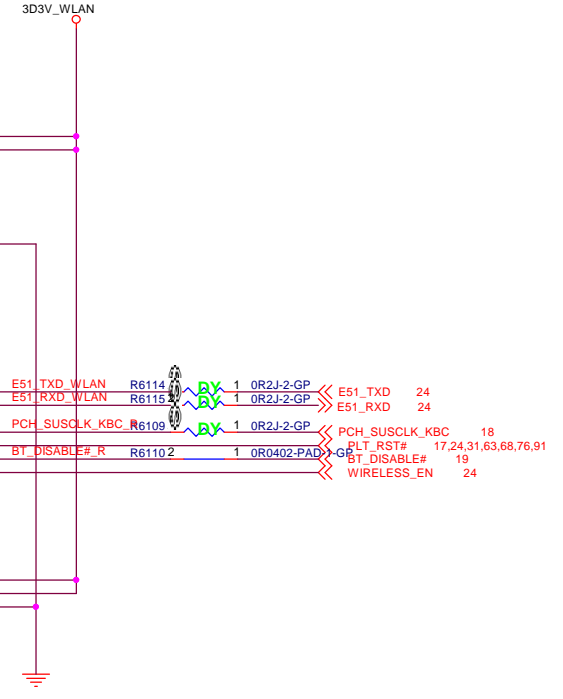


M.2 Key-E FOR WLAN / BT

2.5A peak
1.1A Cont



SKT-MINI67P-2-GP-U
62.10043.I91



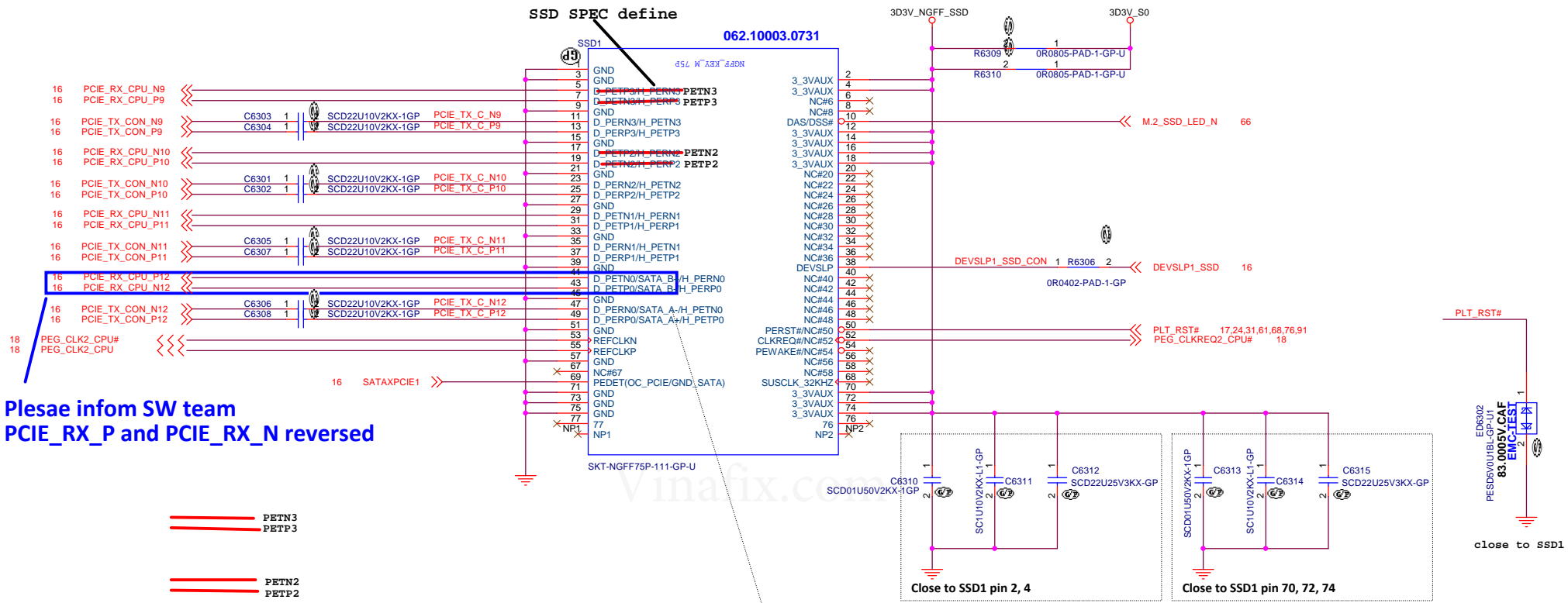
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Vinafix.com

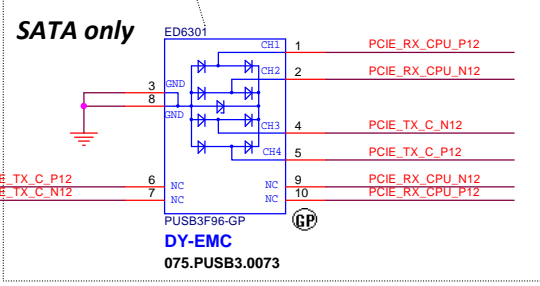
BOM1

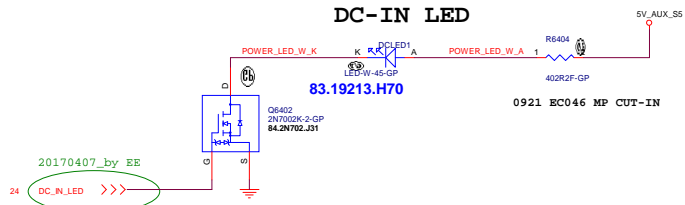
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
RESERVED		
Size A4	Document Number	Rev
Unicorn LV530 KBL MB GA		
Date: Friday, December 15, 2017	Sheet 62	of 105

Main Func = SSD TYPE-M NGFF CARD FOR PCIE SSD/Optane

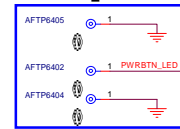


Please inform SW team
PCIE_RX_P and PCIE_RX_N reversed

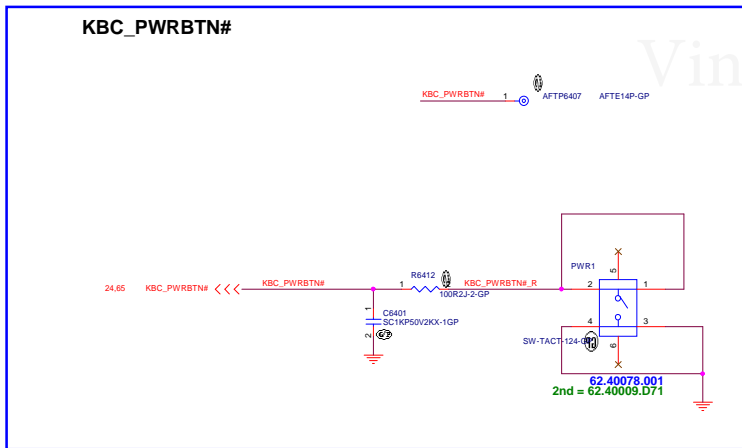
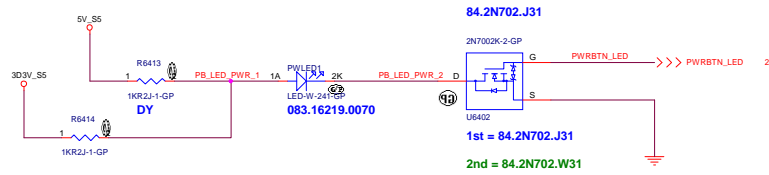




Test point



POWER BTN LED

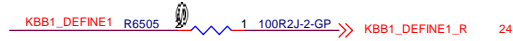
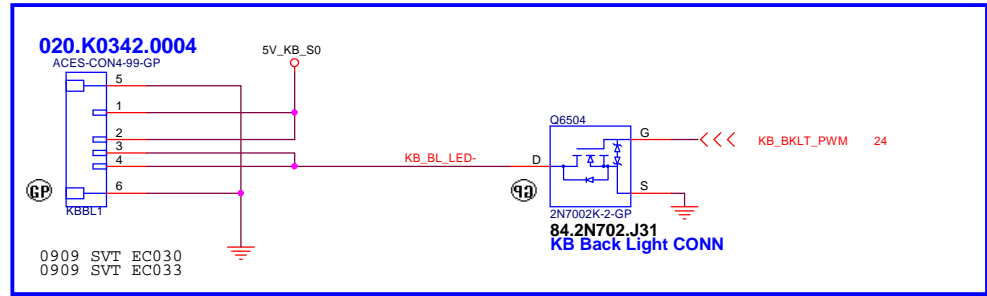
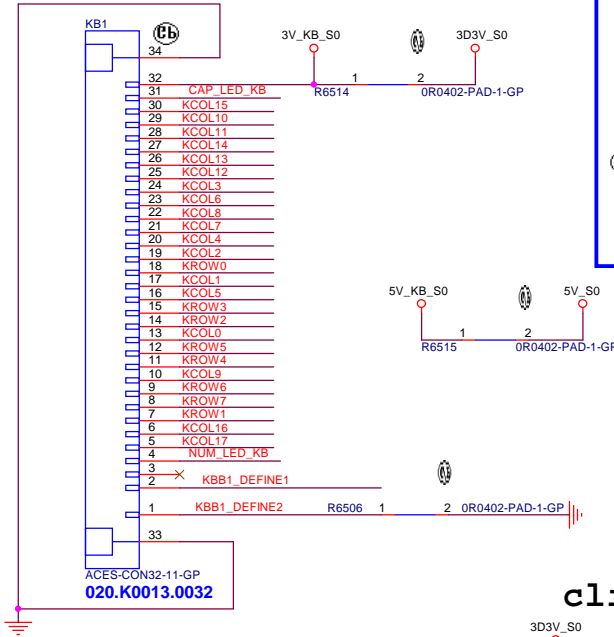
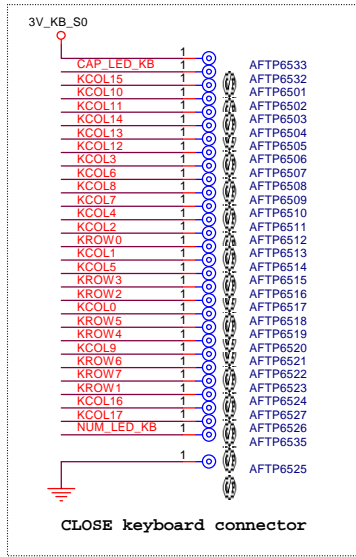


SSID = Touch.Pad

20170427_pin deifne check by Dennis

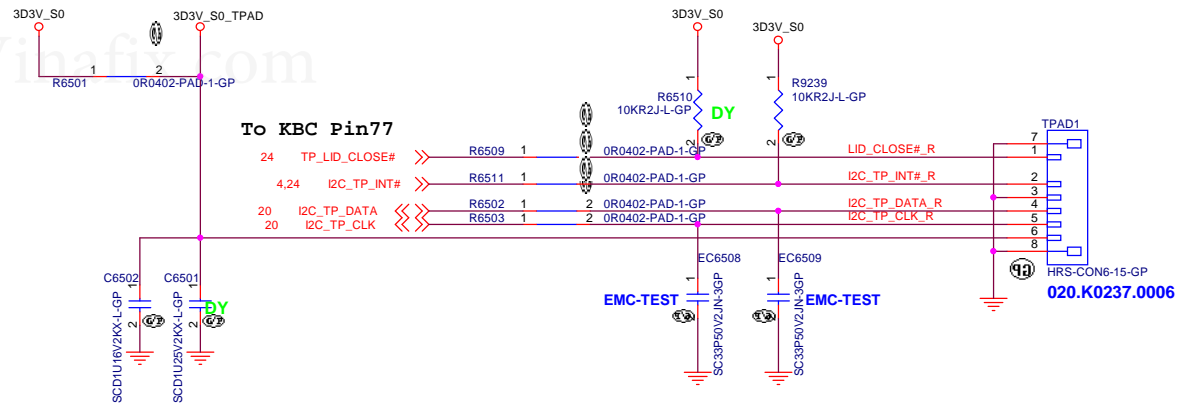
KB_LED

<<< KROW[0..7] 24
 >>> KCOL[0..17] 24

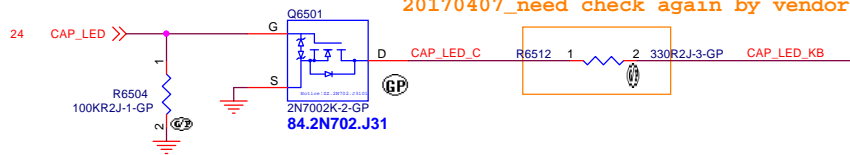


20170421
Change pin define by Dennis

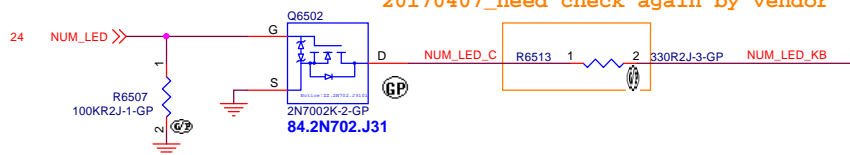
click pad



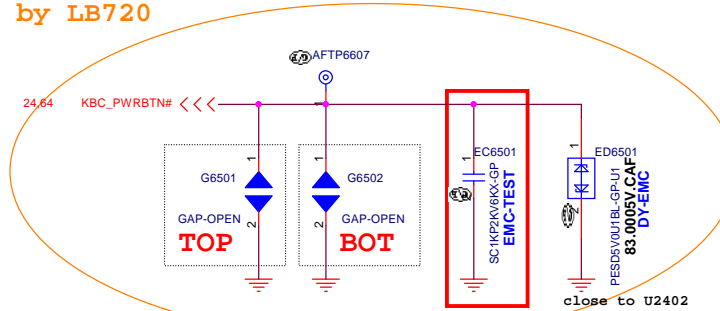
20170407_need check again by vendor



20170407_need check again by vendor



20170412_WKS test by LB720



BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

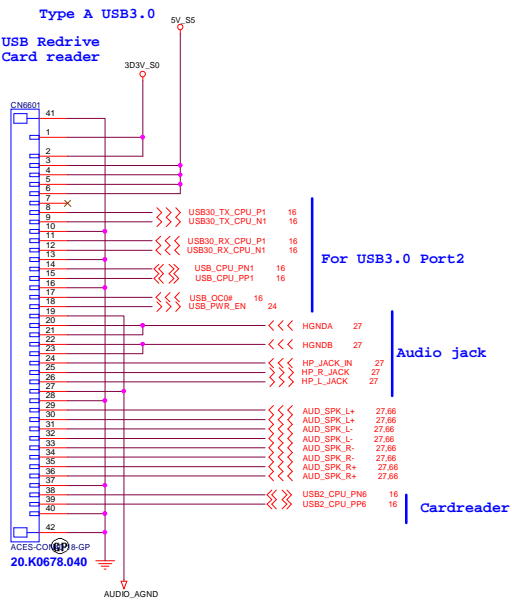
Title: **KEYBOARD/TOUCH PAD**

Size A3 Document Number: **Unicorn LV530 KBL MB14** Rev: **SA**

Date: Friday, December 15, 2017 Sheet 65 of 105

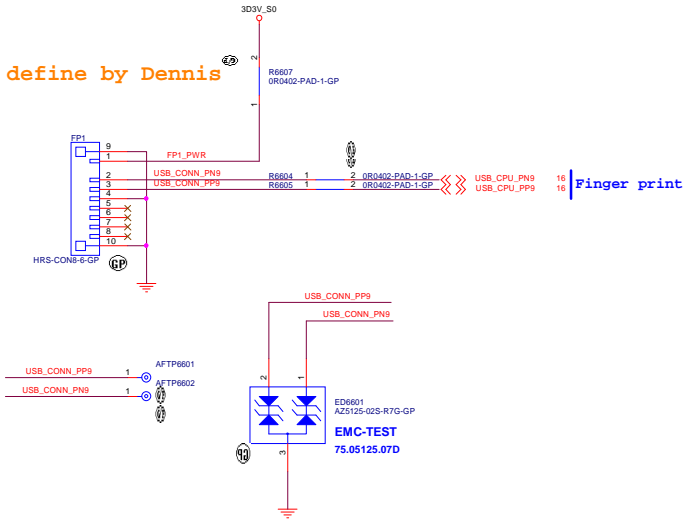
IO CONN

Type A USB3.0
USB Redrive
Card reader

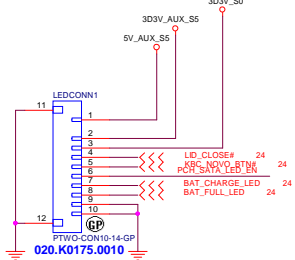


20170421
Change pin define by Dennis

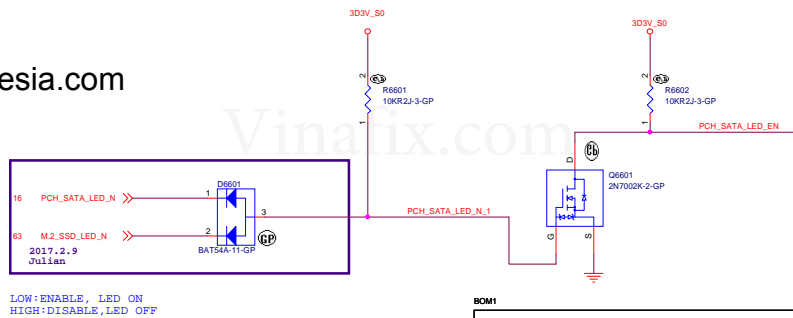
Finger print



LED IO CONN



www.teknisi-indonesia.com



BOM1

Wistron Corporation 2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsuehshien, Taipei Hsien 221, Taiwan, R.O.C.	
Title: LEDIO IO BOARD CONN	
Size: A2	Document Number: Unicom_LV530_KBL_MB14
Date: Friday, December 15, 2017	Rev: SA
Sheet: 66 of 105	

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BOM1

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size
A4

Document Number

Unicorn LV530 KBL MB SA

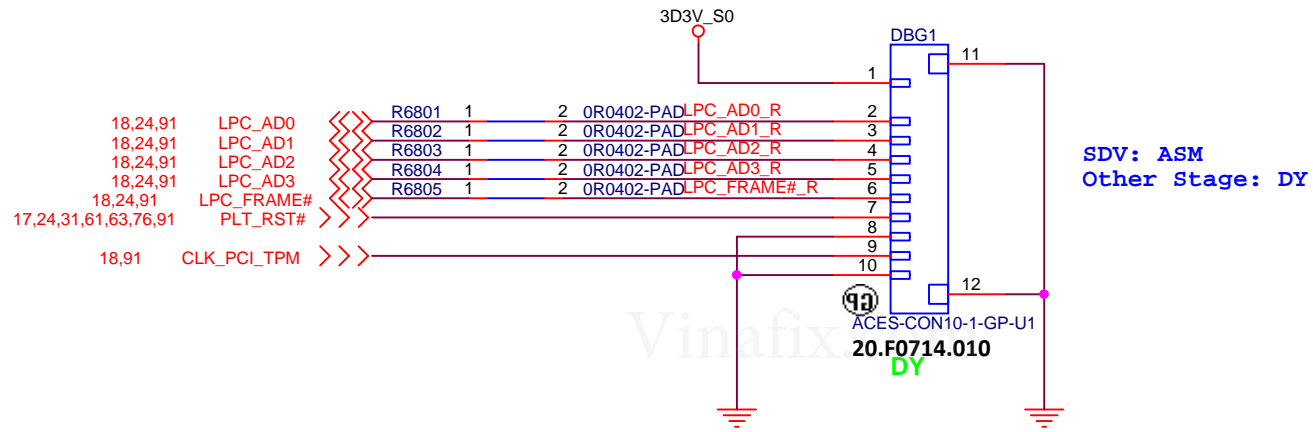
Rev

Date: Friday, December 15, 2017

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Main Func = Debug

Debug Connector

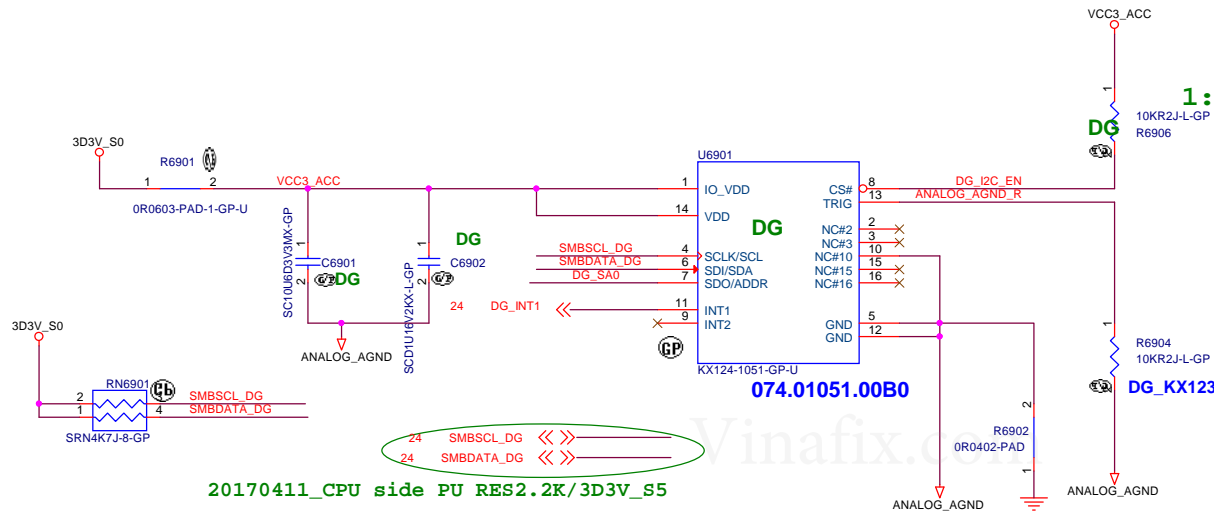


BOM1

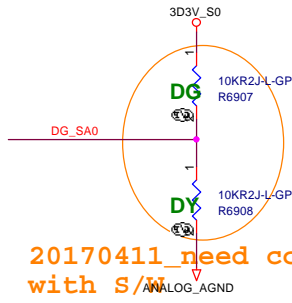
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DEBUG CONN			
Size	Document Number		Rev
A4	Unicorn_LV530_KBL_MB14		SA
Date:	Friday, December 15, 2017	Sheet	68 of 105

G-Sensor

1st: ST/ LIS3DETR, 74.00003.BB0
 (cannot be used, bit not enough)
 2nd: KX124-1051, 074.01051.00B0



1: I2C communication enable



20170411 need confirm address with S/A

20170411_CPU side PU RES2.2K/3D3V_S5

(Blank)

BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size
A4

Document Number

Unicorn LV530 KBL MB SA

Rev

Date: Friday, December 15, 2017

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BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
RESERVED			
Size	Document Number	Rev	
A4			
Date: Friday, December 15, 2017		Sheet 71	of 105

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BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size
A4

Document Number

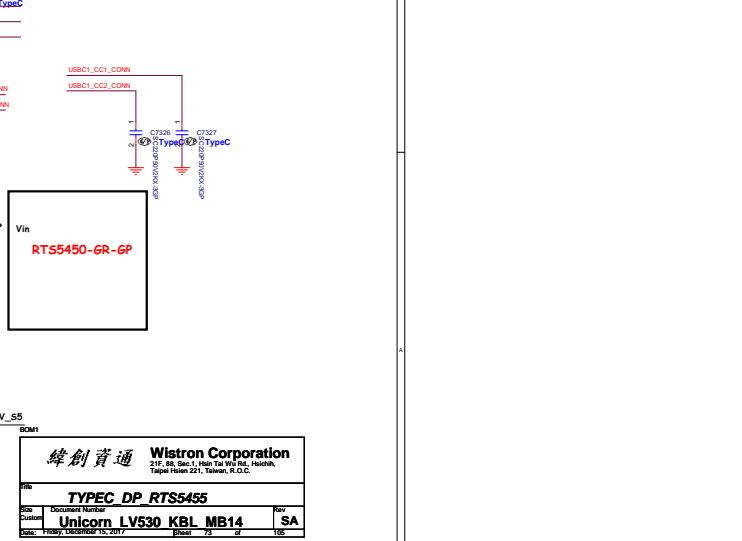
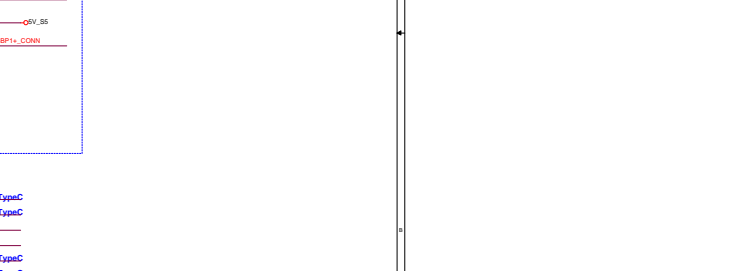
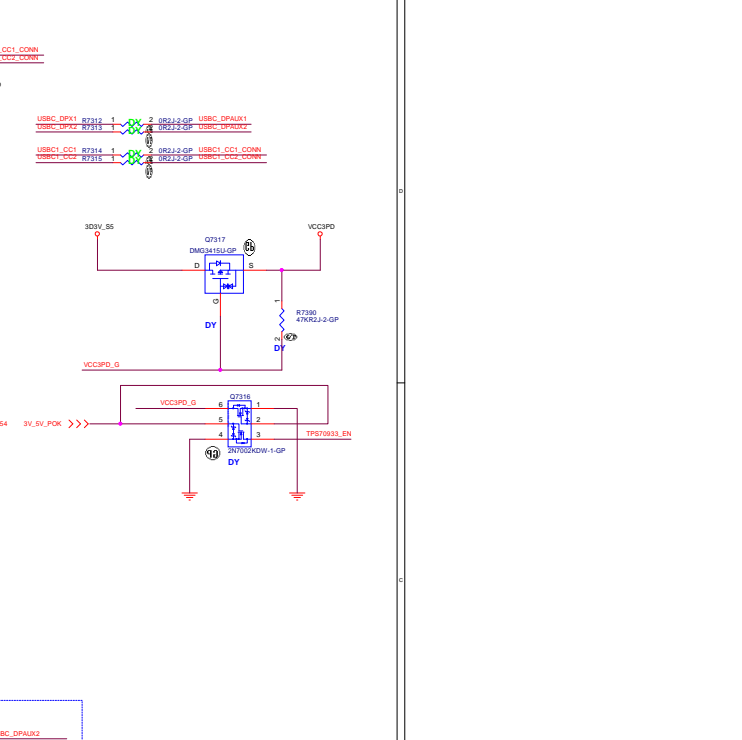
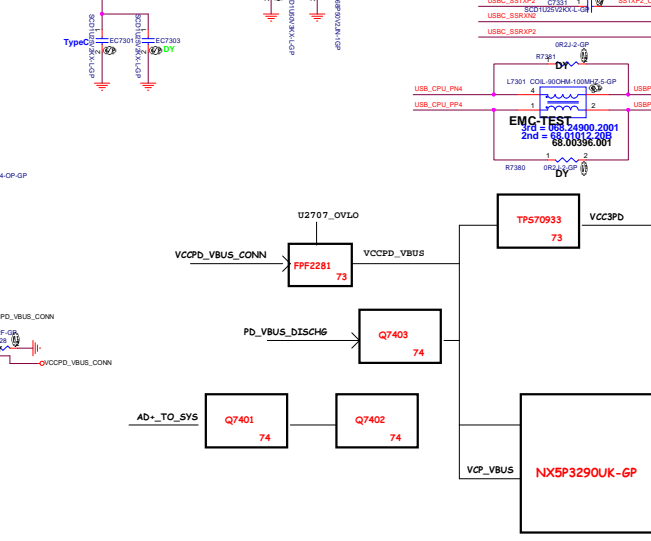
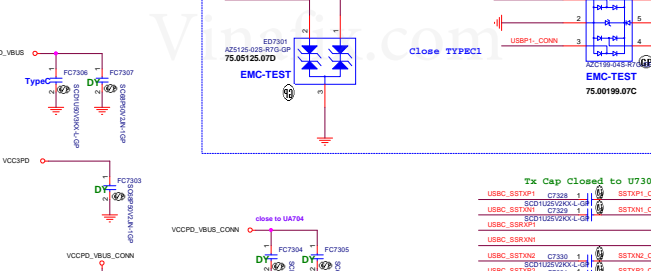
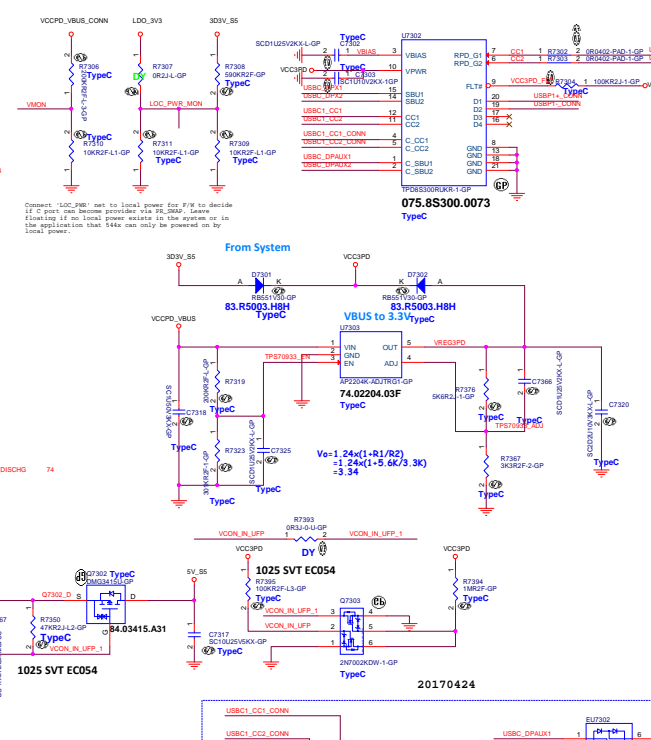
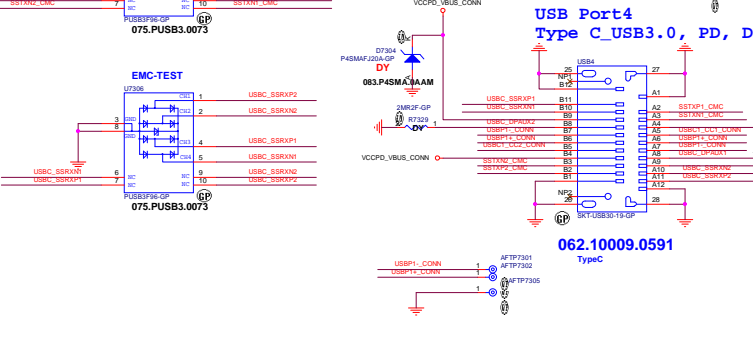
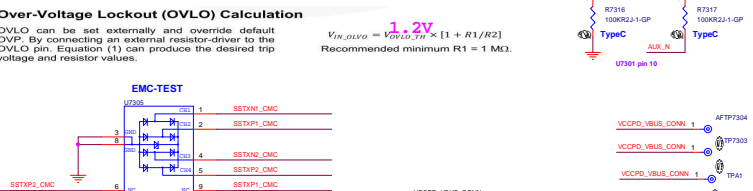
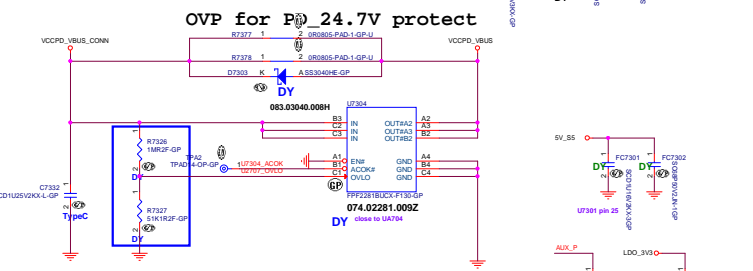
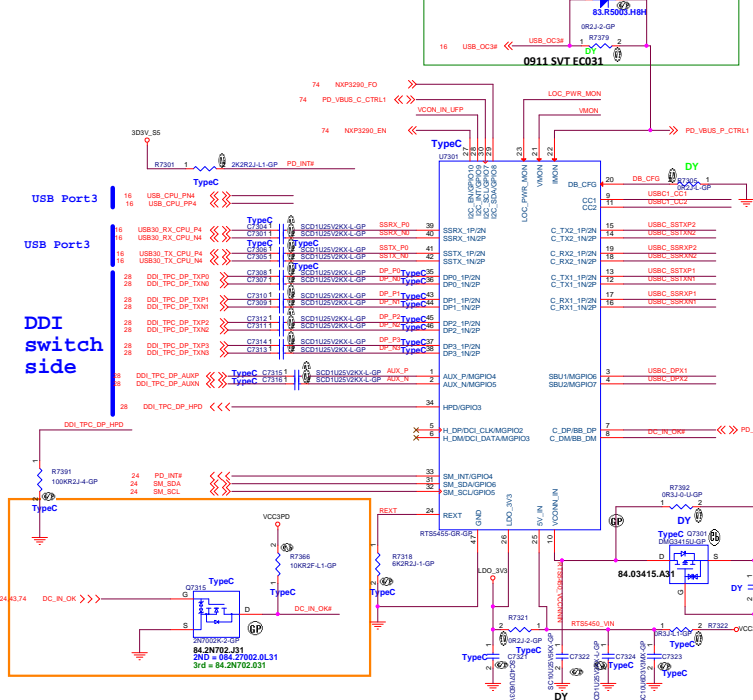
Unicorn LV530 KBL MB GA

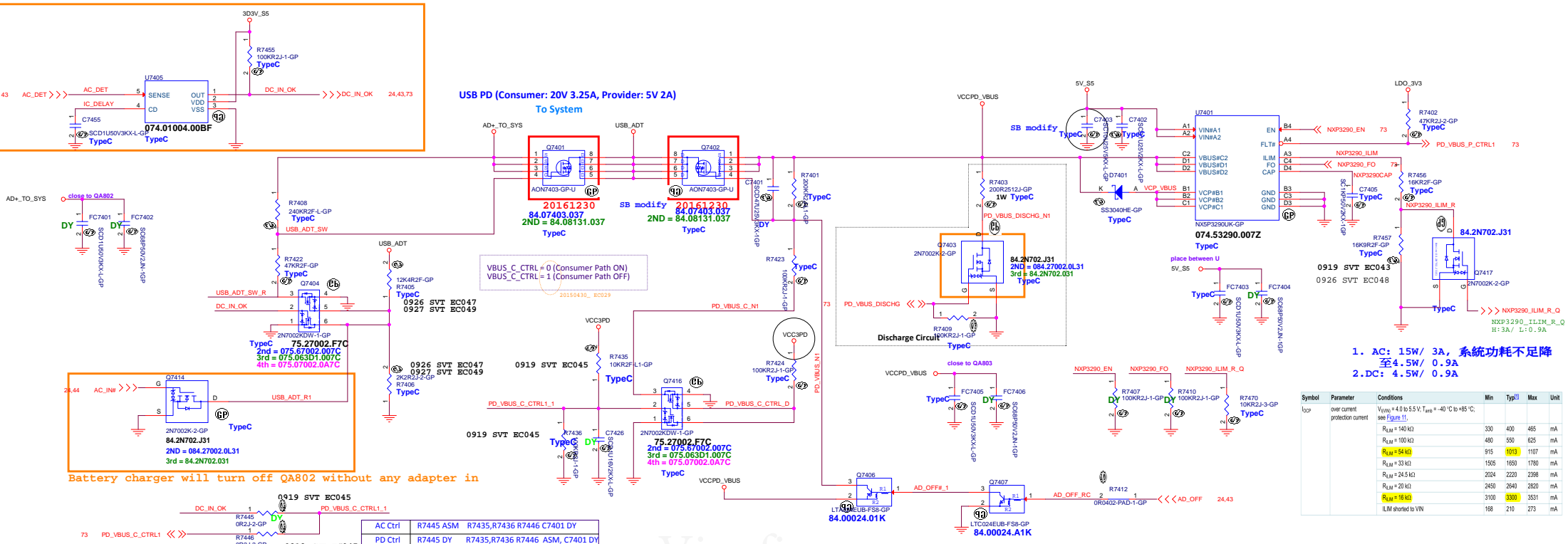
Rev

Date: Friday, December 15, 2017

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USB Port4, Type C_USB3.0, PD, DP



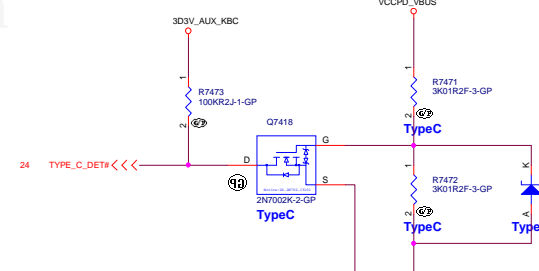


Battery charger will turn off QA802 without any adapter in

1. AC: 15W/ 3A, 系統功耗不足降 至 4.5W/ 0.9A
2. DC: 4.5W/ 0.9A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
locr	over current protection current	V _{IN} = 4.0 to 5.5V, T _{amb} = -40 °C to +85 °C, see Figure 15				
	R _{ILIM} = 140kΩ		330	400	465	mA
	R _{ILIM} = 100kΩ		480	550	625	mA
	R _{ILIM} = 50kΩ		915	1035	1107	mA
	R _{ILIM} = 33kΩ		1595	1650	1760	mA
	R _{ILIM} = 24.5kΩ		2024	2220	2398	mA
	R _{ILIM} = 20kΩ		2450	2640	2820	mA
	R _{ILIM} = 15kΩ		3100	3300	3531	mA
	ILIM shorted to VIN		168	210	273	mA

19V Power source type	Control Pin				PMOS Location	Status	Remark
	Net name	Status	Net name	Status			
Normal adapter Only	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	Control by DC_IN_OK
		High	PD_VBUS_C_CTRL1	High	Q7402	OFF	Control by PD_VBUS_C_CTRL1
		ON	PD_VBUS_C_CTRL1	High	PU4302	ON	Control by DC_IN_OK or ACAV_IN
Type-C adapter Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	Low	Q7401	ON	Control by BGATE
		Low	PD_VBUS_C_CTRL1	Low	Q7402	ON	
		OFF	PD_VBUS_C_CTRL1	Low	PU4302	OFF	
Normal adapter + Type-C	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	
		High	PD_VBUS_C_CTRL1	High	Q7402	OFF	
		ON	PD_VBUS_C_CTRL1	High	PU4302	ON	
Battery Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	High	Q7401	OFF	
		Low	PD_VBUS_C_CTRL1	High	Q7402	OFF	
		OFF	PD_VBUS_C_CTRL1	High	PU4302	OFF	
					PU4412	ON	Battery to 19V_DCBATOUT



BOM1

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Title: **TYPEC PD Controller**

Size: Document Number: **Unicorn LV530_KBL_MB14** Rev: **SA**

Date: 11/05/2017 15:2017 Page: 74 of 105

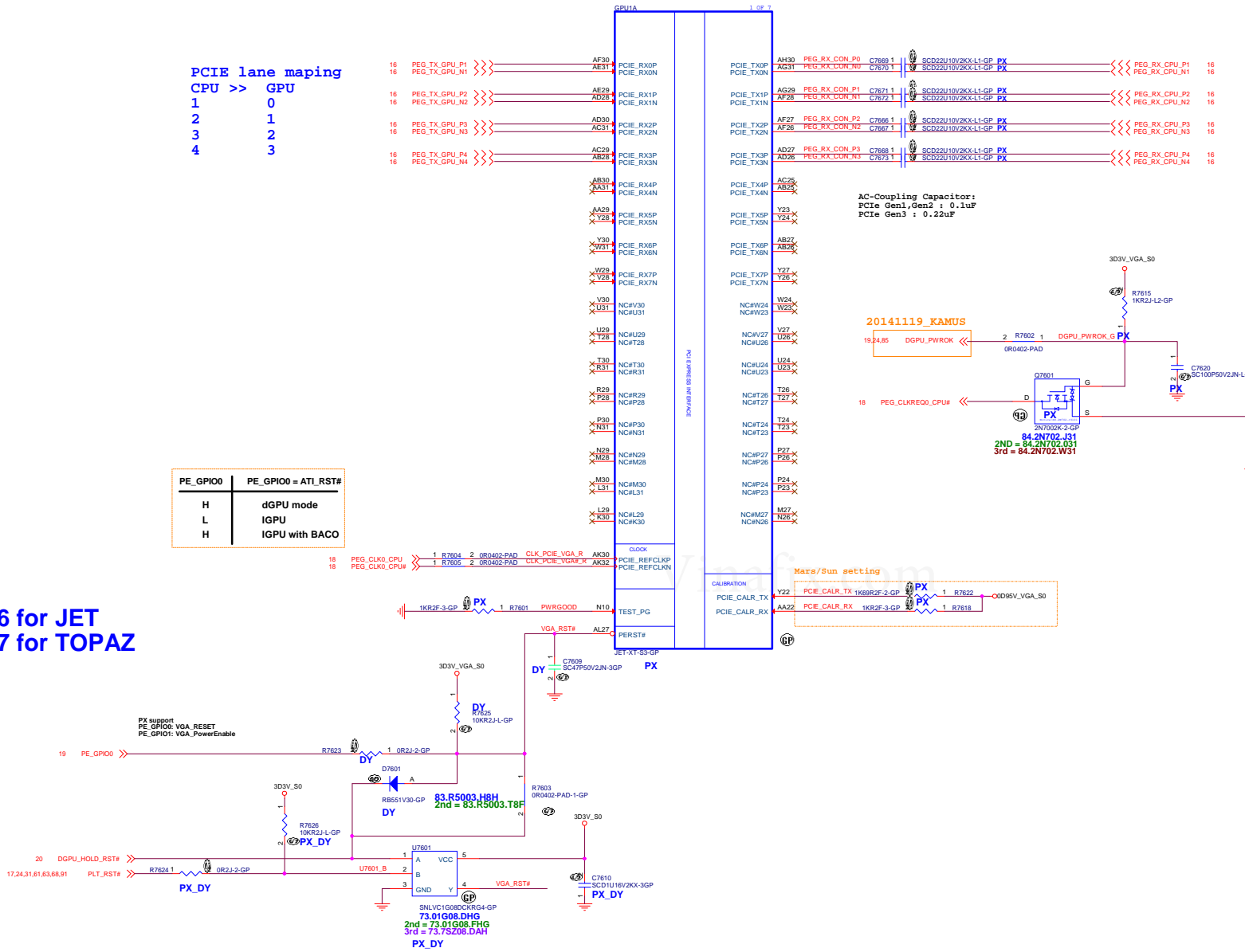
Vinafix.com

PCIE lane mapping
CPU >> GPU

1	0
2	1
3	2
4	3

PE_GPIO0	PE_GPIO0 = ATI_RST#
H	dGPU mode
L	IGPU
H	IGPU with BACO

R16 for JET
R17 for TOPAZ



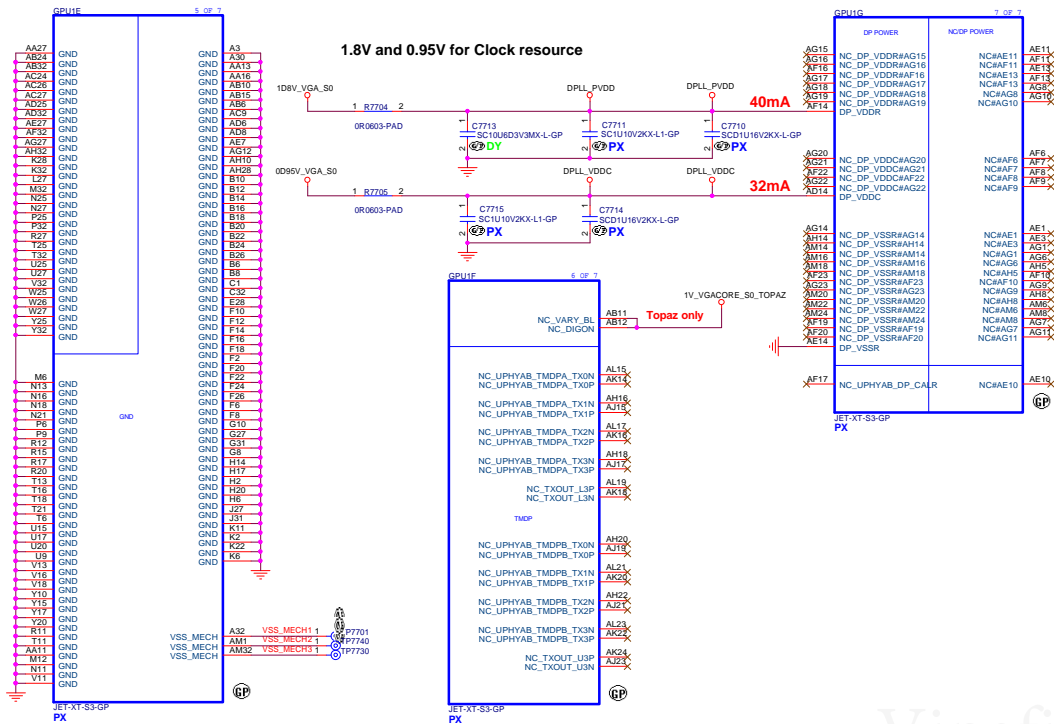
AC-Coupling Capacitor:
PCIe Gen1,Gen2 : 0.1uF
PCIe Gen3 : 0.22uF

20141119_KAMUS

2N7002K-3-GP
84.2N702.131
2ND = 84.2N702.031
3rd = 84.2N702.W31

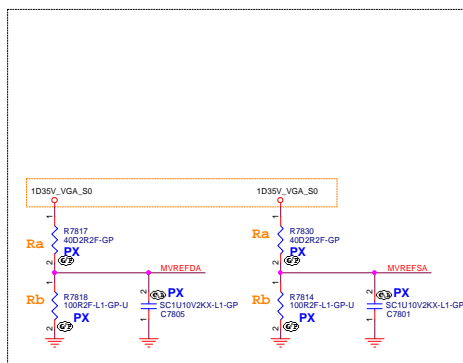
Mesa/Sun setting

BOM1

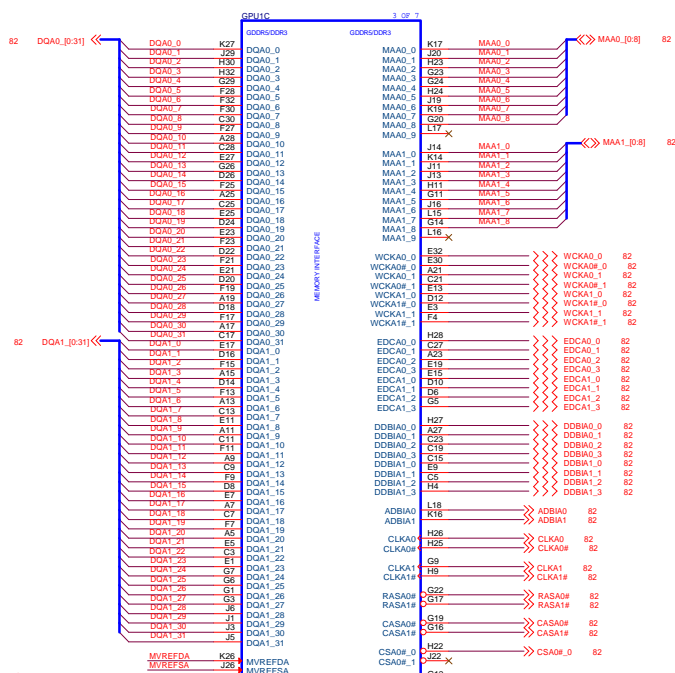
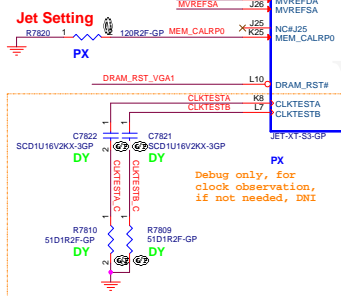
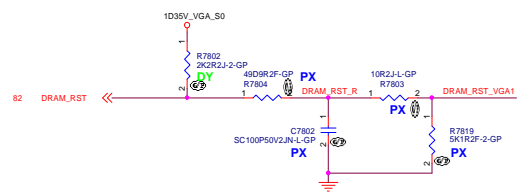


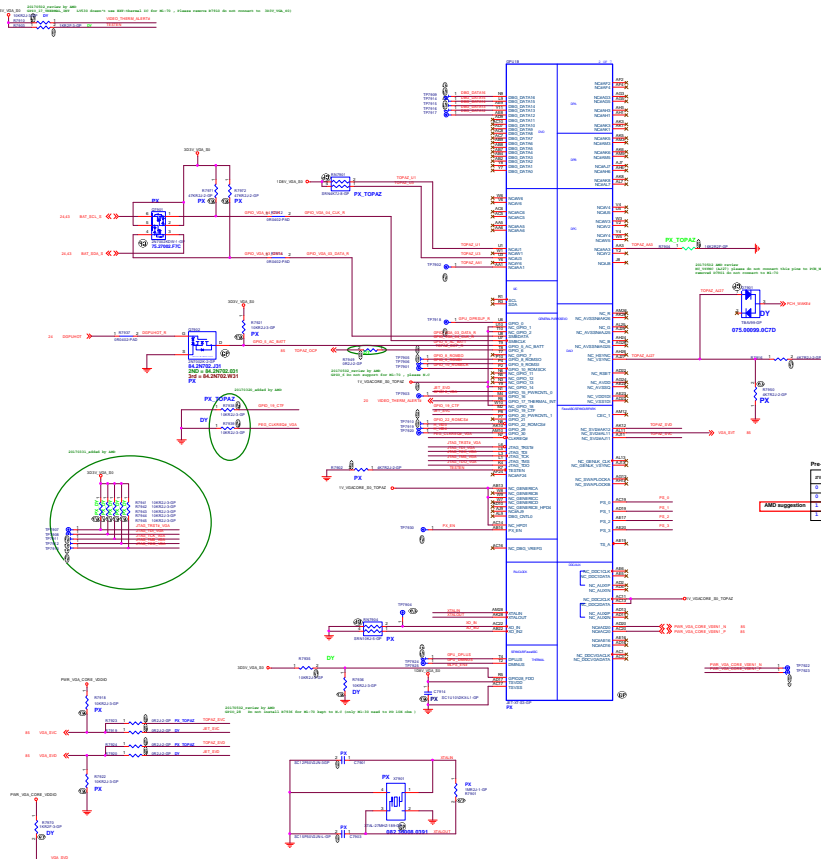
Vinafix.com

Please MVREF drivers and Caps close to ASIC



Place all these componets very close to GPU (within 25mm) and keep all componets close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR5





PS0 - PS3 Setting

Cap Value (pF)	Bin (5-4)	R _{pu} (Ω)	R _{pd} (Ω)	R _{pu} (Ω)	R _{pd} (Ω)	R _{pu} (Ω)	R _{pd} (Ω)	Bin (5-1)
82	01	8200	2000	820	200	820	200	01
15	10	8200	8200	820	820	820	820	10
NC	11	4330	4330	180	180	180	180	11
		2200	2200	220	220	220	220	10
		470	2200	111	111	111	111	10

Note: When PS2 resistors are required.

Board Configure (5-1)

Bin	5	4	3	2	1
PS0	1	1	0	0	1
PS2	1	1	0	1	1
PS3	1	1	1	1	1

Board Configure (2-0)

Bin	2	0	1	0	0	0	1	0	1	0	0
Lenovo PN	SV20L76701	SV20L76696	SV20L76699	SV20L76699	SV20L76699	SV20L76699	SV20L76699	SV20L76699	SV20L76699	SV20L76699	SV20L76699
Wistron PN											
Vendor PN	Hynix 256M32 GDDR5 H5GCH24MUR-ROC 8Gb Samsung 256M32 K4GB0325FB-HC28 8Gb 7Gbps GDDR5 Micron MT51J256M32HF-70A 8Gb 7Gbps GDDR5										

Pin-Matrix METAL VIO CODES

Pin	Name	Output	Package
64540154DL	4930		
64540154DL	4930		
64540154DL	4930		
64280154DL	3900	PULL	
64540154DL	3400	PULL	
64193041DL	10000	PULL	
64479154DL	4750	PULL	

CPU Side GPIDxx

Pin	GPIDxx	GPIDxx
0	0	0
1	0	1

AMD suggest Aperture Size = 256MB

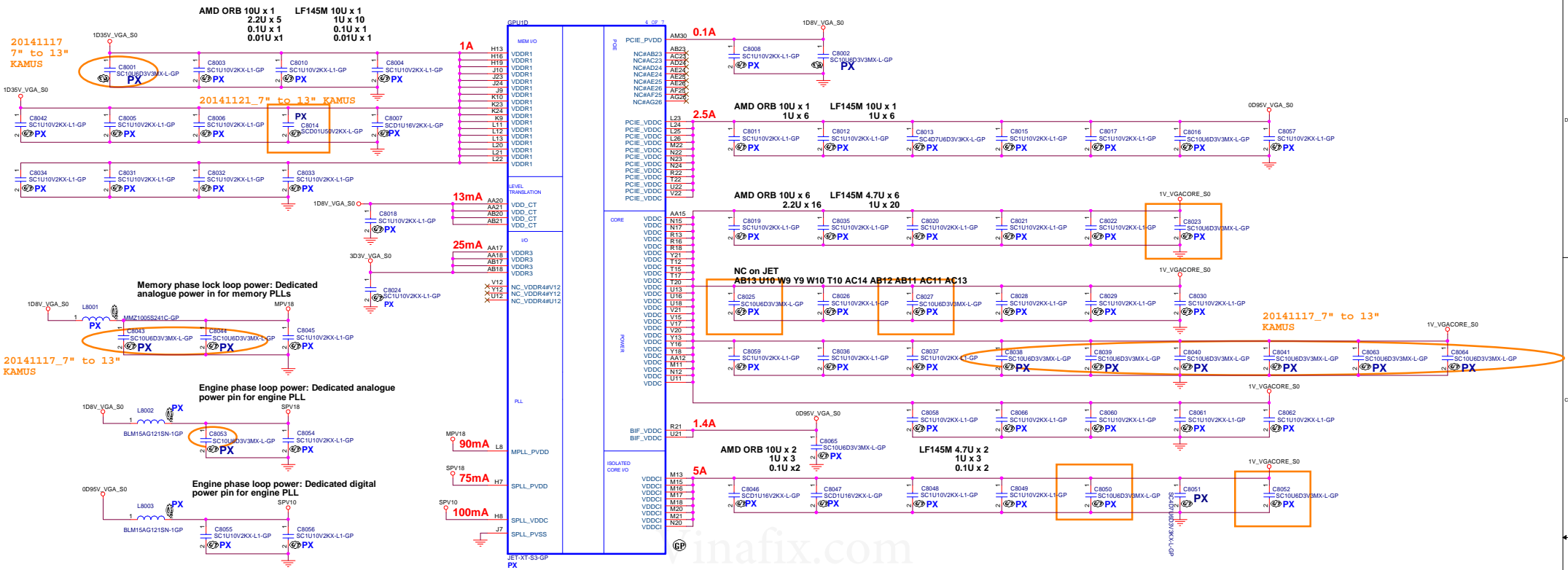
AMD suggest Aperture Size = 256MB

Pin Matrix Table

Pin name	JET	TOPAZ
1 VARY_B (AB1)	NC	VIOA_CORE
2 DECOP (AB2)	NC	VIOA_CORE
3 GENEKCA (AB3)	NC	VIOA_CORE
4 GENEKCC (AB4)	NC	VIOA_CORE
5 GENEKCD (AB5)	NC	VIOA_CORE
6 DECOPDATA (AC1)	NC	VIOA_CORE
7 HFDI (AC2)	NC	VIOA_CORE
8 GDRD (AC3)	NC	VIOA_CORE
9 GDRD (AC4)	NC	VIOA_CORE
10 GDRD (AC5)	NC	VIOA_CORE
11 GDRD (AC6)	NC	VIOA_CORE
12 GDRD (AC7)	NC	VIOA_CORE
13 GDRD (AC8)	NC	VIOA_CORE
14 GDRD (AC9)	NC	VIOA_CORE
15 GDRD (AC10)	NC	VIOA_CORE
16 GDRD (AC11)	NC	VIOA_CORE
17 GDRD (AC12)	NC	VIOA_CORE
18 GDRD (AC13)	NC	VIOA_CORE
19 GDRD (AC14)	NC	VIOA_CORE
20 GDRD (AC15)	NC	VIOA_CORE
21 GDRD (AC16)	NC	VIOA_CORE
22 GDRD (AC17)	NC	VIOA_CORE
23 GDRD (AC18)	NC	VIOA_CORE
24 GDRD (AC19)	NC	VIOA_CORE
25 GDRD (AC20)	NC	VIOA_CORE
26 GDRD (AC21)	NC	VIOA_CORE
27 GDRD (AC22)	NC	VIOA_CORE
28 GDRD (AC23)	NC	VIOA_CORE
29 GDRD (AC24)	NC	VIOA_CORE
30 GDRD (AC25)	NC	VIOA_CORE

NC on JET
AB13 UIO WB YB WB10 TIO AC1A AB12 AB11 AC11 AC13

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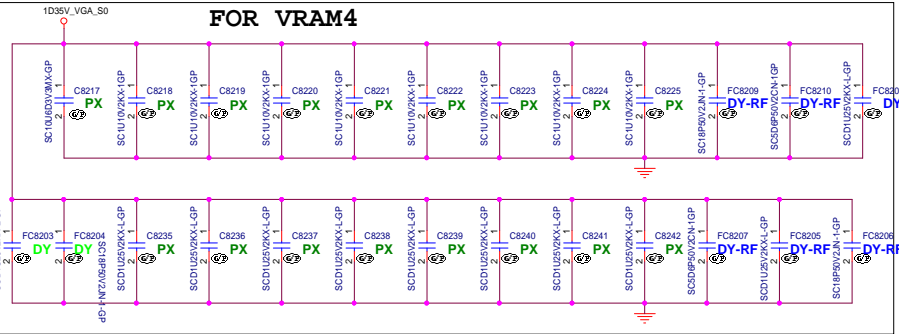
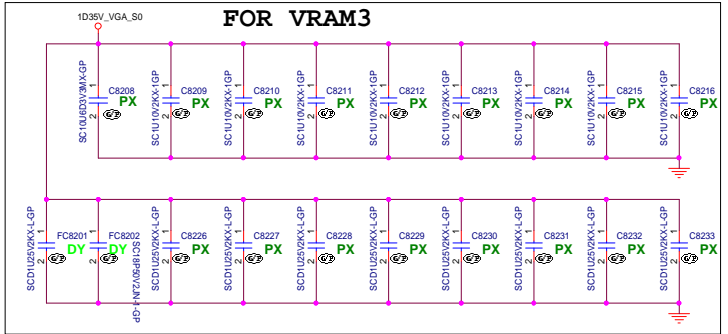
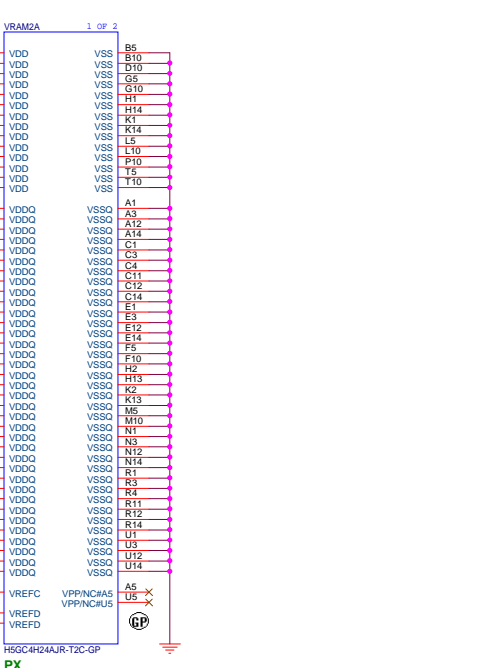
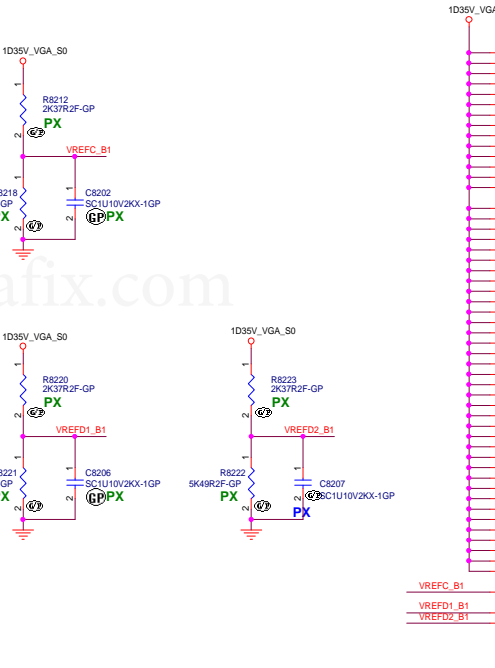
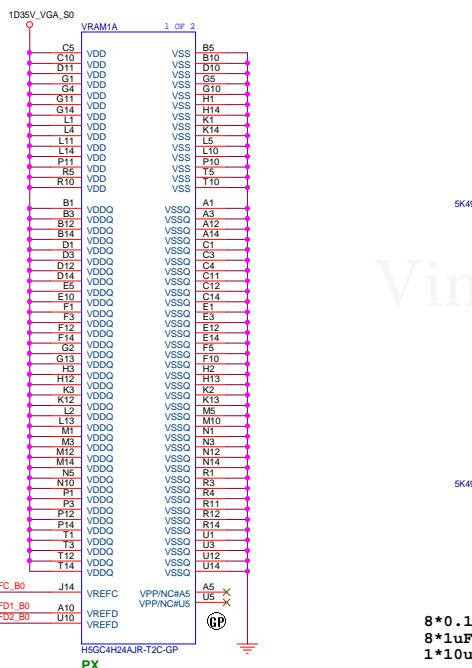
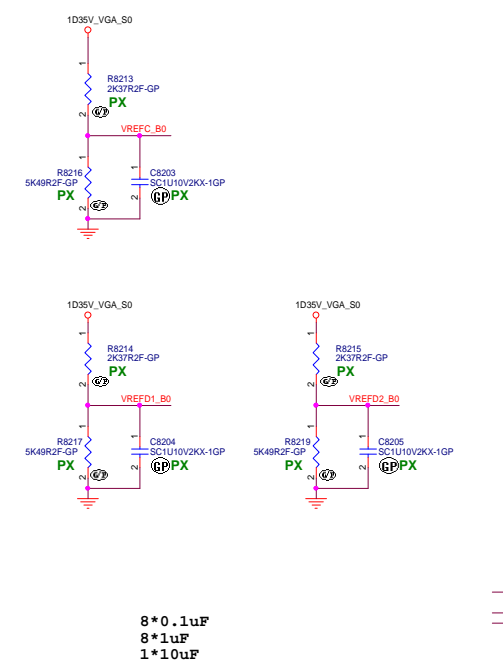
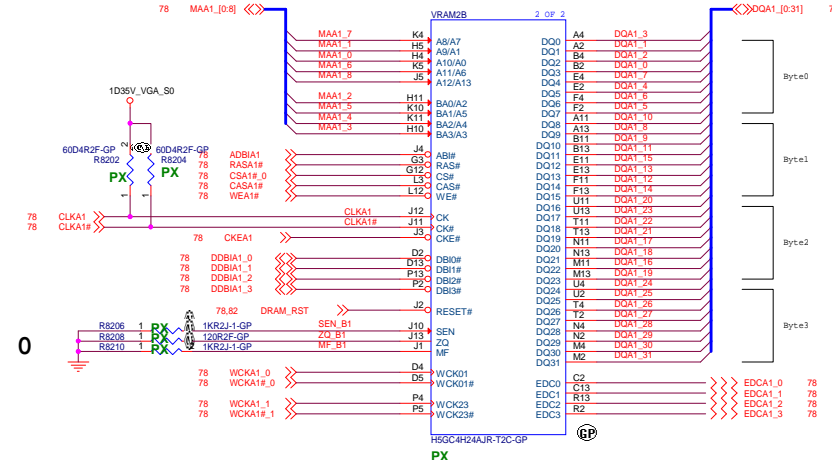
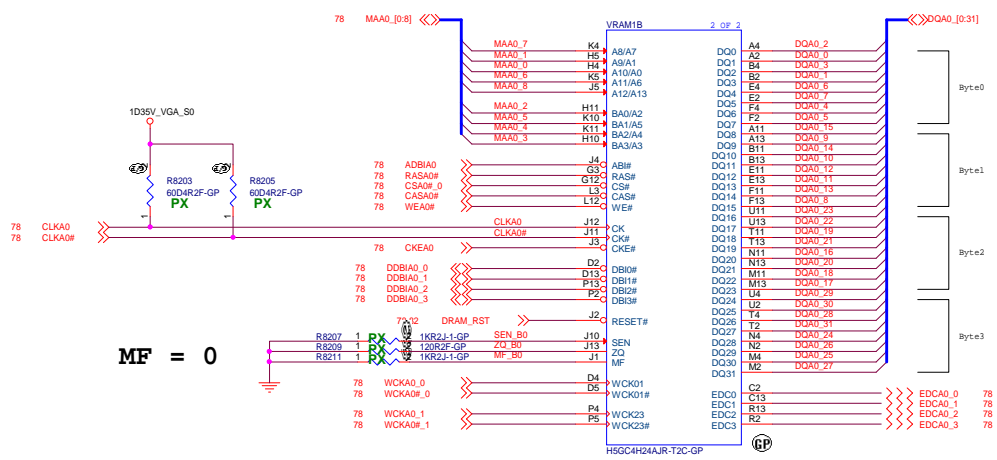


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GPU VRAM7,8 (4/4)

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Document Number

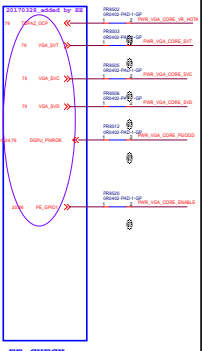
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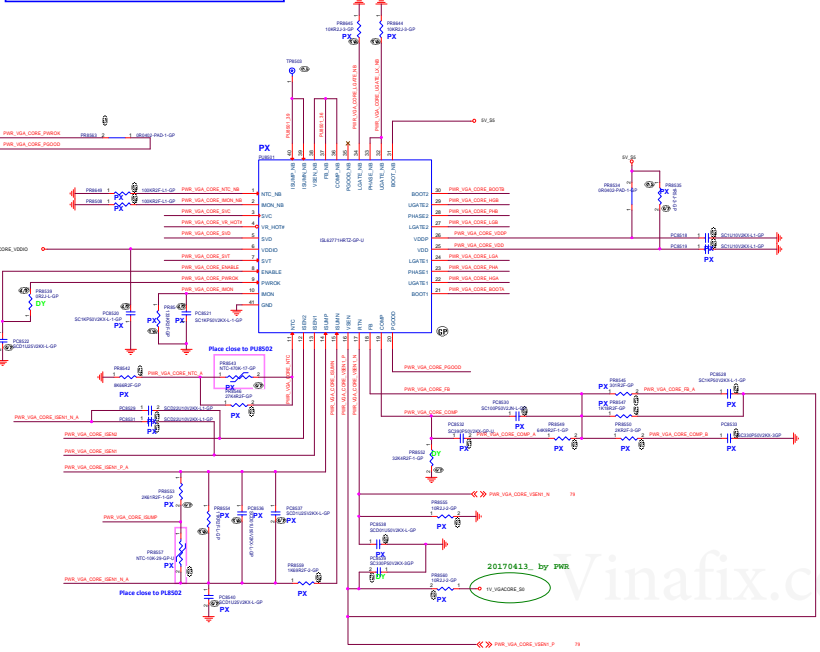
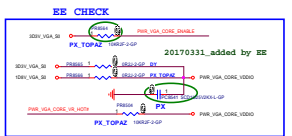
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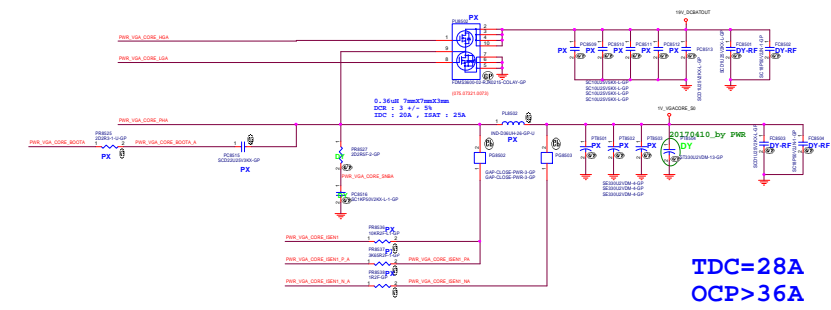
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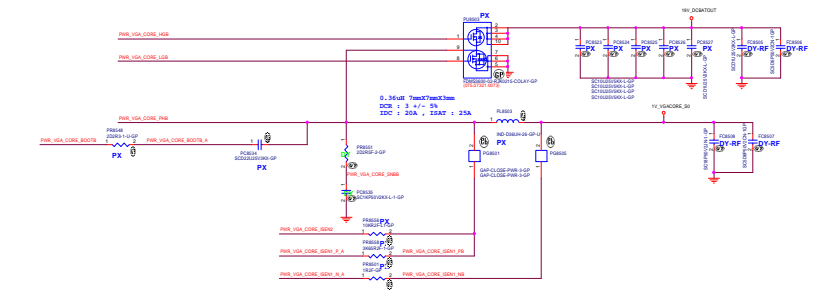
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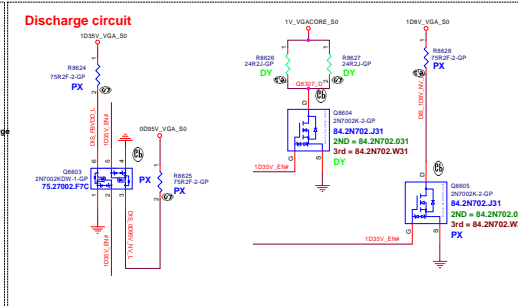
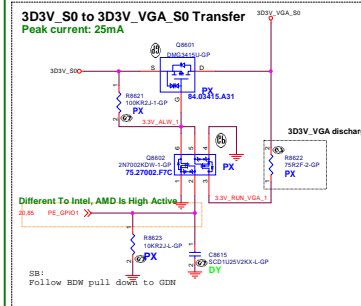
20170413 by PWR



TDC=28A
OCP>36A



20151106 need Add MOS to Control 1D35V_EN# IN SB version

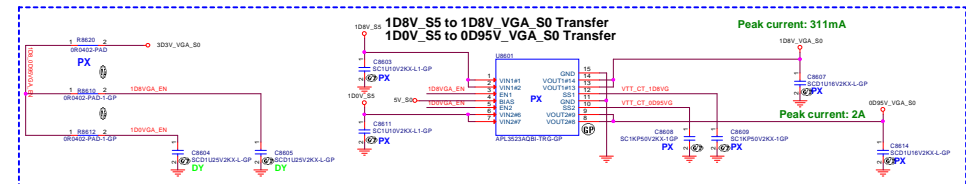


GPU PWR Sequencing
3D3V_VGAS0
 => 0D95V_VGA_S0/1D8V_VGA_S0
 => 1D35V_VGA_S0
 => VGA_CORE

All the ASIC supplies must reach their respective nominal voltages withing **20ms** of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.

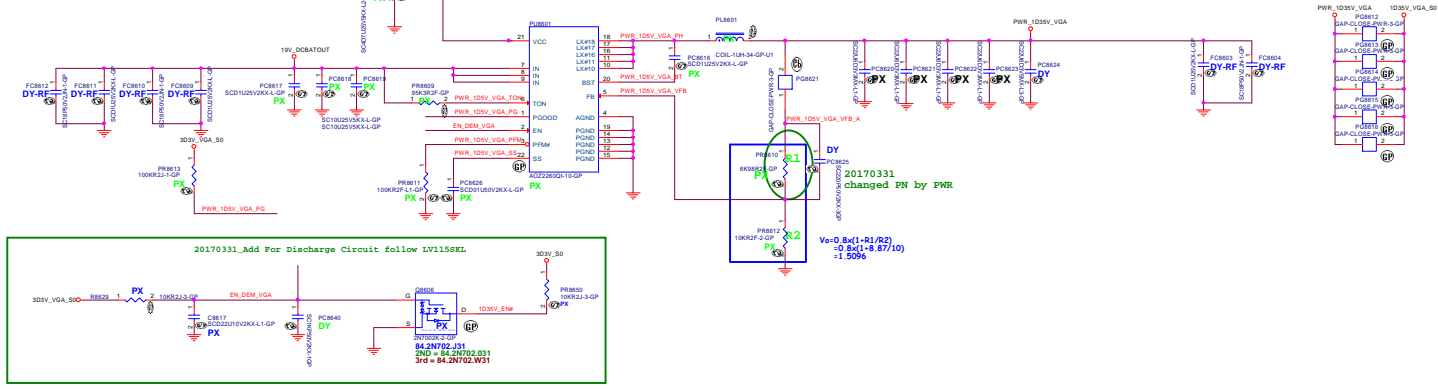
It is recommended that the 3.3V rail ramp up first.

It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.



EE need to confirm 20170208
 EE confirm 20170413

IC	AOZ2262 (10A)	AOZ2261 (8A)	AOZ2260 (6A)
COM	668.1801A.2121	66.1801A.208	66.1801A.208
Check	IDC : 1.8A	IDC : 1.0A	IDC : 1.0A
Output CAP	22uF/6.3V + 5pcs DY*1	22uF/6.3V + 4pcs DY*1	22uF/6.3V + 4pcs DY*1



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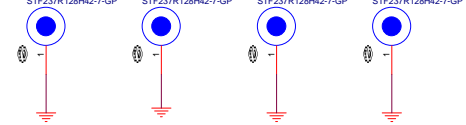
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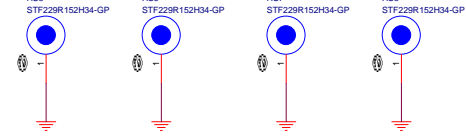
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34.4GD01.101 will change to 434.0DB04.0001 by ME request
Waiting for symbol

34.4WZ01.001 34.4WZ01.001 34.4WZ01.001 34.4WZ01.001



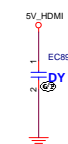
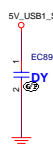
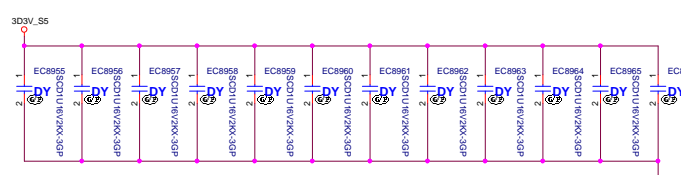
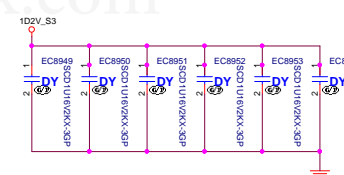
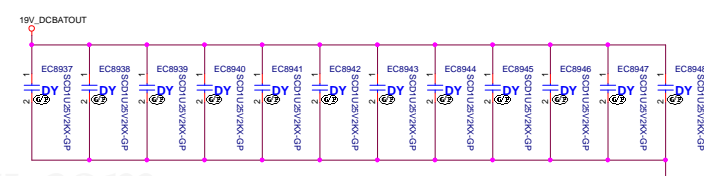
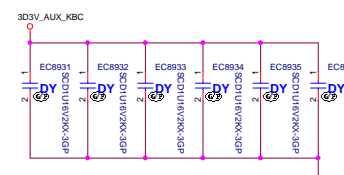
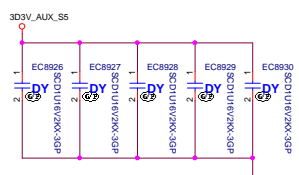
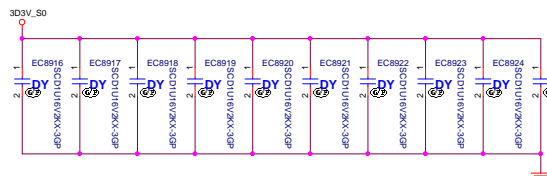
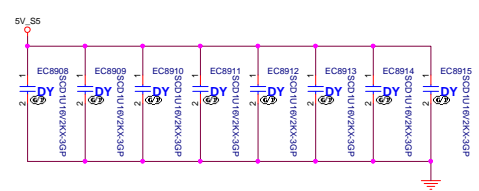
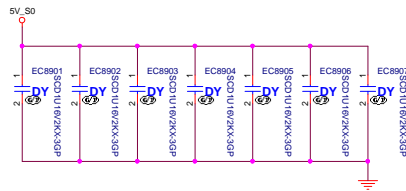
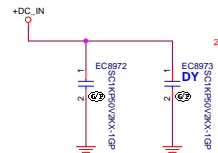
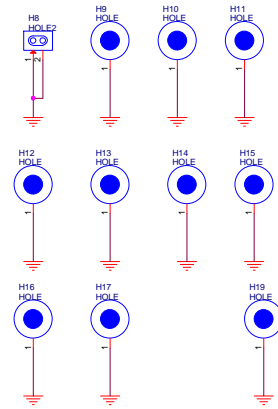
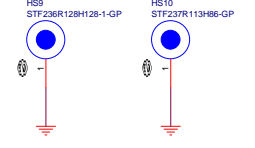
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ZZ.00PAD.EX1 ZZ.00PAD.EJ1 ZZ.00PAD.FN1



34.4LO45.001 434.07K0E.0001



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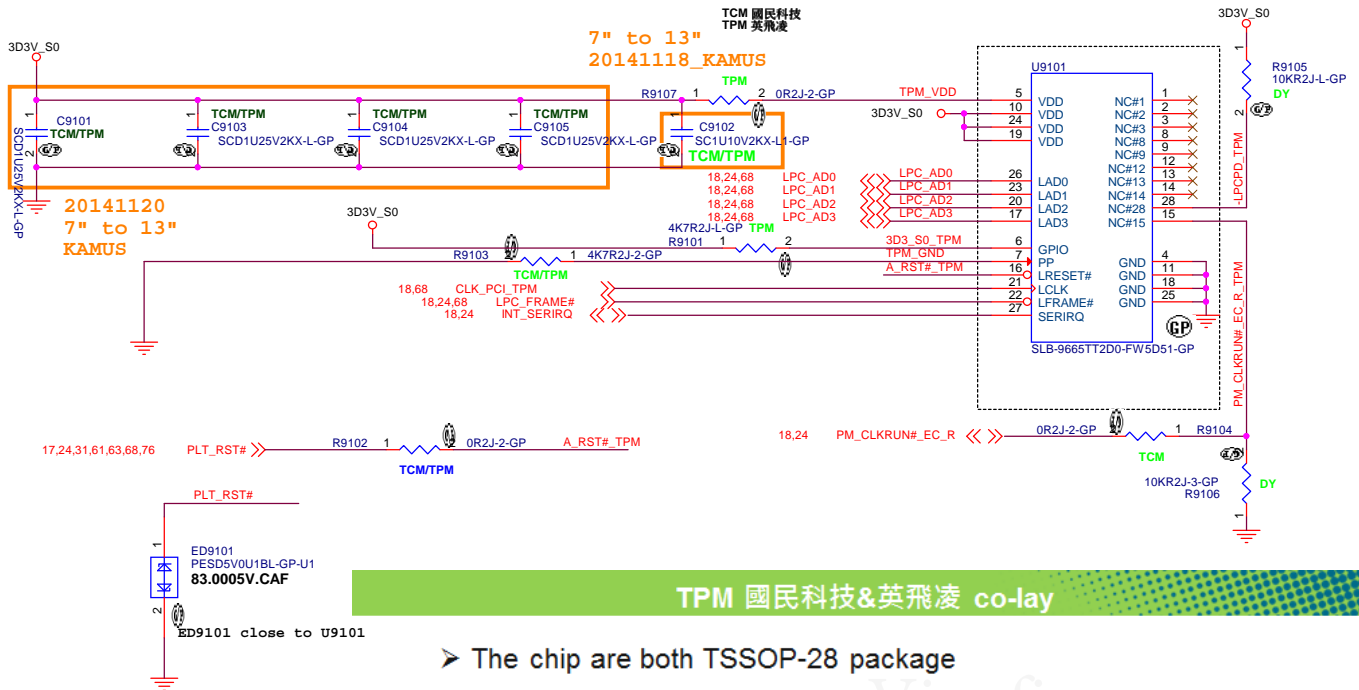
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TPM 國民科技&英飛凌 co-lay

➤ The chip are both TSSOP-28 package

Pin define	國民	英飛凌	Remark	Pin define	國民	英飛凌	Remark
1	NC	NC		15	CLKRUN#	NC	0ohm
2	NC	NC		16	LRESET#	LRESET#	
3	NC	NC		17	LAD3	LAD3	
4	GND	GND		18	GND	GND	
5	NC	VDD	0ohm	19	VDD	VDD	
6	NC	GPIO	0ohm	20	LAD2	LAD2	
7	NC	PP	0ohm	21	LCLK	LCLK	33ohm for 國民
8	NC	NC		22	LFRAME#	LFRAME#	
9	NC	NC		23	LAD1	LAD1	
10	VDD	VDD		24	VDD	VDD	
11	GND	GND		25	GND	GND	
12	NC	NC		26	LAD0	LAD0	
13	NC	NC		27	SIRQ	SERIRQ	
14	NC	NC		28	LPCPD#	NC	0ohm

Czrrizo/Carrizo-Lite + Exo Pro

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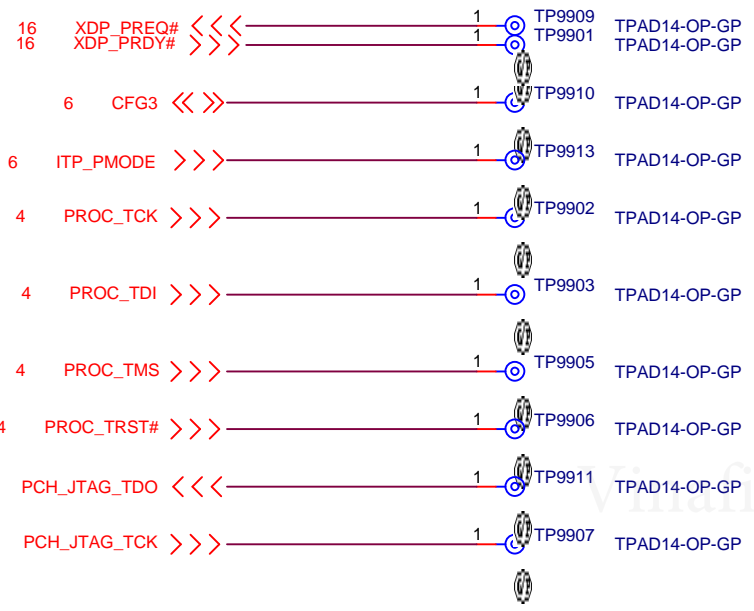
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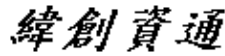
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Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)

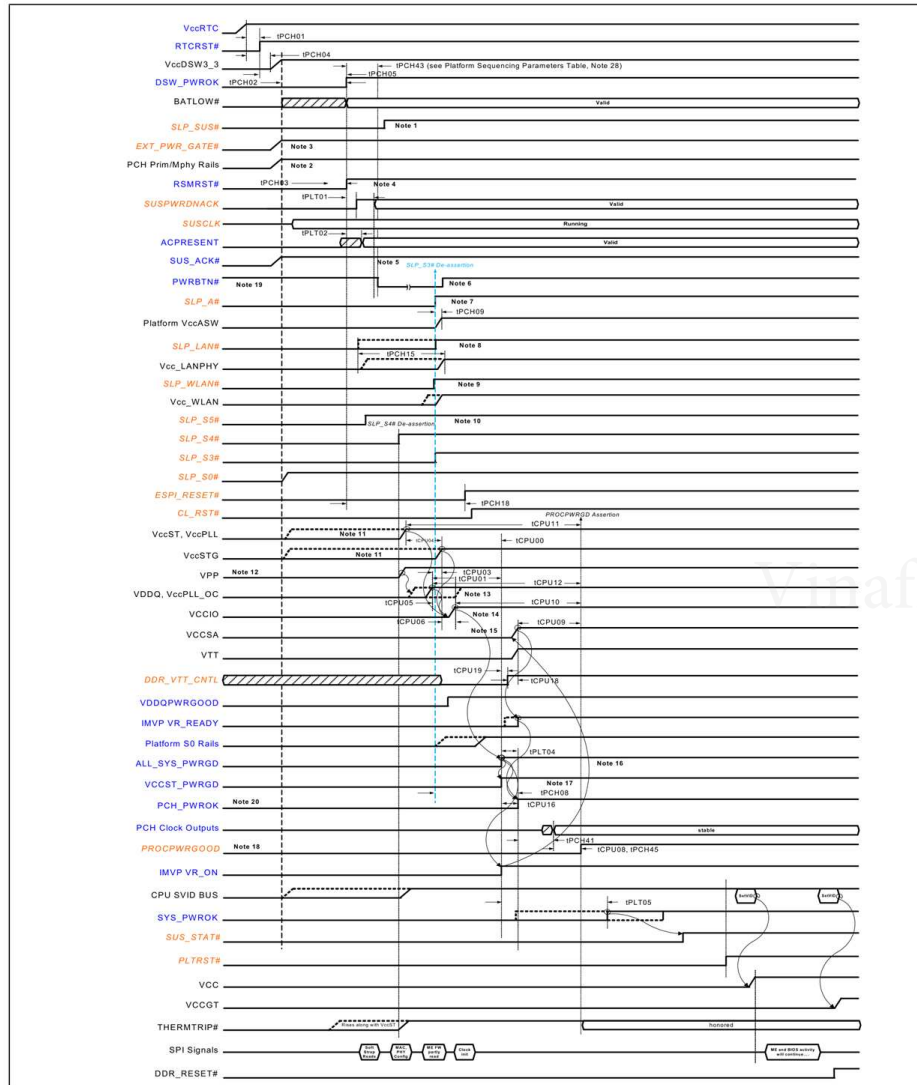


Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 2 of 2)

Notes:

1. SLP_SUS# is ignored in Non-DSx systems
2. Refer Rail-to-Rail Power Sequencing Requirement section for details on PCH prime rail-to-rail power and power down dependencies
3. EXT_PWR_GATE# has been de-featured. This pin, in native mode, will never be driven low
4. For a non-DeepSx system DSU_PWROK and RSMRST# go high at the same time (connected on board)
5. For a non-DeepSx system SUS_ACK# will rise with prime voltage rail powering the VCCPGPPA power pin, due to weak internal pull-up.
6. Minimum duration of PWRBTN# assertion = 16mS. PWRBTN# can assert before or after RSMRST#
7. On first exit from G3, SLP_A# de-asserts with SLP_S3# de-assertion
8. High for WoL=1, Low for WoL=0. SLP_LAN# may rise before, but no later than SLP_A#
9. On first exit from G3, SLP_WLAN# de-asserts with SLP_S3# de-assertion
10. Delay between SLP_S5#, SLP_S4#, and SLP_S3# exaggerated for drawing purposes. If the system EC is driving these signals in ESPI mode if the, the minimum delay between SLP_S3#, SLP_S4#, and SLP_S5# is not guaranteed
11. VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer to Chapter 42, "Platform Debug and Test Hooks" for more details. VCCSTG should only ramp up equal to or after VCCST.
12. Only required with LPDDR3 and DDR4 memory configurations
13. VDDQ must ramp after VPP on DDR4 and LPDDR3 based systems, thus VDDQ may ramp up after SLP_S3# de-assertion due to VR ramp timing and configuration
14. VCCIO, VCCSA must ramp after VccST, VccSTG, and VDDQ have completed their ramps. If VCCSTG and VCCIO supplies are merged together as a single supply, VCCSA must ramp after VccST, VccSTG/VCCIO, and VDDQ have completed their ramps
15. IMVP_VR_ON is recommended to be triggered by ALL_SYS_PWRGD in order to help minimize boot latency.
16. ALL_SYS_PWRGD is assumed to be logically AND together the pwrgood signals for the major system power rails
17. VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it. It is recommended that both VCCST_PWRGD and PCH_PWROK include ALL_SYS_PWRGD in their generation. This ensures during failure events, both signals de-assert at the same time
18. PROCPWRGD is used only for power sequence debug and is not required to be connected to anything on the platform.
19. When "Power Button" is the trigger for wake or sleep event for the system
20. The Platform should ensure that PCH_PWROK does not glitch when RSMRST# is de-asserted

Additional Notes:

The state of the SLP_A# and SUSPWRDNACK signals are used by the EC to determine if PCH requires the suspend-well to stay powered.

- SUSPWRDNACK
 - Platform not supporting M3 - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted **OR** System state is S3. Else, EC has an option to do whatever it wants with the SUS Rails
 - Platform supporting M3 - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted **OR** System state is S3 **OR** SLP_A# is de-asserted **OR** it is the first 200mS after SUS Rails power has been applied. Else, EC has an option to do whatever it wants with the SUS Rails
- Primary rails and Deep Sx Rails should **never** be active while VccRTC rail is inactive.

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POWER BLOCK DIAGRAM

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SMBUS BLOCK DIAGRAM

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