Measurements

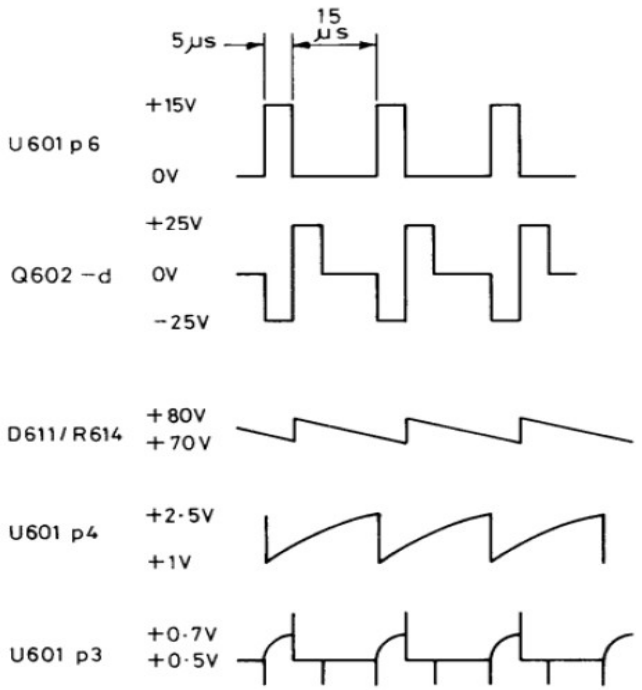

Fig. 5.4.18 Typical Power Supply Waveforms

5.4.19 Video Horizontal Deflection and Line Correction U701b and C706 form part of a ramp generator. R708 and R709 determine the charging current through C706, how-ever not all the current through the above resistors comes from C706, some is supplied via R701 and R702. When the right hand end of C706 (PLD5) is positive, U701b pin 3 sinks current through D711, and R702 has 0V at both its ends. Together with R701 and C706 this results in a curved RC ramp being generated instead of the more usual linear ramp from a simple integrator. When the right hand end of C706 is negative, U701b switches diodes D709 and D711 off and acts as an inverting amplifier with a gain of -2. The gain is set by R712 and R713. Twice the current flows through R702 as can flow in R701. Half the current flows through R701, the other half causes an RC bend to be given to the ramp, but in the oppo-site direction to the bend caused by R701 when C706 was positive. The overall result of this circuit is that the current through the horizontal yoke L704a has a slightly 'S' shaped waveform which can be seen by monitoring the voltage across R717. The ramp is reset by Q712 which in turn is
switched by Q701 driven from NFSYNC. Capacitor C706 is not reset to 0V, but the maximum negative ramp voltage. When Q712 is on, the voltage on C706 must be negative in order to force the voltage at the junction of R707 and R710 to be 0V. The amplitude and starting level of the ramp are set by R709 and R706 respectively. The horizontal yoke L704a is driven by the power Op-amp U70la. pin 8 of which is a virtual earth, as is U701b pin 5.

Measurements C702 negative going pulse 4ms wide 5V pk-pk every 20ms
U70la pin8 positive going pulse 0.2ms wide 0.5V pk-pk every 20ms
U701a pin 1 positive going 20ms linear ramp 6V pk-pk centered about 0V First 4ms flat with 15V negative pulse at start
R717 positive going 20ms linear ramp 2V pk-pk centered about 0V first 4ms flat
U701b pin 3 negative going 20ms linear ramp 3V pk-pk and last 7ms flat

5.4.20 Video Vertical Deflection The vertical defection circuit used in the 400 is a standard television tuned flyback system. T701 the line output transformer (LOPT) is really a tapped inductor which stores and then later releases energy. C722 filters a boost voltage gen-erated during the forward conduction of D705. Two simple halfwave rectifier circuits driven from the flyback pulse generate the required 75V and 400V; D704 and C720 pro-duce 75V whilst D703 and C719 produce 400V. The 8kV EHT voltage comes from a voltage doubler fed from an overwind on the LOPT. Line sync pulses LSYNC from the gate array are delayed by U703 to fix the position of the video relative to the raster, then so long as the display ena-ble line from U702 pin 14 into U703b pin 13 is high, the sync pulses turn on Q715 which then turns on FET Q716 sinking current from +15V through part of T701's primary winding to ground. When Q716 turns off, its drain voltage rapidly rises to about 350V. C718 and the vertical coils L701. L702 and L704b tune the pulse at this point so that it becomes relatively flat topped and 5µs wide for efficient rectification. The body diode of Q716 catches the pulse as it swings negative and clamps the drain to just below 0V.
The flyback pulse causes the scan current in L701, L702 and L704b to reverse thereby forcing the sweep to retrace from the top to the bottom of the CRT. C721 is the S correction capacitor which supplies a sinusoidal current phased such that the resultant sweep current waveform is slightly S shaped to compensate for the geometric distortion caused by the flat CRT screen. When the instrument is first switched on. the soft start cir-cuit Q702, R763 and C714, controlled by NRS pulses reduces the width of the output from U703b which reduces the time that Q716 is on and thus the current drawn, so that when the instrument is powered by a DC power supply. the peak start-up current is substantially reduced.