National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM2595-12-X REV 2A0

Original Creation Date: 09/07/95
Last Update Date: 03/09/99
Last Major Revision Date: 01/11/99

SIMPLE SWITCHER[TM] 1A STEP-DOWN VOLTAGE REGULATOR

General Description

The LM2595-12 is a monolithic integrated circuit that provides all the active functions for a step-down (buck) switching regulator, capable of driving a 1A load with excellent line and load regulation.

Requiring a minimum number of external components, this regulator is simple to use and includes internal frequency compensation and a fixed-frequency oscillator.

The LM2595 operates at a switching frequency of 150KHz thus allowing smaller sized filter components than lower frequency switching regulators.

A standard series of inductors are available from several different manufacturers, optimized for use with the LM2595. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed ±4% tolerance on output voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency. External shutdown is included, featuring typically 80uA standby current. Self protection features include a two stage current limit for the output switch and an over temperature shutdown for complete protection under fault conditions.

Industry Part Number

LM2595

NS Part Numbers

LM2595J-12-QML

Prime Die

LM2595

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Guaranteed 1A output load current
- Input voltage range up to 40V
- Requires only 4 external components
- Excellent line and load regulation specifications
- 150KHz fixed frequency internal oscillator
- TTL Shutdown capability
- Low power standby mode, Iq typically 80uA
- High Efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection
- CONTROLLING DOCUMENT:
  LM2595J-12-QML 5962-9650201QEA

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to Negative converter

(Absolute Maximum Ratings)

(Note 1)

Maximum Supply Voltage		45V
$\overline{ON}$/OFF Pin Input Voltage		-0.3 ≤ V ≤ +25V
Feedback Pin Voltage		-0.3 ≤ V ≤ +25V
Output Voltage to Ground (steady state)		-1V
Power Dissipation (Note 2, 3)		Internally Limited
Storage Temperature Range		-65 C to +150 C
ESD Susceptibility (Note 4)		2kV
Lead Temperature Soldering, (10 seconds)		+260 C
Maximum Junction Temperature		+150 C
Thermal Resistance ThetaJA 16-Pin CERAMIC DIP	(Still Air @ 0.5W)	75 C/W
	(500LF/Min Air flow @ 0.5W)	35 C/W
ThetaJC 16-Pin CERAMIC DIP (Note 3)		2 C/W
Package Weight (Typical) 16 - Pin Ceramic Dip		1920mg

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using junction-to-ambient, rather than junction-to-case, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out of the package, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated junction-to-case thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance, and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.

Note 4: Human body model, 1.5K Ohms in series with 100pF.

Recommended Operating Conditions

(Note 1)

Operating Temperature Range	-55 C ≤ TA ≤ +125 C
Supply Voltage	4.5V to 40V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Characteristics

SYSTEM PARAMETERS:

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vout	Output Voltage	15V ≤ Vin ≤ 40V, IL = 0.1A to 1A			11.52	12.48	V	1
		15V ≤ Vin ≤ 40V, IL = 0.1A to 1A			11.40	12.60	V	2, 3

DEVICE PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vin = 24V, Iload = 200mA

Vsat	Saturation Voltage	Iout = 1A	3, 4			1.2	V	1
			3, 4			1.5	V	2, 3
Icl	Current Limit	Peak Current	3, 4		1.2	2.4	A	1
			3, 4		1.00	2.6	A	2, 3
Il	Output Leakage Current	Output = 0V	3, 5, 6		-50		uA	1
			3, 5, 6		-210		uA	2, 3
		Output = -1V	3, 5, 6		-15		mA	1
			3, 5, 6		-40		mA	2, 3
Iq	Quiescent Current		5			10	mA	1
			5			15	mA	2, 3
Istby	Standby Quiescent Current	ON/OFF Pin = 5V (OFF)	6			200	uA	1
			6			250	uA	2, 3
Ib	Feedback Bias Current					50	nA	1
						100	nA	2, 3

Electrical Characteristics

$\overline{ON}$/OFF CONTROL:

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vin = 24V, Iload = 200mA

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vih	$\overline{ON}$/OFF Pin Logic Input Threshold Voltage	Low (Regulator ON)				0.6	V	1, 2, 3
Vil	$\overline{ON}$/OFF Pin Logic Input Threshold Voltage	High (Regulator OFF)			2.0		V	1, 2, 3
Iih	$\overline{ON}$/OFF Pin Input Current	Vlogic = 2.5V (Regulator OFF)				15	uA	1
Iih	$\overline{ON}$/OFF Pin Input Current	Vlogic = 2.5V (Regulator OFF)				20	uA	2, 3
Iil	$\overline{ON}$/OFF Pin Input Current	Vlogic = 0.5V (Regulator ON)				5	uA	1
Iil	$\overline{ON}$/OFF Pin Input Current	Vlogic = 0.5V (Regulator ON)				5.5	uA	2, 3

AC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vin = 24V, Iload = 200mA

Fo	Oscillator Frequency		2		127	173	KHz	4
			2		110	173	KHz	5, 6

Note 1: External components such as the catch diode, inductor, input and output capacitors, and voltage programming resistors can affect switching regulator system performance.
Note 2: The switching frequency is reduced when the second stage current limit is activated. The amount of reduction is determined by the severity of current overload.
Note 3: No diode, inductor or capacitor connected to output pin.
Note 4: Feedback pin removed from output and connected ot 0V to force the output transistor switch ON.
Note 5: Feedback pin removed from output and connected to 15V, to force the output transitor switch OFF.
Note 6: Vin = 40V.

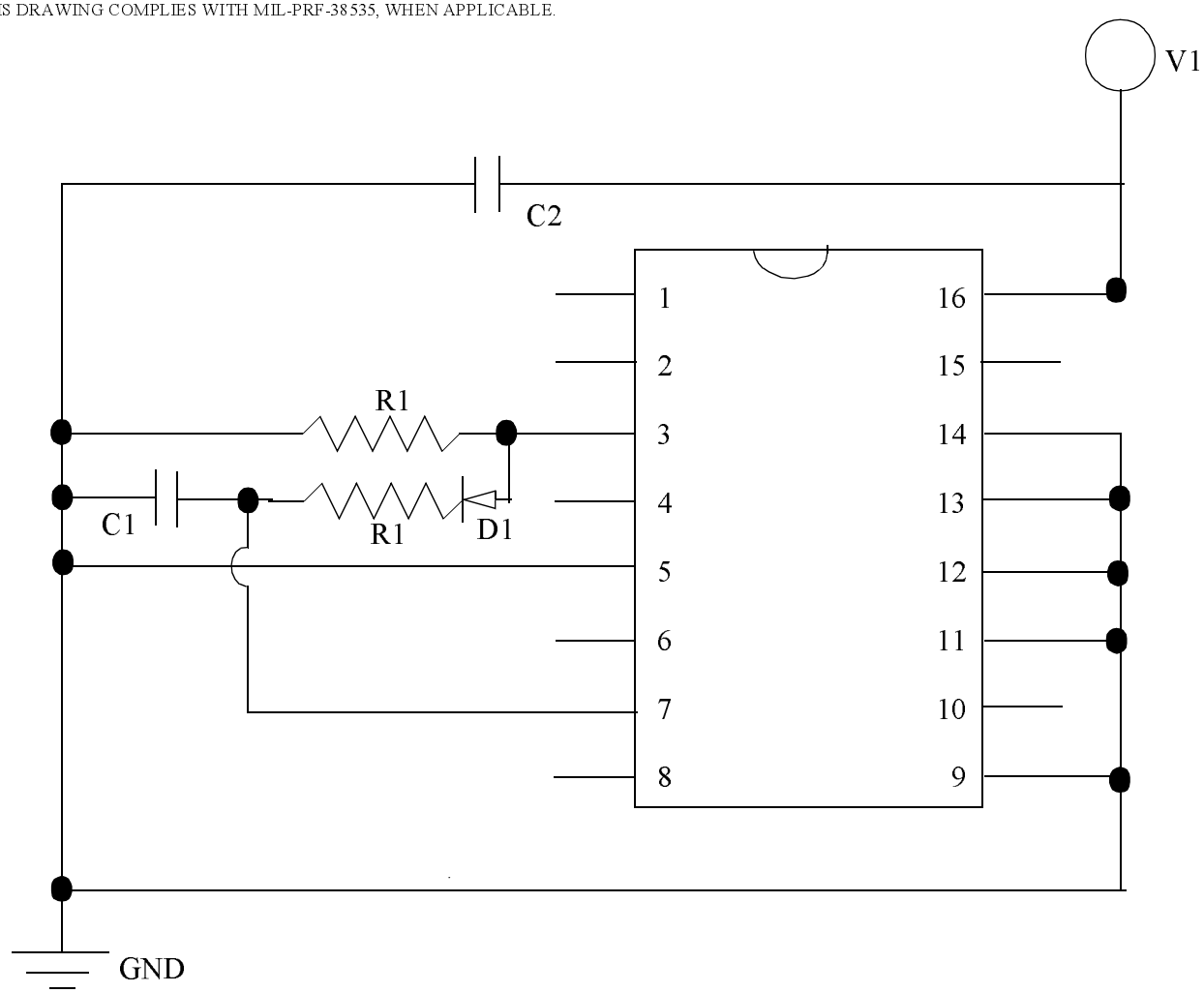
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06327HRA1	CERDIP (J), 16 LEAD (B/I CKT)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
P000132A	CERDIP (J) 16 LEAD (PIN OUT)

See attached graphics following this page.

GENERAL NOTES:
1. GENERIC - INDUSTRY TYPE DEVICES THAT MAY BE USED WITH THIS CIRCUIT SHALL BE AS SPECIFIED IN NSC BURN-IN CIRCUIT LIST R512B-04.
2. ALL 1/4 AND 1/2 WATT RESISTORS SHALL BE METAL FILM. ALL 1, 2, AND 3 WATT RESISTORS SHALL BE WIRE WOUND. TOLERANCE SHALL BE +/-5% UNLESS OTHERWISE SPECIFIED.
3. ALL VOLTAGES SPECIFIED SHALL BE MEASURED AT THE "DEVICE UNDER TEST" PIN AND SHALL BE MINIMUM VALUES UNLESS OTHERWISE SPECIFIED.
4. WHEN APPLICABLE, CLOCK PULSES SPECIFIED SHALL HAVE 50% DUTY CYCLE.
5. THIS DRAWING COMPLIES WITH MIL-PRF-38535, WHEN APPLICABLE.

ECN	REV	APPROVALS	DATE
06797	A1	T.TRINH	9/29/95
		J.GOMEZ	8/26/97



DUT CONDITIONS							
SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS
V1	+39	+41	VOLT				

COMPONENT REQUIREMENTS PER POSITION		
REF DESIG.	QTY	DESCRIPTION
C1	1	1 UF, 75V, 20%
C2	1	4.7 UF, 75V, 20%
A1	2	2 Kohms, 1/4W, 5%
D1	1	1N4001, 1A Class
		100 mA tolerance

Note 6: PD (Power Dissipated) Maximum 600 mW
Note 7: V1 Nominal 40V; I1 Typical 10mA and Max 15 mA
Note 8: LM2595-XX

National Semiconductor
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

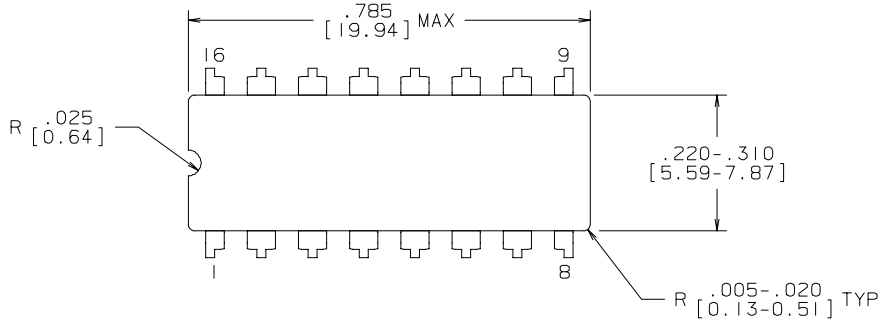
BURN-IN CIRCUIT LINEAR MIL AERO

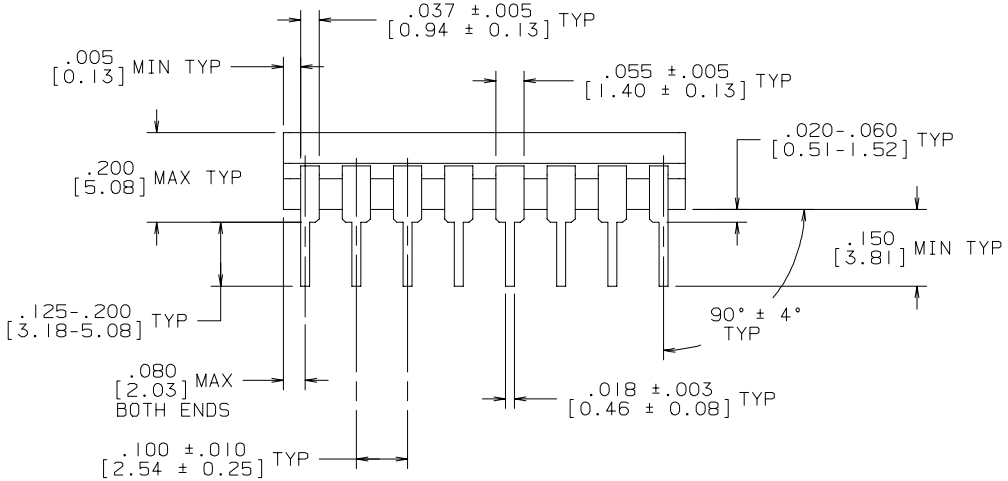
SH 1 OF 1

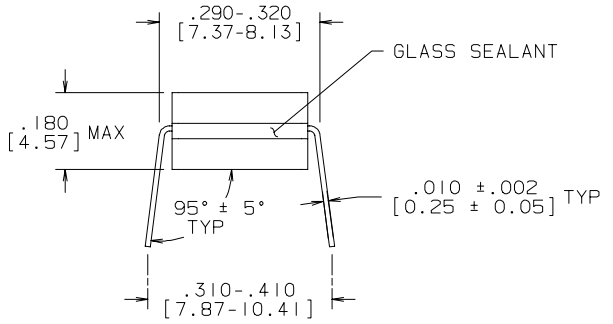
CUSTOMER	PACKAGE TYPE	MIL	NSC	TEST CONDITION
	J16A		Note 8	C

ORIGINATOR	DATE	CHECKED BY	DATE	DRAWING NUMBER	REV
T.Trinh	9/29/95			06327HR	A1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93	TL/







MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

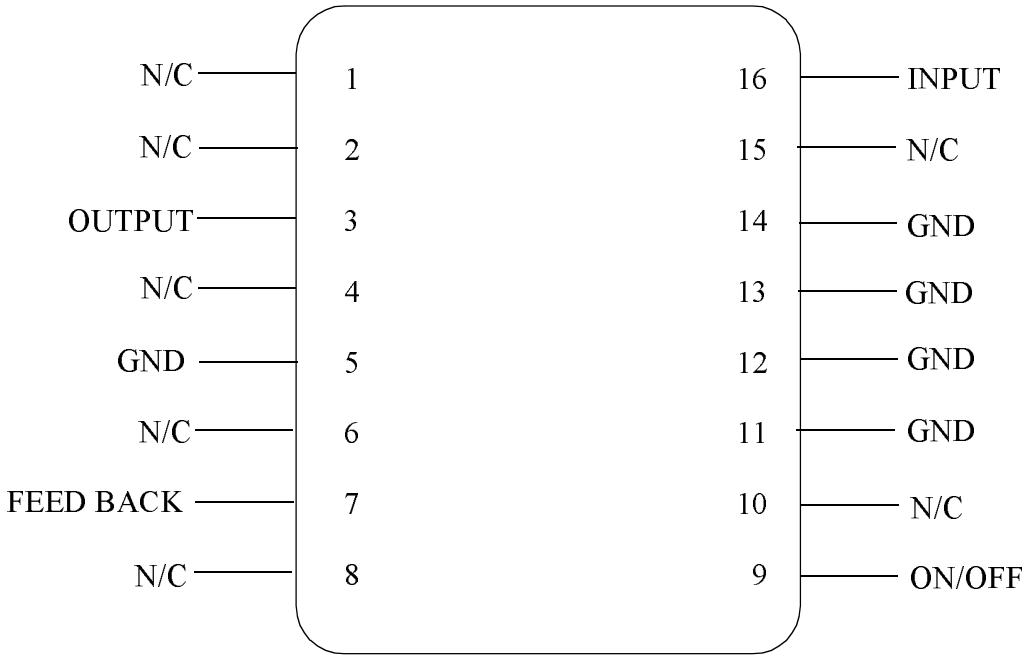
INCH [MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 16 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J16A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



LM2595J-XX

16 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000132A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0000584	07/08/98	Barbara Lopez	Initial Release of: MNLM2595-12-X Rev. 0A0.
1A0	M0002898	03/09/99	Rose Malone	Update MDS: MNLM2595-12-X, Rev. 0A0 to MNLM2595-12-X, Rev. 1A0 - Condition for Vout, Subgroups for Fo and moved to AC Parameter Section. Added limits to Il, Iq, Iih, Iil. Added Ib Condition to datasheet. Added Package Weight to Absolute section.
2A0	M0003220	03/09/99	Rose Malone	Update MDS: MNLM2595-12-X, Rev. 1A0 to MNLM2595-12-X, Rev. 2A0.