AN-6611

Binary/BCD Gain Programmed Amplifiers

Many systems require logic controlled Gain Programmable Amplifiers (GPA) for signal preconditioning, level control and dynamic range expansion. The system sets GPA requirements for accuracy, speed and signal handling capability, limiting the type used. Conventional CMOS analog switches limit signal handling to ±7.5 V and accuracy to 1%. High voltage CMOS or JFET analog switches increase both accuracy and signal handling (±10 V to ±15 V) but at a greater cost. Programmable amplifiers using current mode analog switches have the highest signal handling capability (±25 V) with high accuracy, speed and low cost.

In reality, the logic controlled GPA is a multiplying digital-to-analog converter (multiplying D/A). The D/A input is the reference node which is multiplied by the digital input. Multiplying D/A converters have been available for some time in module, hybrid and monolithic form but suffer from high cost and poor signal handling capability (±10 V maximum).

Large signal handling (±25 V), moderate cost multiplying D/A converters can be built using monolithic current mode analog switches, an op amp and a few resistors.

Unlike conventional analog switches, only signal current is switched at the virtual ground of an op amp with current mode analog switches. Limiting the voltage across the switch to a few hundred millivolts, power supplies, logic interface and level translator circuits are eliminated allowing the JFET switches to be driven directly by standard logic.

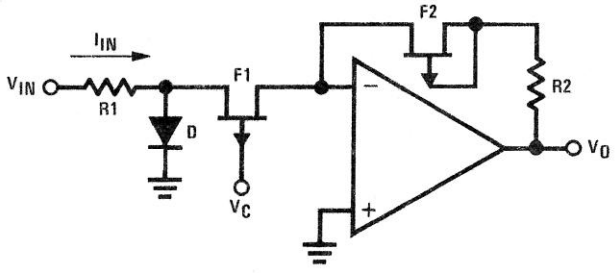


Figure 1. Current Mode Analog Switch

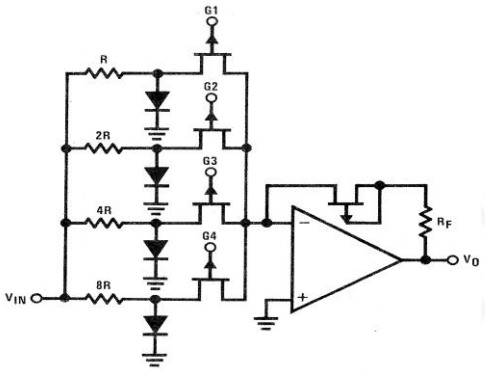
A logic "0" turns the switch ON with a logic "1" shutting the switch OFF by pinching the JFET OFF. The diode is used to clamp the source to drain voltage to about 0.7 V in the switch OFF state. The series JFET in the feedback path is used to compensate for the ON resistance of the switch JFET.

Current through the switch is determined by the input resistor, R1, the switch ON resistance and the input voltage, V_{IN}. Scaling of the output voltage is accomplished with the feedback resistor, setting the gain of the amplifier.

$$A_V = -\frac{R2 + R_{ON2}}{R1 + R_{ON1}} \qquad (1)$$

A 4-bit multiplying D/A converter can be built using a quad current mode switch, 4 binary weighted resistors (R, 2R, 4R, and 8R) and an op amp. The output voltage will be a function of the feedback resistor, input resistors and the logic state of the JFET gates, G_N.

The number of bits is expanded by cascading another quad current switch and resistor array to the first. Instead of continuing the binary progression of the input resistors, (16R, 32R, etc), current splitting resistors are used such that the same resistor array (R, 2R, 4R, 8R) is used for the additional bits, minimizing the number of resistor values required for higher order converters.



$$V_O = -V_{IN}\frac{R_F}{R}\left(\bar{G}1\,2^0 + \bar{G}2\,2^{-1} + \bar{G}3\,2^{-2} + \bar{G}4\,2^{-3}\right)$$

Figure 2. 4-Bit Multiplying D/A Converter

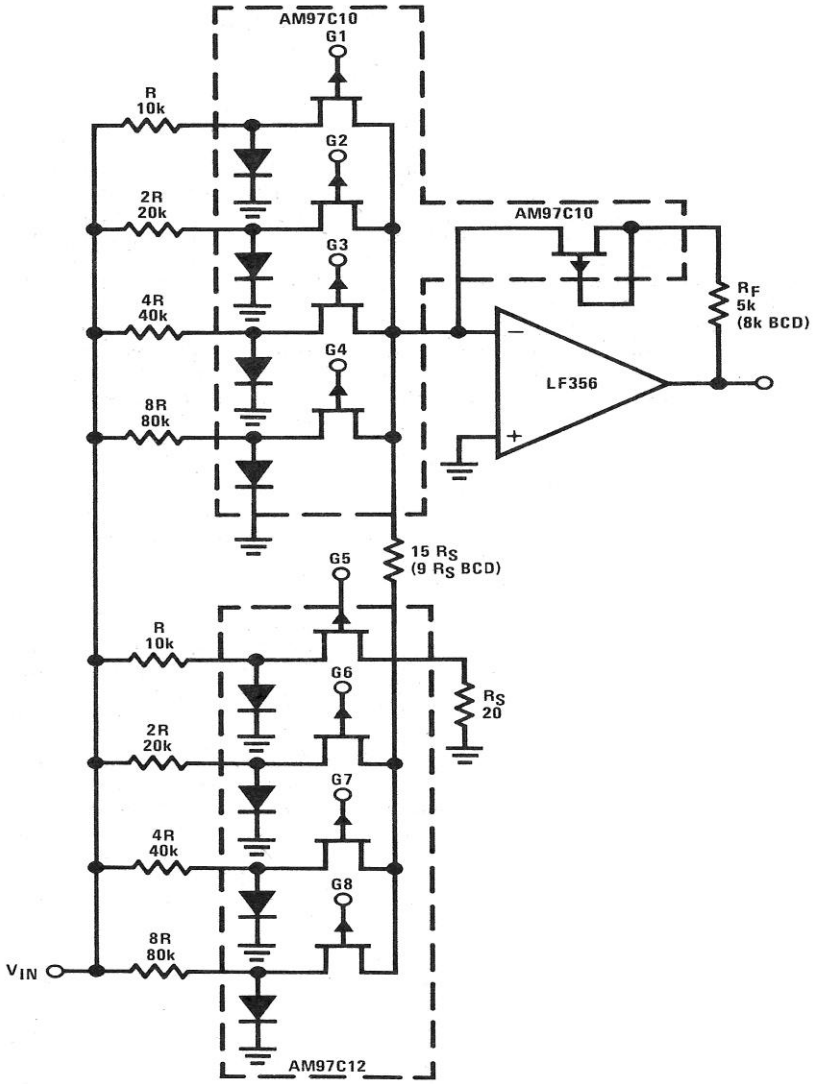


Figure 3. 8-Bit Multiplying D/A Using Cascaded 4-Bit Sections

Binary weighting requires a 1/16 current split for the second switch quad while BCD weighting requires a 1/10 split.

There are two basic switch configurations available that are optimized for a variety of logic drives: TTL or CMOS Multiple independent switches (four by SPST) and a four channel multiplex version with a series compensation JFET.

Practical limitations in using monolithic current mode analog switches need consideration. Resistor values and tolerance impacted by switch resistance is minimized by increasing resistor values without regard, but limits bandwidth and creates leakage errors at elevated temperatures. Using resistors that are too small, increases switch resistance errors. Current saturation (increased switch resistance) occurs when the switch current approaches the JFET saturation current, I_{DSS}. High currents also cause I_G(ON), current lost through the gate, as the diode and JFET source to gate diode become forward biased. An input resistor value of 10 k limits the switch current to less than 2 mA minimizing both leakage and switch resistance problems. For example, the gain accuracy at unity gain using the compensation JFET is less than 0.05% with R = RF = 10 k.

The current shunt resistor used in cascading switches should be kept small to minimize the voltage drop, keeping the JFET drains near ground. Values of R_S should be less than 100 Ω (20 typical).

Resistor tolerance will be determined by converter resolution, i.e., the number if bits (N). For example, an 8-bit binary D/A converter will have 2^N-1 or 255 steps (99 for BCD) or different gains. The resolution or smallest step is (least significant bit) $1/2^N$ of the full-scale value (0.0039). Typical accuracy specifications for D/A converters are stated as 1 LSB or ±1/2 LSB.

This works out to be ±0.2% for the 8-bit binary unit. Errors in the feedback resistor directly affect the output of the converter. The most significant resistor, R, contributes 1/2 full-scale, reducing its error contribution by a factor of 2. The same is true for the rest of the resistors with

contributions of 1/4, 1/8, etc. Using a resistor tolerance of 0.1% for the feedback resistor, 0.2% for the 2 most significant resistors (R, 2R), 0.5% for the 3rd and 1% for the 4th and 5th switches allows 5% resistors to be used in the 6th, 7th and 8th switch positions.

Using the above information, 4-bit or more binary/BCD gain programmable amplifiers can be built with large signal handling capability, few parts and easily adjustable gain or attenuation. Figure 3 shows a practical 8-bit binary/BCD GPA with gains of 0.996 (binary) with R_F = 5 k and 0.99 (BCD) with RF = 8 k. For other gains, only the feedback resistor need be changed.

$$\% \text{ error} = \left[\epsilon_f^2 + \left(\frac{\epsilon_R}{2}\right)^2 + \left(\frac{\epsilon_{2R}}{2^2}\right)^2 + - - - + \left(\frac{\epsilon_{nR}}{2^n}\right)^2 \right]^{1/2}$$

or

$$\% \text{ error} = \left[(0.1)^2 + \left(\frac{0.2}{2}\right)^2 + \left(\frac{0.2}{4}\right)^2 + - - - + \left(\frac{5}{256}\right)^2 \right]^{1/2} = \pm 0.198\% \quad (2)$$

ϵ_f = tolerance of feedback resistor
ϵ_R = tolerance of most significant resistor
ϵ_{nR} = tolerance of Nth resistor

Author: *John Maxwell, Feb 1977*