SG3526

Pulse Width Modulation Control Circuit

The SG3526 is a high performance pulse width modulator integrated circuit intended for fixed frequency switching regulators and other power control applications.

Functions included in this IC are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two high current totem pole outputs ideally suited for driving the capacitance of power FETs at high speeds.

Additional protective features include soft start and undervoltage lockout, digital current limiting, double pulse inhibit, adjustable dead time and a data latch for single pulse metering. All digital control ports are TTL and B–series CMOS compatible. Active low logic design allows easy wired–OR connections for maximum flexibility. The versatility of this device enables implementation in single–ended or push–pull switching regulators that are transformerless or transformer coupled. The SG3526 is specified over a junction temperature range of 0° to +125°C.

- 8.0 V to 35 V Operation
- 5.0 V ±1% Trimmed Reference
- 1.0 Hz to 400 kHz Oscillator Range
- Dual Source/Sink Current Outputs: ±100 mA
- Digital Current Limiting
- Programmable Dead Time
- Undervoltage Lockout
- Single Pulse Metering
- Programmable Soft–Start
- Wide Current Limit Common Mode Range
- Guaranteed 6 Unit Synchronization

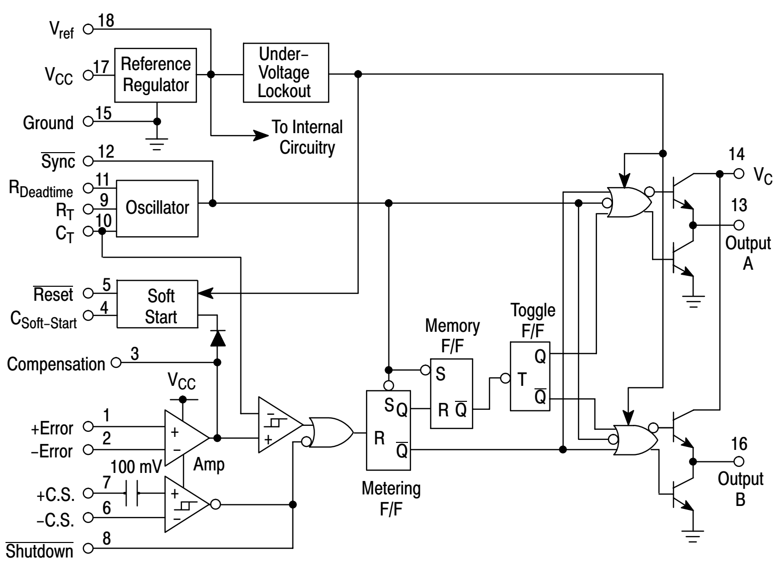

Figure 1. Representative Block Diagram

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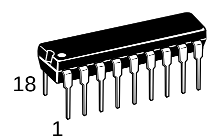
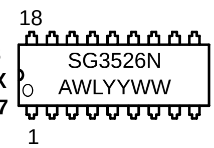
MARKING DIAGRAM

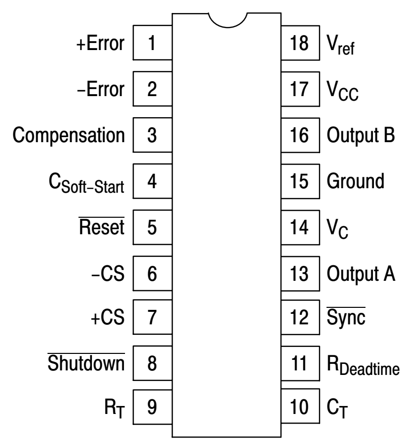


PDIP–18
N SUFFIX
CASE 707



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
SG3526N	PDIP–18	20 Units/Rail

MAXIMUM RATINGS (Note 1.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs		–0.3 to +5.5	V
Analog Inputs		–0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±200	mA
Reference Load Current (V_{CC} = 40 V, Note 2.)	I_{ref}	50	mA
Logic Sink Current		15	mA
Power Dissipation T_A = +25°C (Note 3.) T_C = +25°C (Note 4.)	P_D	 1000 3000	mW
Thermal Resistance Junction–to–Air	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction–to–Case	$R_{\theta JC}$	42	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)	T_{Solder}	±300	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	8.0	35	Vdc
Collector Supply Voltage	V_C	4.5	35	Vdc
Output Sink/Source Current (Each Output)	I_O	0	±100	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.001	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	20	µF
Available Deadtime Range (40 kHz)	–	3.0	50	%
Operating Junction Temperature Range	T_J	0	+125	°C

1. Values beyond which damage may occur.
2. Maximum junction temperature must be observed.
3. Derate at 10 mW/°C for ambient temperatures above +50°C.
4. Derate at 24 mW/°C for case temperatures above +25°C.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, T_J = T_{low} to T_{high} [Note 6.], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION (Note 7.)					
Reference Output Voltage (T_J = +25°C)	V_{ref}	4.90	5.00	5.10	V
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	–	10	30	mV
Load Regulation (0 mA ≤ I_L ≤ 20 mA)	Reg_{load}	–	10	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T$	–	10	–	mV
Total Reference Output Voltage Variation (+8.0 V ≤ V_{CC} ≤ +35 V, 0 mA ≤ I_L ≤ 20 mA)	ΔV_{ref}	4.85	5.00	5.15	V
Short Circuit Current (V_{ref} = 0 V) (Note 5.)	I_{SC}	25	80	125	mA
UNDERVOLTAGE LOCKOUT					
$\overline{\text{Reset}}$ Output Voltage (V_{ref} = +3.8 V)		–	0.2	0.4	V
$\overline{\text{Reset}}$ Output Voltage (V_{ref} = +4.8 V)		2.4	4.8	–	V
OSCILLATOR SECTION (Note 8.)					
Initial Accuracy (T_J = +25°C)		–	±3.0	±8.0	%
Frequency Stability over Power Supply Range (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	–	0.5	1.0	%
Frequency Stability over Temperature (ΔT_J = T_{low} to T_{high})	$\frac{\Delta f_{osc}}{\Delta T_J}$	–	2.0	–	%
Minimum Frequency (R_T = 150 kΩ, C_T = 20 μF)	f_{min}	–	0.5	–	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 0.001 μF)	f_{max}	400	–	–	kHz
Sawtooth Peak Voltage (V_{CC} = +35 V)	$V_{osc}(P)$	–	3.0	3.5	V
Sawtooth Valley Voltage (V_{CC} = +8.0 V)	$V_{osc}(V)$	0.45	0.8	–	V
ERROR AMPLIFIER SECTION (Note 9.)					
Input Offset Voltage (R_S ≤ 2.0 kΩ)	V_{IO}	–	2.0	10	mV
Input Bias Current	I_{IB}	–	–350	–2000	nA
Input Offset Current	I_{IO}	–	35	200	nA
DC Open Loop Gain (R_L ≥ 10 MΩ)	A_{VOL}	60	72	–	dB
High Output Voltage ($V_{Pin\ 1}$–$V_{Pin\ 2}$ ≥ +150 mV, I_{source} = 100 μA)	V_{OH}	3.6	4.2	–	V
Low Output Voltage ($V_{Pin\ 2}$–$V_{Pin\ 1}$ ≥ +150 mV, I_{sink} = 100 μA)	V_{OL}	–	0.2	0.4	V
Common Mode Rejection Ratio (R_S ≤ 2.0 kΩ)	CMRR	70	94	–	dB
Power Supply Rejection Ratio (+12 V ≤ V_{CC} ≤ +18 V)	PSRR	66	80	–	dB

5. Maximum junction temperature must be observed.
6. T_{low} = 0°C T_{high} = +125°C
7. I_L = 0 mA unless otherwise noted.
8. f_{osc} = 40 kHz (R_T = 4.12 kΩ ± 1%, C_T = 0.01 μF ± 1%, R_D = 0 Ω)
9. 0 V ≤ V_{CM} ≤ +5.2 V.

ELECTRICAL CHARACTERISTICS (continued)

Characteristics	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR SECTION (Note 10.)					
Minimum Duty Cycle ($V_{Compensation}$ = +0.4 V)	DC_{min}	–	–	0	%
Maximum Duty Cycle ($V_{Compensation}$ = +3.6 V)	DC_{max}	45	49	–	%
DIGITAL PORTS ($\overline{SYNC}$, $\overline{SHUTDOWN}$, $\overline{RESET}$)					
Output Voltage (High Logic Level) (I_{source} = 40 µA) (Low Logic Level) (I_{sink} = 3.6 mA)	 V_{OH} V_{OL}	 2.4 –	 4.0 0.2	 – 0.4	V
Input Current — High Logic Level (High Logic Level) (V_{IH} = +2.4 V) (Low Logic Level) (V_{IL} = +0.4 V)	 I_{IH} I_{IL}	 – –	 –125 –225	 –200 –360	µA
CURRENT LIMIT COMPARATOR SECTION (Note 12.)					
Sense Voltage ($R_S \le 50\ \Omega$)	V_{sense}	80	100	120	mV
Input Bias Current	I_{IB}	–	–3.0	–10	µA
SOFT–START SECTION					
Error Clamp Voltage ($\overline{Reset}$ = +0.4 V)		–	0.1	0.4	V
$C_{Soft–Start}$ Charging Current ($\overline{Reset}$ = +2.4 V)	I_{CS}	50	100	150	µA
OUTPUT DRIVERS (Each Output, V_C = +15 Vdc, unless otherwise noted.)					
Output High Level I_{source} = 20 mA I_{source} = 100 mA	V_{OH}	 12.5 12	 13.5 13	 – –	V
Output Low Level I_{sink} = 20 mA I_{sink} = 100 mA	V_{OL}	 – –	 0.2 1.2	 0.3 2.0	V
Collector Leakage, V_C = +40 V	$I_{C(leak)}$	–	50	150	µA
Rise Time (C_L = 1000 pF)	t_r	–	0.3	0.6	µs
Fall Time (C_L = 1000 pF)	t_f	–	0.1	0.2	µs
Supply Current ($\overline{Shutdown}$ = +0.4 V, V_{CC} = +35 V, R_T = 4.12 kΩ)	I_{CC}	–	18	30	mA

10. f_{osc} = 40 kHz (R_T = 4.12 kΩ ± 1%, C_T = 0.01 µF ± 1%, R_D = 0 Ω)
11. 0 V ≤ V_{CM} ≤ +5.2 V
12. 0 V ≤ V_{CM} ≤ +12 V

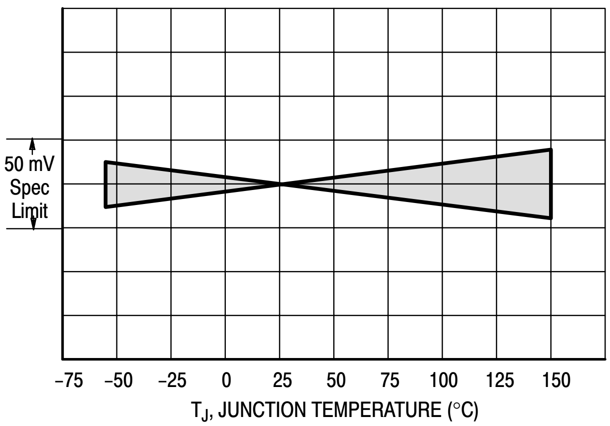


Figure 2. Reference Stability over Temperature

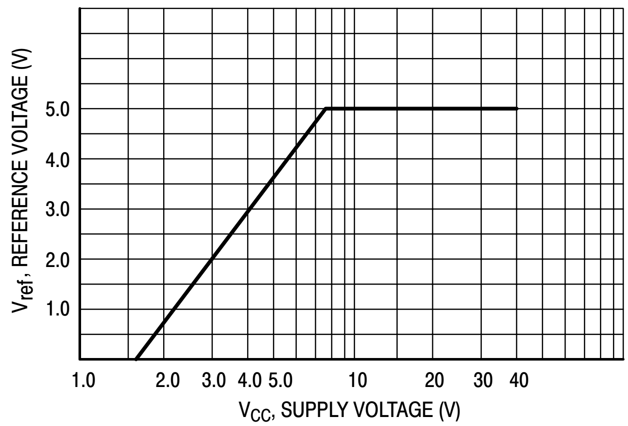


Figure 3. Reference Voltage as a Function Supply Voltage

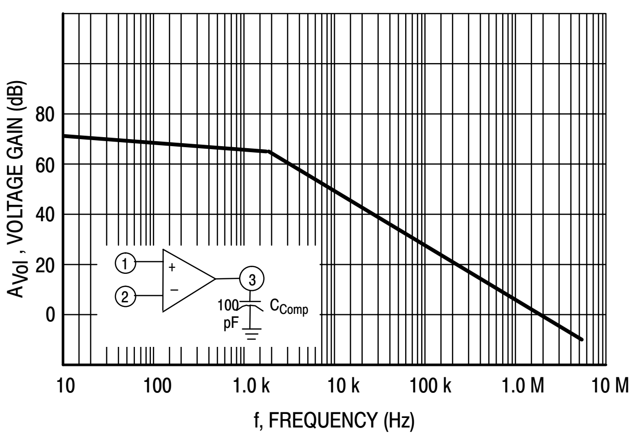


Figure 4. Error Amplifier Open Loop Frequency Response

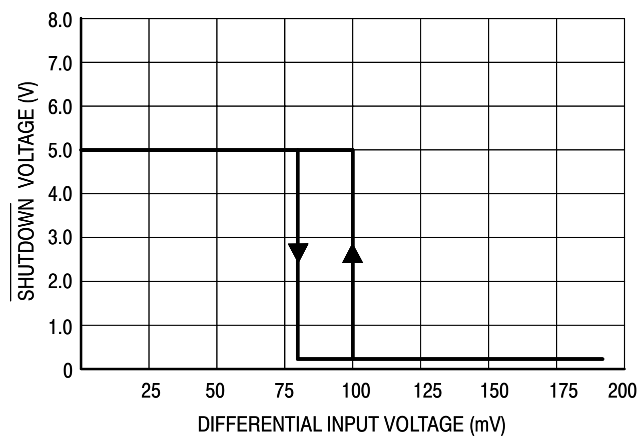


Figure 5. Current Limit Comparator Threshold

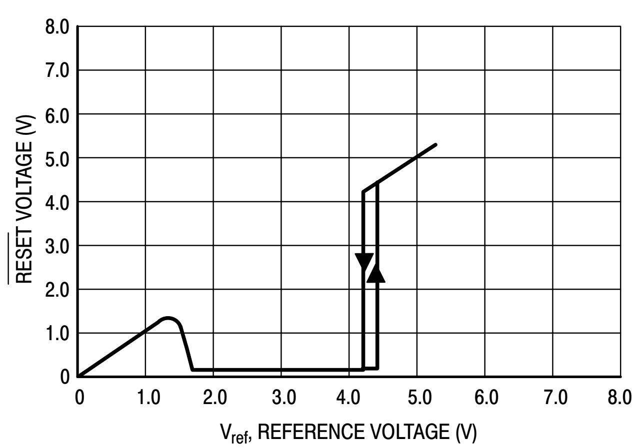


Figure 6. Undervoltage Lockout Characteristic

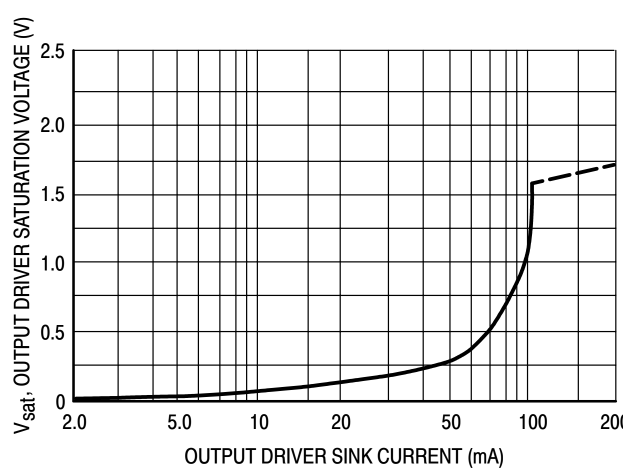


Figure 7. Output Driver Saturation Voltage as a Function of Sink Current

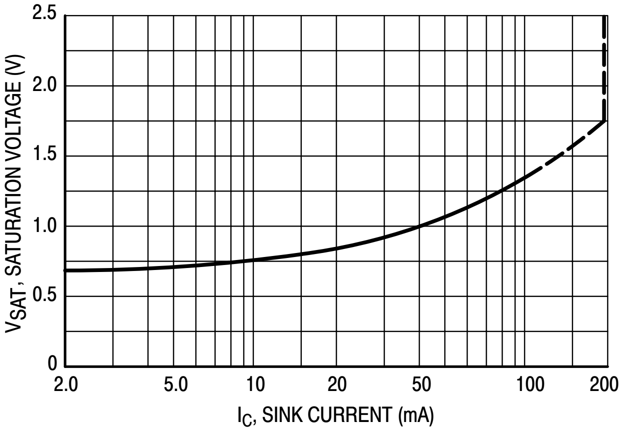


Figure 8. V_C Saturation Voltage as a Function of Sink Current

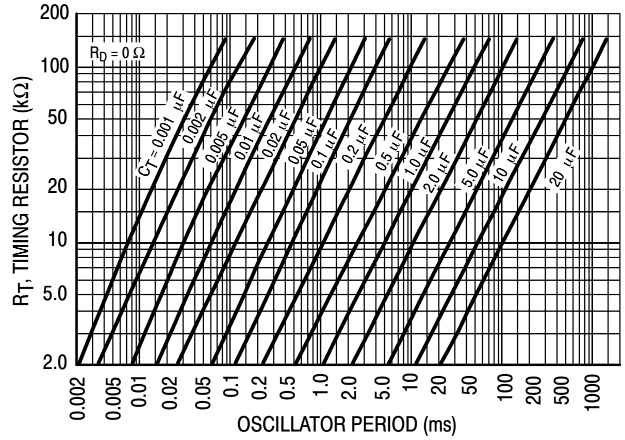


Figure 9. Oscillator Period

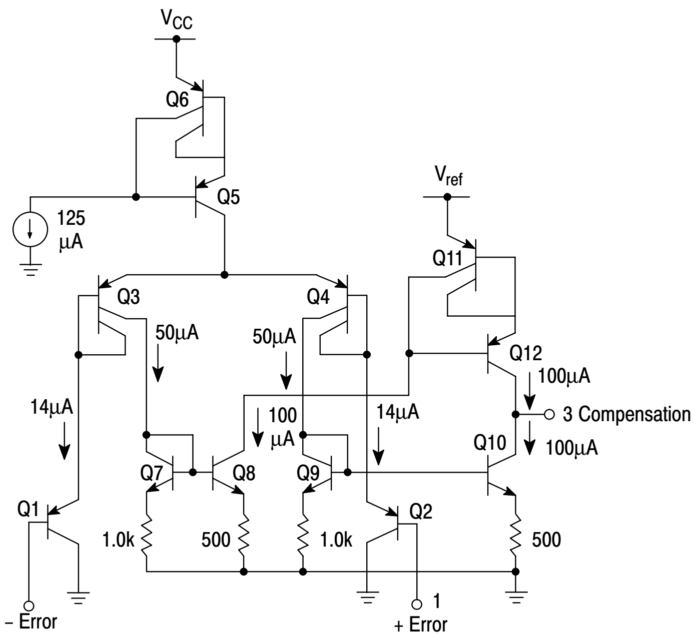


Figure 10. Error Amplifier

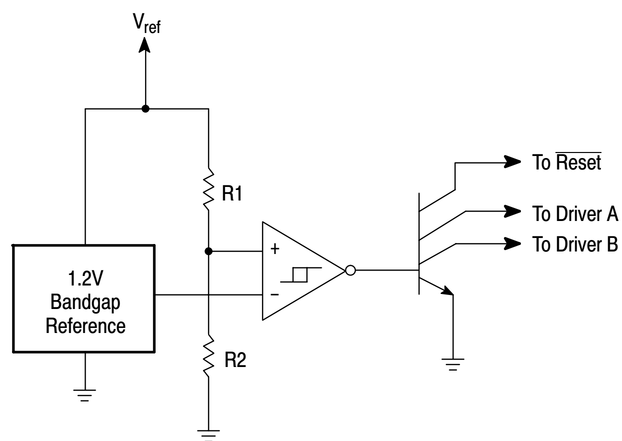
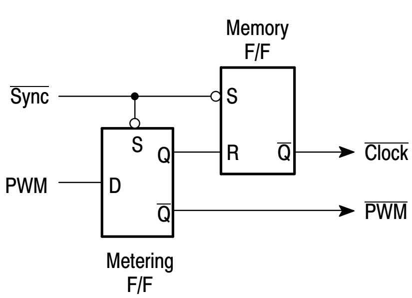


Figure 11. Undervoltage Lockout

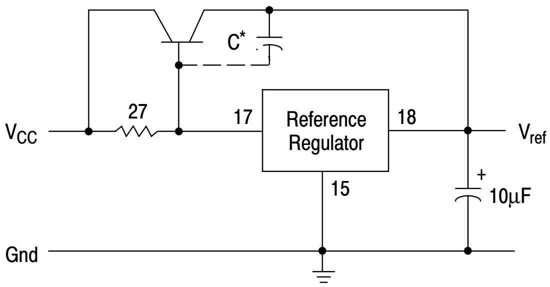


The metering Flip−Flop is an asynchronous data latch which suppresses high frequency oscillations by allowing only one PWM pulse per oscillator cycle.

The memory Flip−Flop prevents double pulsing in a push−pull configuration by remembering which output produced the last pulse.

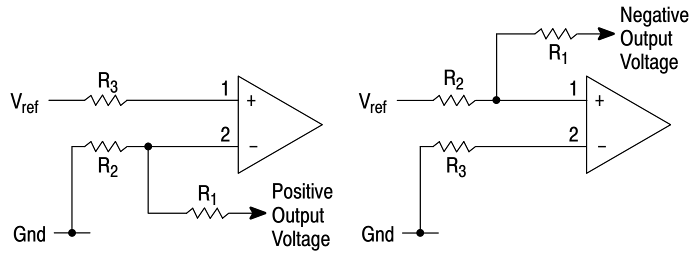
Figure 12. Pulse Processing Logic

APPLICATIONS INFORMATION



* May be required with some types of transistors

Figure 13. Extending Reference Output Current Capability



$$V_{out} = V_{ref}\left(\frac{R_1 + R_2}{R2}\right) \qquad V_{out} = V_{ref}\left(\frac{R_1}{R_2}\right)$$

$$R_3 = \left(\frac{R_1R_2}{R_1 + R_2}\right)$$

Figure 14. Error Amplifier Connections

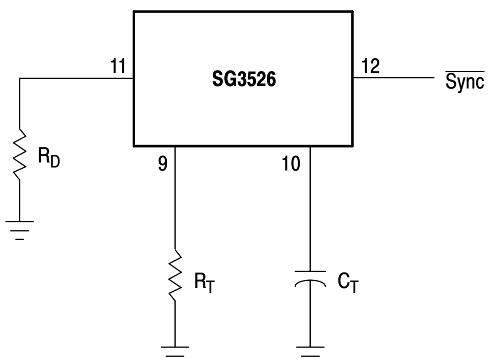
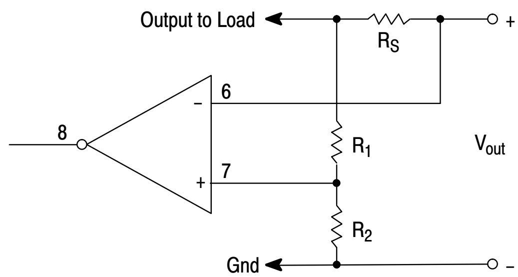


Figure 15. Oscillator Connections



$$I_{(max)} = \frac{\left(0.1\ V + \frac{V_{out}\ R_1}{R1 + R2}\right)}{R_S} \qquad I_{SC} = \left(\frac{0.1\ V}{R_S}\right)$$

Figure 16. Foldback Current Limiting

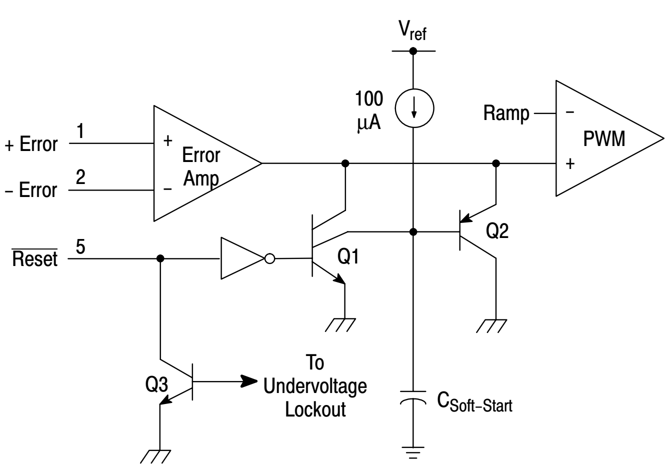
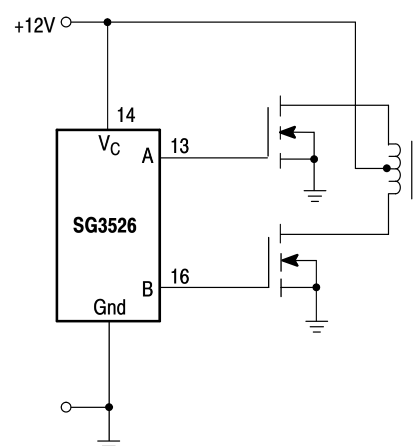


Figure 17. Soft–Start Circuity



The totem pole output drivers of the SG3526 are ideally suited for driving the input capacitance of power FETs at high speeds.

Figure 18. Driving VMOS Power FETs

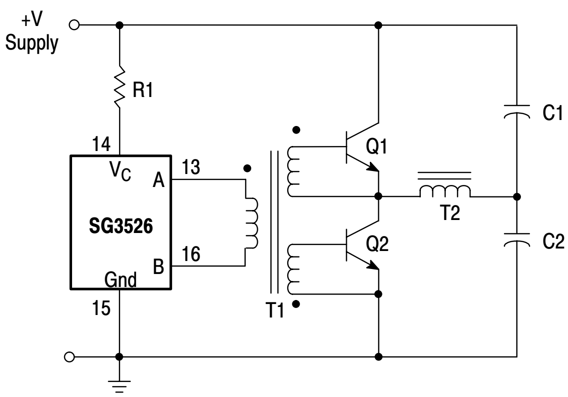
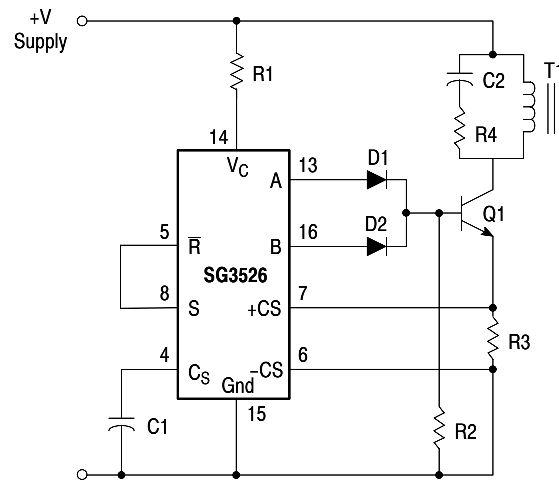


Figure 19. Half–Bridge Configuration



In the above circuit, current limiting is accomplished by using the current limit comparator output to reset the soft–start capacitor.

Figure 20. Flyback Converter with Current Limiting

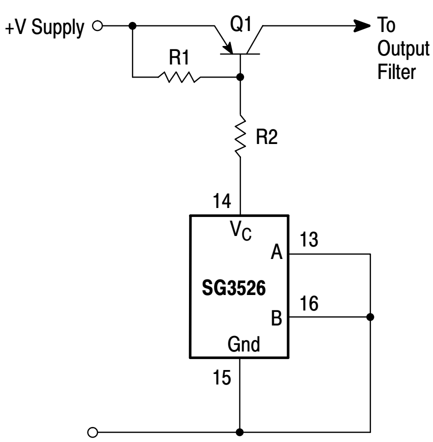


Figure 21. Single–Ended Configuration

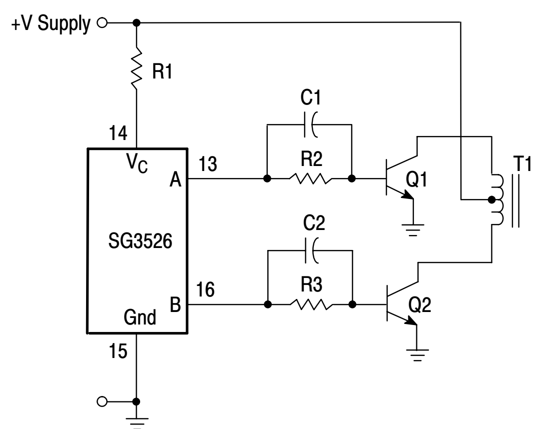
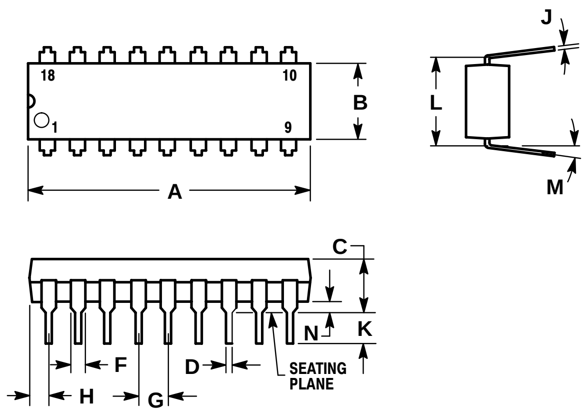


Figure 22. Push–Pull Configuration

PACKAGE DIMENSIONS

PDIP–18
N SUFFIX
CASE 707–02
ISSUE D



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.875	0.915	22.22	23.24
B	0.240	0.260	6.10	6.60
C	0.140	0.180	3.56	4.57
D	0.014	0.022	0.36	0.56
F	0.050	0.070	1.27	1.78
G	0.100 BSC		2.54 BSC	
H	0.040	0.060	1.02	1.52
J	0.008	0.012	0.20	0.30
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.02

Notes

Notes

PUBLICATION ORDERING INFORMATION

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Toll Free from Hong Kong & Singapore:
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Email: ONlit–asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
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