VMMK-1218 Application Note

Using the VMMK-1218 Wafer Scale Packaged Enhancement Mode PHEMT in a 10 GHz Low Noise Amplifier

Application Note 5408

Introduction

The VMMK-1218 is a low noise 400 u gate width device using Avago Technologies industry leading Enhancement mode PHEMT technology housed in an ultra miniature 0402 chip scale package.

At 10 GHz, when the VMMK-1218 is biased at a Vds of 3V and 20 mA the device will produce an approximate 0.8 dB Fmin with typically 11 dB of associated gain. This application note describes the use of the VMMK-1218 in two 10 GHz low noise amplifiers. One LNA is optimized for lowest noise figure and best output return loss. The second amplifier is optimized for best input and output return loss. A schematic diagram describing the two amplifiers is shown in Figure 1.

The design makes use of microstripline matching on low loss RO4350 .010" thickness printed circuit board. The input matching network can be optimized for lowest noise figure or best input return loss. The output matching network is generally matched for best return loss, however, output match can also effect P1dB and OIP3.

Biasing

The VMMK-1218 is biased at a Vds of 3V and 20 mA which provides a low noise figure coincident with good linearity. The VMMK-1218 can be easily re-biased to improve gain and or power output. Application Note 5385 covers the topic of biasing in great detail. Referencing Figure 1, resistor R1 and R2 set the gate voltage for the desired drain current. Resistor R3 is multifunctional in that it affects both dc and RF operation of the FET. Resistor R3 is quite often used to drop the power supply voltage Vdd down to a lower Vds desired by the VMMK-1218. In addition R3 is used to de-Q the bypass capacitors used in the drain decoupling network. Due to the inherent series parasitic inductance of most bypass capacitors, paralleling capacitors without any de Qing resistance quite often produces parallel resonances which can adversely affect an amplifier's stability. Typical values for de-Qing range between a few ohms and 50 to 100 ohms. The LNA design presented in this application uses a 10Ω resistor for R3 which will require a nominal Vdd of 3.2V. For other supply voltages such as 5V, an additional resistor can be inserted between the demo board Vdd terminal and the power supply. The total current draw is approximately 20.5 mA with the addition 0.5 mA being consumed by bias resistors R1 and R2. The value of the additional resistor is calculated based on the voltage drop divided by the LNA current consumption.

Design Tradeoffs

Designing a single stage low noise amplifier requires paying attention to many key points.

- Noise Figure
- Gain
- Input and output match.
- Stability both in-band and out-of-band
- P1dB and IP3

This LNA was optimized using Avago Technologies Advanced Design System (ADS) using the published S and Noise parameters from the Avago Technologies Web Site. This allows the designer to balance the tradeoffs between noise figure, gain, input return loss, output return loss, and stability with a linear simulator. Optimizing an LNA for P1dB and / or IP3 requires the use of the nonlinear model which can be used as a next step in trying to optimize linearity. Generally optimizing for linearity will require some compromise in output or input match and sometimes even stability. However, the linear simulator will provide the best overall first step in any successful LNA design.

Circuit Topology

Since our primary objective with this design is to achieve a low noise figure, it is most important to attempt to provide a noise match to the device.

Achieving the lowest noise figure possible from a device requires matching the input of the device to an impedance represented by Γo. Γo for the VMMK-1218 when biased at a Vds of 3V and Ids of 20 mA is .27 @ 143 degrees.

The input matching network consists of a series capacitor shown as C1 and a small length of transmission line between the capacitor and the VMMK-1218. Additional stubs which are actually open circuited transmission lines act as small values of capacitance which help tune the higher frequency networks. These are shown as stubs S1 and S2. The low noise version shown in Table 1 does not use S1 but does require a small amount of stub length at S2. The gain matched version does not use S2 but rather uses a small amount of stub at S1 to provide a better input return loss. In a single stage amplifier, obtaining a low noise match and good input return loss simultaneously is very difficult. More on this later.

Once the input network has been optimized for best noise figure, then the output network is optimized for best gain over the desired bandwidth. Since the input match is a noise match rather than a gain match, it will be impossible to obtain the MSG or MAG that the device is capable of. Instead, the goal would be Ga which is the associated gain at minimum noise figure. In the case of the VMMK-1218 biased at 3V and 20ma Ids, Ga is approximately 10.8 dB. Providing a gain match at the output will provide optimum gain coincident with good S22.

The output matching network consists of a series capacitor C2 and a small length of transmission line tuned with a small open circuited stub shown as S4 which acts as a small value of shunt capacitance. The stub shown at S3 on the original demo board is not used. Two different versions of the output network were analyzed. One provides slightly better P1dB and the other provides slightly higher OIP3.

The bias decoupling on both the gate and drain is accomplished by using shunt microstripline inductors that are "RF" bypassed with a trapezoidal type open circuited microstrip stub on the gate circuit and a small value 1 pF bypass capacitor on the drain circuit. The trapezoidal stub is approximately a quarter wave in length so that the open circuited stub presents a low impedance to the shunt bias decoupling stub providing an effective bias decoupling network at the frequency of operation. This form of bypass is often preferred over the use of a small value chip capacitor as it provides a low loss bypass capacitor with its only limitation possibly being its size. At 10 GHz, the length is only on the order of .100" There is no real preference on one type of bypass over the other at 10 GHz except that as one goes higher in frequency it may be easier to make a good bypass capacitor out of a trapezoidal stub than trying to find a low value bypass capacitor with low associated inductance.

The addition of R3, C5, C6 and R4, C3 provide low frequency resistive stabilization for the both the drain and gate of the VMMK-1218. As mentioned before the series resistors R3 and R4 also provide a way to de-Q or minimize the interaction between two bypass capacitors. Resistors R3 and R4 also become important for linearity as they also provide a termination for the difference signal that is introduced when performing 2 tone 3rd order IP3 tests.

Demo Board Performance

The generic demo board biases the VMMK-1218 at a Vds of 3V and an Ids of 20 mA. The measured noise figure performance of both versions of the completed VMMK-1218 demo boards is shown in Figure 3. The loss of the input network has been measured at 0.3 dB at 10 GHz which places the noise figure of the VMMK-1218 device by itself at about 0.7 dB which corresponds to the published fmin of the device. ADS predicts an optimistic 0.82 dB noise figure of the noise matched circuit. The second demo board which was matched for better input return loss and gain shows a 1.15 dB noise figure.

Figure 4 shows an S Parameter analysis of the VMMK-1218 amplifier. The plots show a comparison between measured demo board performance and performance as predicted by ADS. The VMMK-1218 amplifier has a measured gain of 10.8 dB which compares well with the ADS predicted value of nearly 11dB gain. The measured input return output loss is -5.8 dB which is actually better than the ADS predicted -4.5 dB input return loss. The measured output return loss of -14.1 dB compares favorably with the ADS predicted -14.5 dB output return loss. The S parameters are also used to calculate mu and K which are 2 important parameters that can help predict an amplifier's stability. Both the ADS simulated K and mu predict unconditional stability as well as the calculated results based on demo board measured data.

A 2 stage version using this circuit as a basic building model can be optimized to provide a 1 dB noise figure, 20 dB gain block with good output and input return loss. In a multistage amplifier, the high pass structure of the bias decoupling network can be optimized to further roll off the low frequency gain and then the output of the second stage can then be rematched to provide the desired S22. The interstage network can also be used to improve input return loss and enhance stability. A 2 stage amplifier will be the subject of a future application note.

The VMMK-1218 amplifier was also tested for OIP3 and P1dB at 10 GHz. Vds was set at 3V and measurements were made at an Ids of 20 mA and 25 mA. The results are shown in Table 3. The gain matched LNA with approximate -10 dB input and output return loss provides higher OIP3 +29 to +30 dBm vs +27 to +28 dBm for the noise matched LNA that has a -14 dB output return loss. However, the noise matched LNA with the -14 dB output return loss provides higher P1dB. The noise matched LNA provides a +17 to +18 dBm P1dB vs +15 to +17 dBm for the gain matched LNA.

Drain efficiencies of approximately 30% to 40% at P1dB and 40% to 50% at P3dB are possible by using a passive bias network that allows the device to be driven from class A to class AB. As shown in Table 3, the drain current does increase from its quiescent value as the device is driven to P1dB and beyond. Biasing the device in an active bias configuration will then limit its ability to provide the P1dB mentioned in this ap note.

OIP3 was measured at a signal spacing of 5 MHz. Measuring intercept point accurately requires a good power divider with isolators on both ports to combine the two signal sources. It is important to minimize reciprocal mixing within the two signal generators as any mixing or doubling of the frequency of the two signal generators will produce 2F1 and 2F2 which will only enhance the generation of the undesired third order products. A 3 dB attenuator at the input of the spectrum analyzer will also provide a better broad band load for the LNA.

Conclusion

The VMMK-1218 10 GHz demo board has been shown to provide a nominal 1 dB noise figure with nearly 11 dB of associated gain, a P1dB of +14 to +16 dBm and an OIP3 as high as +30dBm.

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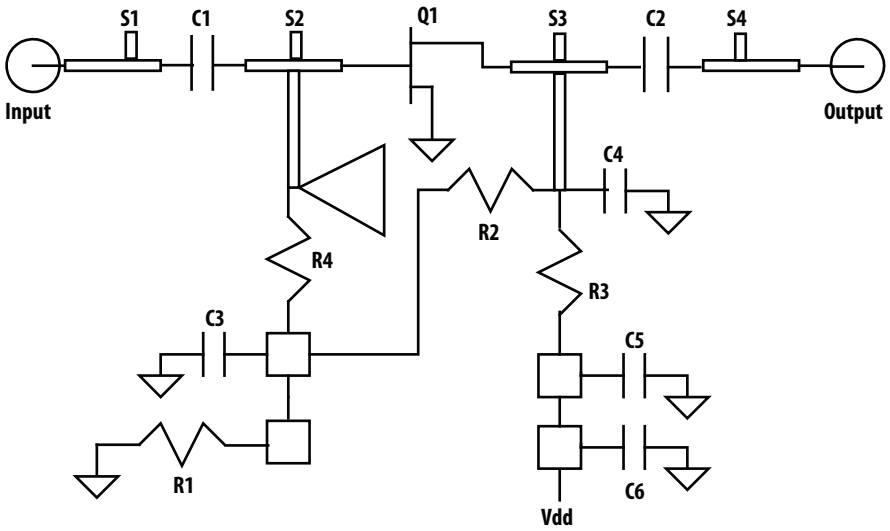

Figure 1. Schematic Diagram of 10 GHz VMMK-1218 Amplifier

Table 1. LNA component parts list for low noise version

C1	0.5 pF 0402 chip capacitor – ATC 600L 0R5BT
C2	0.8 pF 0402 chip capacitor - ATC 600L 0R8BT
C3,C5	1000 pF 0402 chip capacitor – Garrett 04022R102K9B200
C4	1 pF 0402 chip capacitor - ATC 600L 1R0BT
C6	0.1 uF 0402 chip capacitor – Kyocera – AVX0402YG104ZAT2A
R1	1.3 KΩ 0402 chip resistor – KOA RK73B1ETTP132J
R2	6.2 KΩ 0402 chip resistor – KOA RK73B1ETTP622J
R3	10 Ω 0402 chip resistor – Garrett MCR01J100E
R4	51 Ω 0402 chip resistor – Garrett MCR01J510E
Q1	Avago Technologies VMMK-1218
S1	Stub not used
S2	Stub - .030" wide by .030" long, used for fine tuning S11 vs NF
S3	Stub not used
S4	Stub - .030" wide by .035" long, edge placed .035" from C2

Table 2. LNA component parts list for gain matched version

C1	0.5 pF 0402 chip capacitor – ATC 600L 0R5BT
C2	0.5 pF 0402 chip capacitor - ATC 600L 0R5BT
C3,C5	1000 pF 0402 chip capacitor – Garrett 04022R102K9B200
C4	1 pF 0402 chip capacitor - ATC 600L 1R0BT
C6	0.1 uF 0402 chip capacitor – Kyocera – AVX0402YG104ZAT2A
R1	1.3 KΩ 0402 chip resistor – KOA RK73B1ETTP132J
R2	6.2 KΩ 0402 chip resistor – KOA RK73B1ETTP622J
R3	10 Ω 0402 chip resistor – Garrett MCR01J100E
R4	51 Ω 0402 chip resistor – Garrett MCR01J510E
Q1	Avago Technologies VMMK-1218
S1	Stub - .030" wide by .040" long, edge placed .060" from C1
S2	Stub not used
S3	Stub not used
S4	Stub - .030" wide by .035" long, edge placed .060" from C2

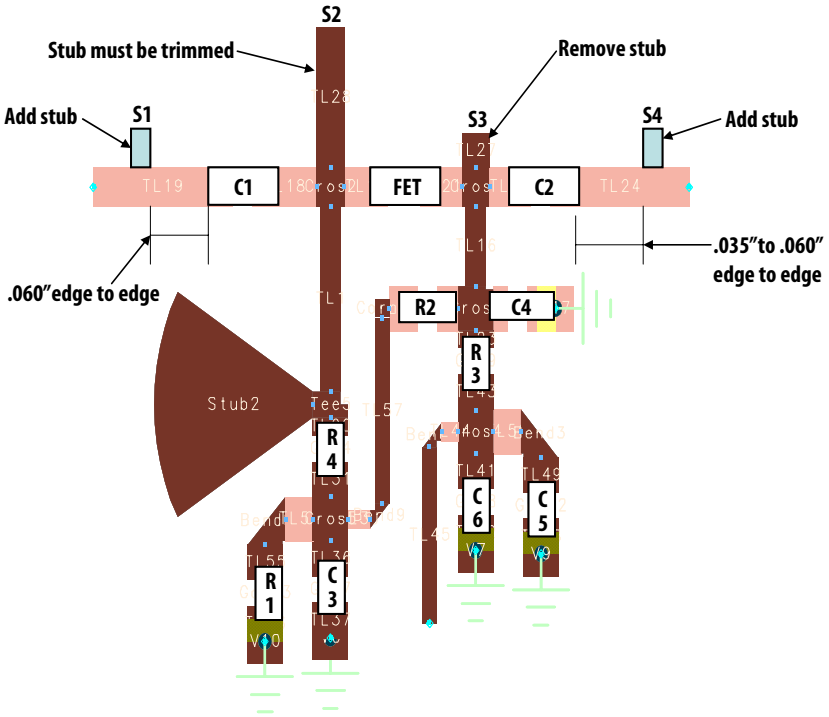

Figure 2. Changes to Original VMMK-1218 10 GHz demo board – see text for information on the use of stubs for tuning

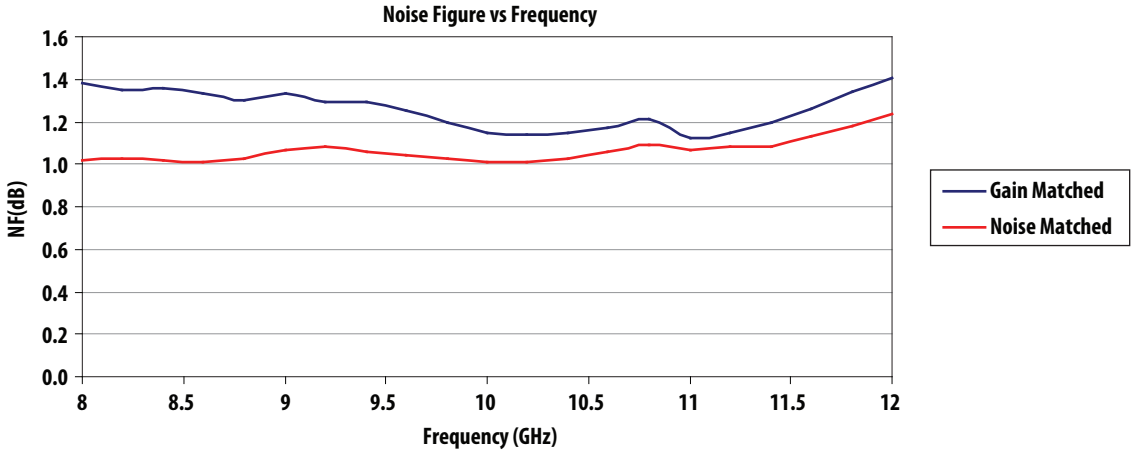

Figure 3. VMMK-1218 Demo Board Noise Figure vs Frequency. The loss of the input portion of the demo board is about 0.3 dB at 10 GHz. ADS predicts an LNA noise figure of 0.82 dB for the noise matched condition.

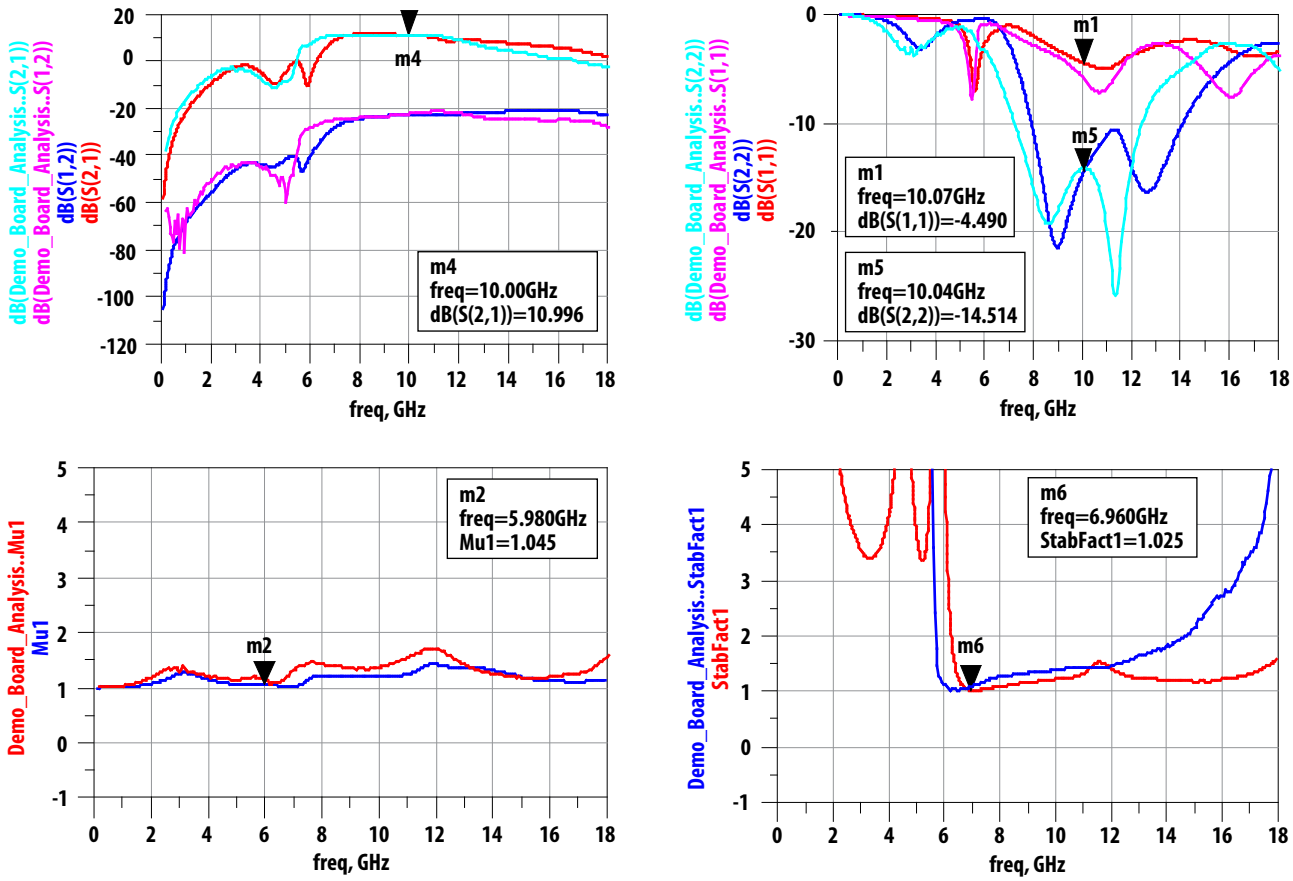

Figure 4. VMMK-1218 Demo Board S Parameter Analysis showing comparison of the demo board performance vs ADS predicted performance. The markers represent the ADS simulated performance.

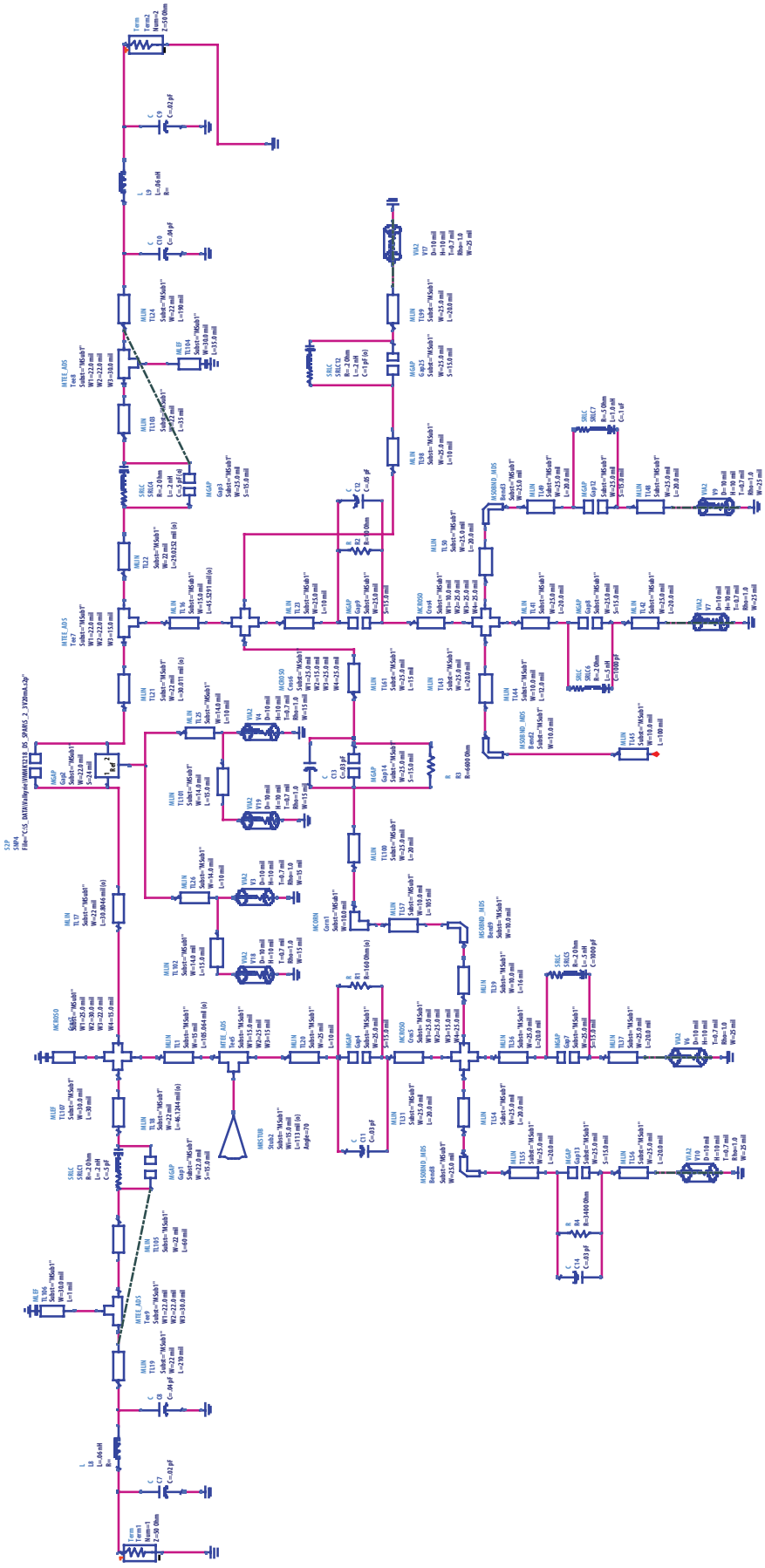

Figure 5. ADS Circuit for 10 GHz VMMK-1218 Amplifier

Table 3. VMMK-1218 10 GHz Demo board power output performance

Configuration	Bias Vds=3V	P1dB (dBm)	Ids (mA) @P1dB	Efficiency	P3dB (dBm)	Ids@P3dB	Efficiency	OIP3 (dBm)
Gain Matched	Idsq=20mA	+15.0	35.0	30.1%	+17.6	44.1	43.5%	+29
Cout=0.5pF	Idsq=25mA	+16.7	41.1	37.9%	+17.7	44.8	43.8%	+30.8
Noise matched	Idsq=20mA	+17.0	37.3	44.8%	+18.0	41.0	51.3%	+27.0
Cout=0.8pF	Idsq=25mA	+17.1	38.4	44.5%	+18.0	41.8	50.3%	+28.0

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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