AN1184
APPLICATION NOTE

BU808DFI IN THE HORIZONTAL DEFLECTION STAGE

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1. INTRODUCTION

The purpose of this application note is to give the TV designer the simple tools, when the Darlington solution is used in the horizontal deflection stage. Generally this transistor is specifically designed for low cost CTV, in the range of 14” to 21” screen size.

The features are:
- High voltage capability
- Improved ruggedness
- Fully insulated package

The benefits are:
- Easy to drive
- Few external components needed
- Low power dissipation

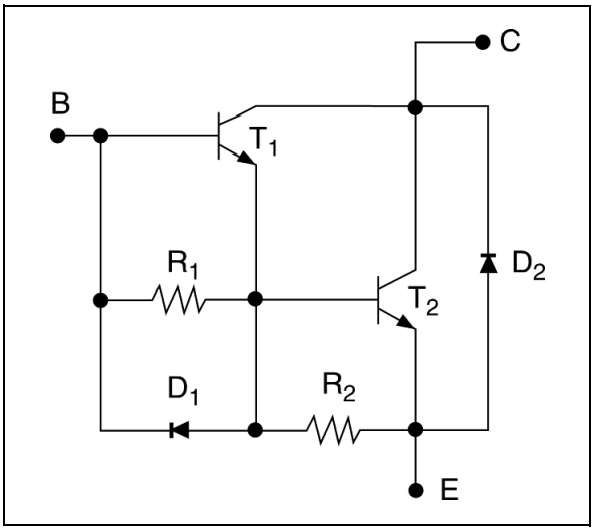

Figure 1. BU808DFI monolithic solution.

2. BU808DFI: DARLINGTON INTEGRATED CIRCUIT.

The part number BU808DFI is a monolithic Darlington solution that matches and optimizes the above mentioned parameters. This device is designed and manufactured by STMicroelectronics in multi-epitaxial mesa technology with a hollow emitter fast switching structure. In addition, the Damper diode D_2 is built-in, consequently no external diodes are needed when the 90° CRT is used. Figure 1 shows the schematic diagram of the Monolithic Darlington BU808DFI.

2.1. Horizontal Deflection Stage.

In this paragraph we describe how to use the BU808DFI in the horizontal deflection stage. Figure 2 shows the schematic diagram of the horizontal deflection circuit, where L_y represents the horizontal line yoke and C_f the resonant flyback voltage capacitor.

R_{BB}, C_{BB} and STX112 are the base drive components. Compared to a traditional base drive transformer, the circuit BU808DFI is much simpler, easier to drive, more compact and because it employs just a few external components it is more cost effective.

In the following sections we will analyze the input and output parts of the circuit separately, when the BU808DFI is in on/off phase.

2.2. Horizontal Deflection Output Circuit.

In order to simplify the calculations we will analyze the horizontal deflection output circuit, without taking into consideration the losses of the flyback voltage capacitor C_f.

2.2.1. When The BU808DFI Is On.

In the above mentioned condition, applying Kirchhoff's law at the output network, when the STX112 is cut-off, we can write the following equation:

$$V_{CC} = r_y I_C + L_y \frac{dI_C}{Dt} + V_{CE(sat)} \quad \textbf{(A)} \qquad \text{normally,} \quad \Delta t_{(on)Darlington} \leq \frac{L_y}{r_y} \quad \textbf{(B)}$$

so, the eq. **(A)** becomes: $V_{CC} = r_y I_{CP} + L_y \frac{I_{CP}}{t_{(on)}} + V_{CE(sat)}$ **(C)**

and $t_{(on)Darlington} = \frac{L_y \cdot I_{CP}}{V_{CC} - [r_y I_{CP} + V_{CE(sat)}]}$ **(D)**

Where, $t_{(on)Darlington}$ represents the time collector current to reach the maximum peak I_{CP}.

2.2.2. When The Damper Diode Is On.

Applying Kirchhoff's law at the output network in the same conditions of the previous paragraph, we have:

$$V_{CC} = r_y I_D + L_y \frac{dI_D}{Dt} + V_D \quad \textbf{(E)} \qquad \text{normally,} \quad t_{(on)Damper} \leq \frac{L_y}{r_y} \quad \textbf{(F)}$$ so, eq. **(E)** becomes

$$V_{CC} = r_y I_D + L_y \frac{I_{DP}}{t_{(on)}} + V_D \quad \textbf{(G)} \qquad \text{and} \quad t_{(on)Damper} = \frac{L_y \cdot I_{DP}}{V_{CC} - [r_y I_D + V_D]} \quad \textbf{(H)}$$

Where $t_{(on)Damper}$ represents the time of the damper diode current to reach the maximum peak I_{DP}.

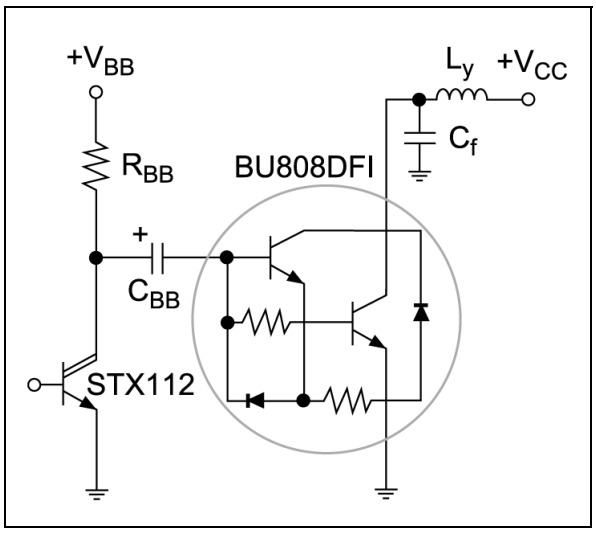

Figure 2. Complete horizontal deflection circuit with BU808DFI Darlington.

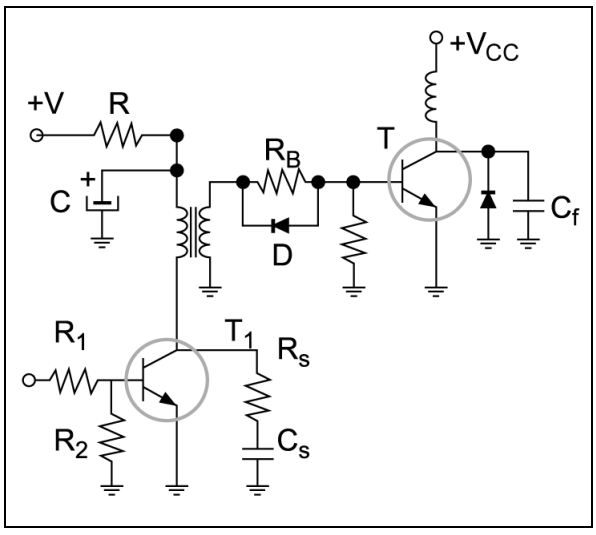

Figure 3. Traditional horizontal deflection circuit with transistor.

3. HORIZONTAL DEFLECTION INPUT CIRCUIT.

In order to simplify the calculations we will analyze the horizontal deflection input circuit, without taking into consideration the losses of the power supply V_{BB}.

3.1.1. R_{BB} Calculation.

With reference to the input circuit shown in figure 2, we can write:

$$V_{BB} = R_{BB} \cdot I_{B(on)} + [V_{C(average)} + V_C(t)] + V_{BE(sat)} \quad \textbf{(I)}$$

$$V_{BB} = R_{BB} \cdot \frac{I_{CP}}{H_{FE(forced)}} + [V_{C(average)} + V_C(t)] + V_{BE(sat)} \quad \textbf{(J)}$$

Where, $V_C(t)$ is the capacitor voltage ripple, $V_{C(average)}$ is the average voltage across the capacitor C_{BB}, and $H_{FE(forced)} = \frac{I_{CP}}{I_{B1}}$ is the H_{FE} forced.

From the eq. **(J)** it is possible to calculate the R_{BB}, in fact

$$R_{BB} = \frac{V_{BB} - [V_{C(average)} + V_C(t) + V_{BE(sat)}]}{I_{CP} / H_{FE(forced)}} \quad \textbf{(K)}$$

3.1.2. Power Dissipation On The R_{BB}.

In order to minimize the power dissipation on the R_{BB} it is advisable to split it into resistors ($R_{BB}/2$). When the STX112 is off, the power dissipation on the resistor R_{BB} is given by the following equation

$$P_{BB} = \frac{R_{BB}}{2} \cdot I_{B(on)}^2 \cdot D \quad \textbf{(L)}$$

where D is the duty cycle. Instead, when the STX112 is on, we have

$$P_{BB} = \frac{[V_{BB} - V'_{CE(sat)}]^2}{\frac{R_{BB}}{2}} \cdot (1 - D) \quad \textbf{(M)}$$

So, the total power dissipation on the resistor is:

$$P_{BB} = \frac{R_{BB}}{2} \cdot I^2_{B(on)} \cdot D + \frac{[V_{BB} - V'_{CE(sat)}]^2}{2 \cdot R_{BB}} \cdot (1 - D) \quad \textbf{(N)}$$

3.1.3. C_{BB} Calculation.

During the no picture phase the Darlington must be completely off, in order to avoid the reconduction phenomenon. Usually, the safety margin for $V_{BE(off)}$ must be greater or equal to 2V. So, the average voltage $V_{C(average)}$ across the capacitor C must be necessarily greater than 2V, because we must take into account the STX112 maximum saturation voltage $V'_{CE(sat)}$ at $I'_{C(sat)}$. The capacitor voltage ripple $V_C(t)$ must be a percentage variation of the average voltage $V_{C(average)}$. In any case the maximum voltage ripple must guarantee that the negative base-emitter voltage must be below zero during the flyback voltage.

r_C represents the series resistor leakage of the capacitor C_{BB}.

$$V_{C(average)} = V'_{CE(sat)} - V_{BE(off)} \quad \textbf{(O)}$$

$$V_C(t) = V_{C(average)} \exp -\left(\frac{Th}{\tau}\right) \quad \textbf{(P)} \qquad C = \frac{Th}{r_C} \cdot Ln^{-1}\left(\frac{V_{C(average)}}{V_C(t)}\right) \quad \textbf{(Q)}$$

4. HORIZONTAL DEFLECTION TIMING

The collector current I_C, Damper diode current I_D, yoke current and the flyback voltage $V_{Cflyback}$ waveforms are shown in figure 4.

The horizontal period T_h is the sum of the scanning time t_s and flyback time $t_{flyback}$.

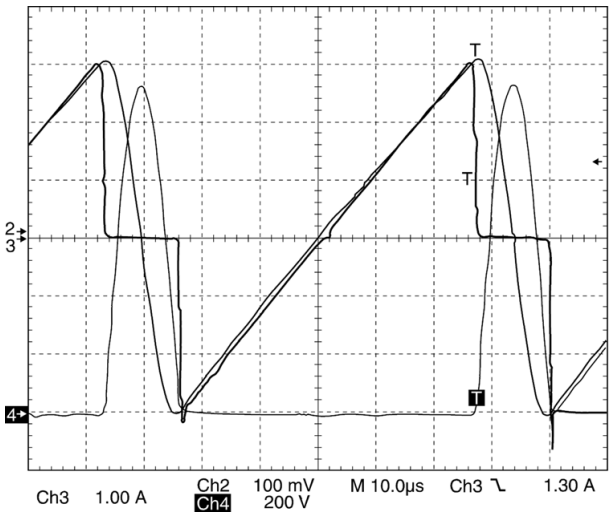

Figure 4.

$$T_h = t_s + t_{flyback} \quad \textbf{(R)}$$

where, $t_s = [t_{(on)Darlington} + t_{storage} + t_{fall}] + t_{(on)Damper}$ **(S)**

$t_{flyback} = \pi\sqrt{L_y C_f}$ **(T)** .If we assume that $t_{(on)Darlington}$ and $t_{(on)Damper}$ are very close,

we can write: $T_h = \dfrac{2 \cdot L_y \cdot I_C}{V_{CC} - [r_y I_C + V_{CE(sat)}]} + (t_{storage} + t_{fall}) + \pi\sqrt{L_y C_f}$ **(U)**

therefore, $(t_{storage} + t_{fall})max \leq \left[T_h - \left(\dfrac{2 \cdot L_y \cdot I_{CP}}{V_{CC} - [r_y I_{CP} + V_{CE(sat)}]} + \pi\sqrt{L_y C_f}\right)\right]min$ **(V)**

The last inequality **(V)** gives the important result:

The maximum value measured from the sum of the storage time t_s and fall time t_f of the Darlington, must be less or equal to the right hand side of the inequality given above. The term on the right hand side is given by calculation as all the parameters are defined.

Usually, with a fixed I_{Bon} the criteria adopted to guarantee the eq. **(V)** is to adjust the slope and amplitude of the reverse current base I_{Boff}.

5. EXAMPLE OF DESIGN-IN OF BU808DFI IN TYPICAL APPLICATION CONDITIONS.

The aim of this section is to apply the previous formulas in a real application. The values of R_{BB} and C_{BB} will be calculated in order to minimize the switching power losses of the Darlington, when the design output circuit specifications are already fixed.
The PAL system will be taken as an example in this investigation; obviously the same analysis could be extended to other standard systems (SECAM, NTCS, etc.). As known, in the PAL system the frequency is 15625 Hz, so the period is 64 µsec, see figure 5.

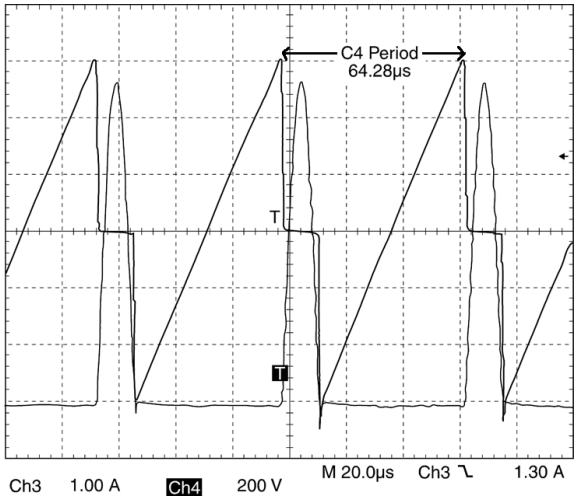

Figure 5.

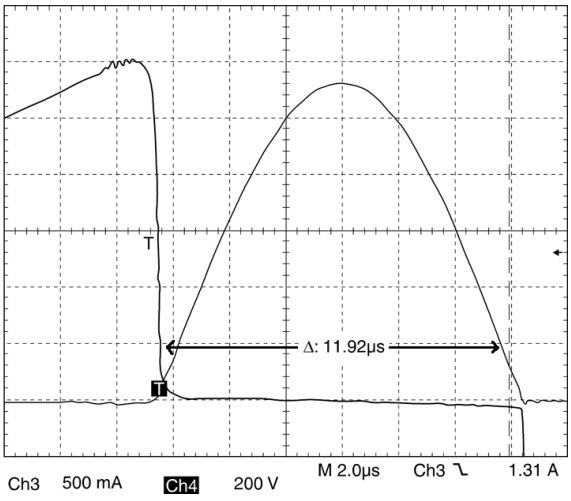

Figure 6.

From the eq. **(T)** we can calculate the retrace time: $t_{flyback} = \pi\sqrt{1.2mH \cdot 12nF} = 11.92\mu s$
Figure 6 shows the retrace time during the flyback phase.

Design-in specifications

Output passive components values:

- yoke inductance value L_y=1.20mH
- yoke resistance series value r_y=0.40Ω
- flyback capacitance value C_R=12.00nF

BU808DFI working point:

- collector current peak I_{CP}=3.00A
- flyback voltage saturation $V_{flyback}$=1.125kV
- collector-emitter voltage saturation $V_{CE(sat)}$=1.00V @ 3A/0.1A
- base-emitter voltage saturation $V_{BE(sat)}$=1.50V @ 3A/0.1A

STX112 working point:

- collector current peak I'_{CP}=2.20A
- collector-emitter voltage saturation V'_{CE}(sat)=0.70V @ 2.2A/0.01A

External power supply:

- output p.s. value V_{CC}=146.00V
- input p.s. value V_{BB}=12.00V

Now, it is possible to calculate the maximum value for the sum ($t_{storage} + t_{fall}$), in fact, from the eq. **(V)**

$$(t_{storage} + t_{fall})max \leq \left[T_h - \left(\frac{2 \cdot L_y \cdot I_{CP}}{V_{CC} - [r_y I_{CP} + V_{CE(sat)}]} + \pi\sqrt{L_y C_f}\right)\right]min$$

$$(t_{storage} + t_{fall})max \leq 64\mu s - (50\mu s + 11.92\mu s) \qquad (t_{storage} + t_{fall})max \leq 2.08\mu s$$

Figures 7, 8 and 9 show the $t_{on(Darlington)}$, $t_{on(Damper)}$ and storage time during the picture phase.

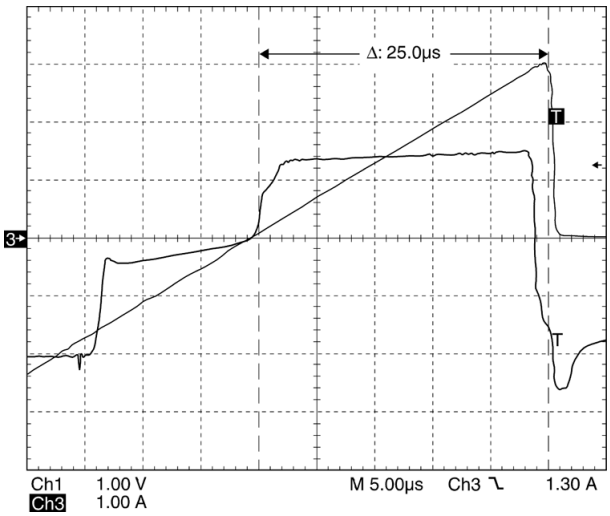

Figure 7. $t_{on(Darlington)}$

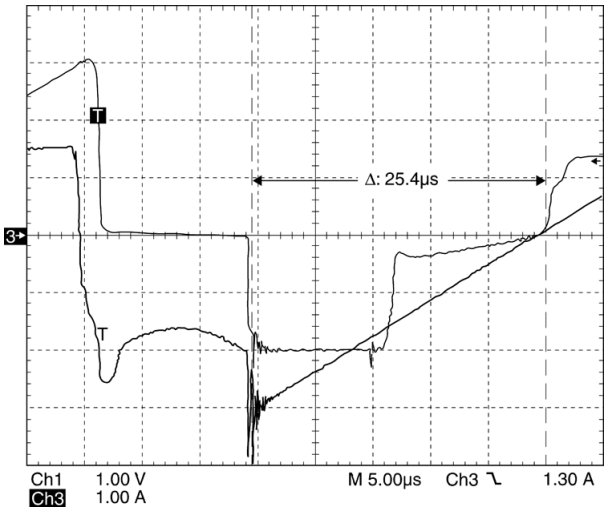

Figure 8. $t_{on(Damper)}$

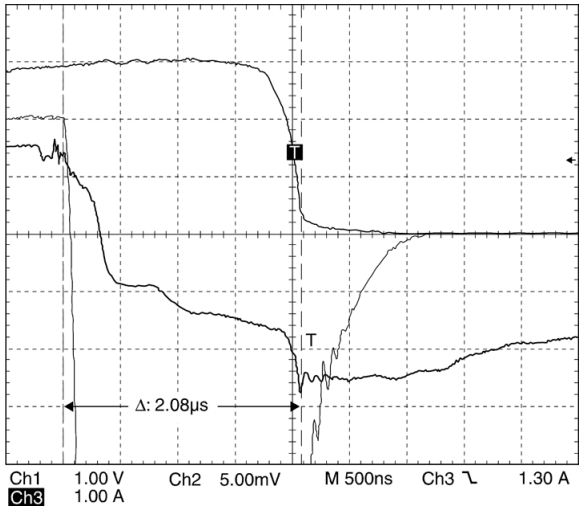

Figure 9. Storage time

5.1. Resistor R_{BB} Calculation.

Based on this result, we can calculate the R_{BB} and C_{BB} value in order to satisfy the above mentioned inequality.
With reference to eq. **(K)**:

$$R_{BB} = \frac{12 - (3.00 + 1.5)}{3/30} = 75\Omega$$

Assuming, at the moment, that:

$H_{FE(forced)} = 30$,

$V_{C(average)} = 3V$,

$V_{C(t)} = 3V$

The closest nominal value could be the sum 39+39 Ω , with 5% tolerance.

5.2. Power Dissipation On The R_{BB}.

Applying the eq. **(N)**:

$$P_{BB} = \frac{78}{2} \cdot 0.1^2 \cdot 0.6 + \frac{(12-0.6)^2}{2 \cdot 78} \cdot 0.4 \quad P_{BB} = 0.234 + 0.327 = 0.561W$$

the nominal, tolerance and power values are indicated as follows: $R_{BB} = (39+39)\Omega$, ±5 %, 1W

The tables show the BU808DFI thermal and dynamic performance when the R_{BB} is variable in the range (15+15) to (47+47) Ω.

*HFE max.=230 @ 5A/5V CBB=47mF, rC=0.6 Ω IC=3A, ICpeak-peak=6A Rth=19°C/W

R_{BB} Ω	I_{Bon} mA	H_{FE} (forced)	I_{Boff} A	V'_{CEoff} V	V_{BEoff} V	$V_{cap.}$ V	Storagetime µsec	Falltime nsec	Tcase C°	Power Losses W
15+15	132	22.73	2.45	8	5.84	6.44	1.4	550	56	1.63
22+22	117	25.64	2.32	6.76	4.56	5.22	1.42	480	55	1.58
27+27	110	27.27	2.22	6.08	3.92	4.52	1.45	440	53	1.47
33+33	100	30.00	2.11	5.28	3.16	3.74	1.54	360	52	1.42
39+39	88	34.09	1.95	4.68	2.6	3.18	1.65	360	51	1.37
47+47	80	37.50	1.7	4.16	2.04	2.64	1.69	480	52	1.42

*HFE min.=60 @ 5A/5V CBB=47mF, rC=0.6 W IC=3A, ICpeak-peak=6A Rth=19°C/W

R_{BB} Ω	I_{Bon} mA	H_{FE}	I_{Boff} A	V'_{CEoff} V	V_{BEoff} V	Vcond. V	Storagetime µsec	Falltime nsec	Tcase C°	Power Losses W
15+15	132	22.73	2.5	7.98	5.8	6.4	1.49	570	56	1.63
22+22	122	24.59	2.34	6.6	4.4	5.04	1.52	500	55	1.58
27+27	115	26.09	2.25	5.96	3.68	4.28	1.5	460	53	1.47
33+33	100	30.00	2.07	5.16	3	3.58	1.65	360	52	1.42
39+39	93	32.26	1.91	4.56	2.44	2.98	1.78	330	53	1.47
47+47	82	36.59	1.66	4.12	1.98	2.54	1.9	450	55	1.58

* Please note that devices with H_{FEmin} and H_{FEmax} limits have been used in this evaluation.

5.3. Capacitor C_{BB} Calculation.

Applying the eq. **(Q)**: $C = \frac{64\mu s}{0.6\Omega} \cdot Ln^{-1}(10) = 46\mu F$

Whereas we have assumed that $V_{C(average)}$ is ten times the value of the $V_C(t)$ and the resistor leakage (ESR) of the capacitor C_{BB} is 0.6 Ω. The commercial, tolerance and resistor leakage values are indicated as follows: $C_{BB} = 47\mu F$, ±10 %, $r_C = 0.6\Omega$

APPENDIX.

1. DISCRETE DARLINGTON STAGE.

The main goal of this paragraph is to describe the mechanism of switching with the discrete Darlington stage and then to investigate in depth the influence of the principal parameters.
Figure 10 shows the discrete Darlington circuit, the transistor T_1 is the driver and T_2 is a power transistor where the base current I_{B2} is delivered from the emitter current I_{E1}. In addition, in this model T_1 and T_2 have the same high voltage breakdown BV_{CEx}, but their dc current gain is different, H_{FE1} and H_{FE2}.

1.1. DC Current Gain.

The main advantage of the Darlington is the high d.c. current gain. If H_{FE1} represents the current gain of the transistor T1 (see figure 10) and H_{FE2} the transistor T_2 we can easily see that the total current gain is:

$$H_{FE} = H_{FE1} + H_{FE2} + H_{FE} \cdot H_{FE2} \quad \textbf{(W)}$$

However, the Darlington is rarely used in this form, since leakage current stabilization resistance affects the added gain.

1.1.1. Influence Of The Stabilising Resistors.

In the simplified Darlington circuit, the emitter current of transistor T_1 is completely injected into the base of T_2; consequently, the leakage current of transistor T_1, when cut-off, is amplified by the transistor T_2; the result is an overall high leakage current for both transistors. This effect can be reduced by stabilising resistors (R_1 and R_2) between base and emitter of the transistors T_1 and T_2 (see figure 11).

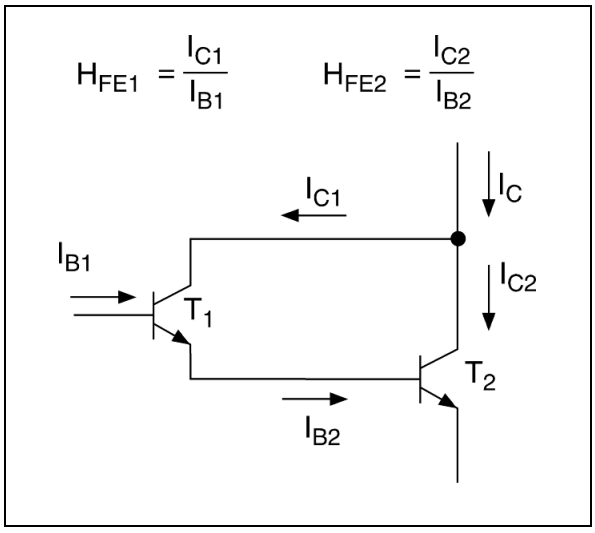

Figure 10: The d.c. gain of a Darlington stage is approximately equal to the d.c. current gains

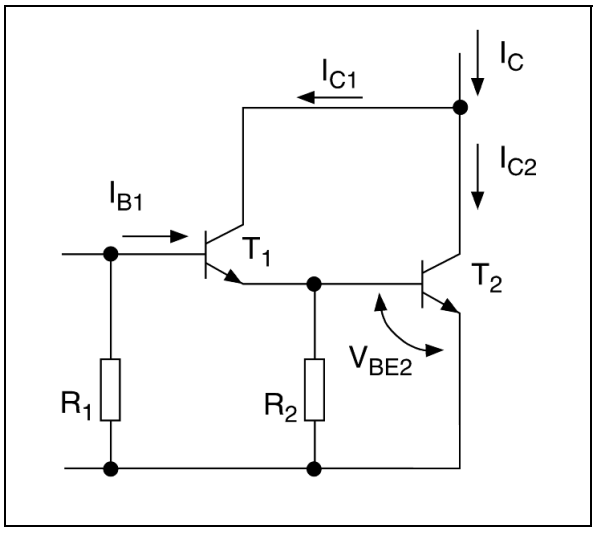

Figure 11: The stabilising resistors reduce the d.c. gain of the circuit. If we consider that the resistance R_1 is part of the drive circuit, it can be seen that the presence of resistance R_2 results in the appearance of a negative term in the gain equation.

1.2. Collector-emitter Saturation Voltage.

In the Darlington circuit, the overall collector-emitter voltage is the sum of the collector-emitter V_{CE1} of the first transistor T_1 and the base-emitter voltage V_{BE2} of the second transistor T_2. (figure 12)

$$V_{ce} = V_{ce1} + V_{be2} \qquad \textbf{(X)}$$

When the gain of the circuit is forced and the base current I_{B1} of the first transistor is increased whilst maintaining the total current I_C, the collector emitter voltage decreases, stabilizes itself, and remains constant. In addition, the base emitter voltage V_{BE2} of the transistor T_2 remains almost constant, whereas the collector emitter voltage V_{CE1} of T_1 is greatly influenced by the forced gain. In other words, as the base current I_{B1} of the transistor T_1 is increased, the transistor saturates, whereas T_2 operates at its normal current gain $H_{FE2} = I_C/I_{B2}$ which, for a given value of collector current, depends on the collector emitter voltage V_{CE}. When a sufficient low forced gain is imposed on the circuit (high base current) such that the collector emitter voltage no longer reduces with forced gain, the Darlington is saturated. The collector emitter saturation voltage $V_{CE\ sat}$ of the Darlington can be written as: $V_{CE\ sat}=V_{CE\ sat1}+V_{BE2}$

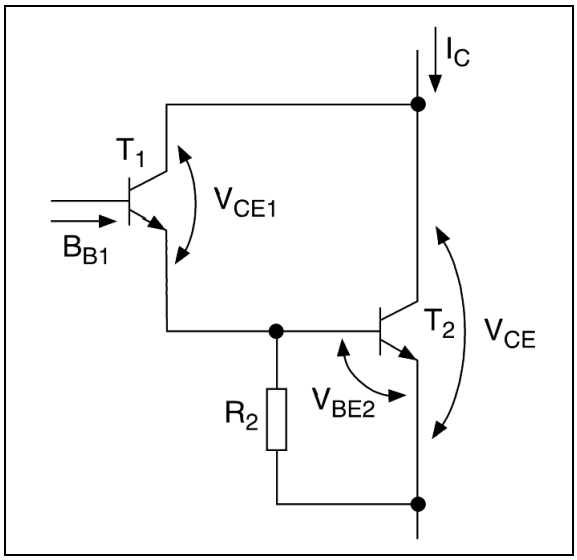

Figure 12: In a Darlington Circuit, the overall collector emitter voltage is the sum of the collector emitter voltage T_1 and the base-emitter voltage of T_2.

In conclusion the base emitter voltage V_{BE2} of transistor T_2 plays a major role in determining the residual collector emitter voltage V_{CE} of the Darlington, and constitutes a lower limit, below which the collector emitter saturation voltage $V_{CE\ sat}$ of the Darlington cannot fall.

1.3. Storage Time.

One of the drawbacks of the Darlington is its relatively long storage time. In effect, in a Darlington configuration, the saturated driver transistor T_1 exhibits a storage time t_{s1}, during which time its collector current varies very little. It is only at the end of time t_{s1} that the collector current I_{C1} of the driver transistor T_1 decreases and leads the base current I_{B2} of the transistor T_2 to decrease. The power transistor T_2 which is quasi saturated, exhibits a storage time t_{s2} which is far from being negligible particularly with high voltage transistors. The result is that the storage time Darlington is the sum of the storage times of the two transistors: $t_s = t_{s1} + t_{s2}$

It can be seen that the fall time of the collector current of T_1 is very high. This is because the switching of T_1 is carried out with low collector emitter voltage, since T_2 is still in a quasi saturation condition, during the switching of the driver stage. Because of this, turn-off produces no losses in the driver transistor.

An examination of the waveforms of figure 13 shows that, during the discharge phase of T_2, its collector current increases slightly. This phenomenon is due to the inductive load. In fact, it is not possible to have a sudden change of current in an inductance. The current through the load thus remains constant. As the driver collector current is annulled, it is the collector current of T_2 which compensates for this. A long storage time can be inconvenient in many applications.

We will examine the parameters which contribute to this phenomenon and which could reduce this storage effect.

I.3.1. Influence Of Forced Gain.

The forced gain H_{FEF} to which the Darlington is subjected, influences its storage time. Figure 14 shows the evolution of the storage time of the Darlington as a function of the forced gain.
It can be seen that the storage time increases quite rapidly as the forced gain H_{FE} influences mainly the storage time t_{s1} of the driver transistor T_1 (since it is this transistor which saturates according to the forced gain). Transistor T_2 operates in quasi-saturation at its normal gain, its storage time being independent of the forced gain.

1.3.2. Influence Of Stabilising Resistors.

The value of the stabilising resistor is equally important when considering the storage time. The value of resistance R_1 influences the storage time t_{s1} of the first transistor T_1. As its value is reduced, (all parameters remaining constant), the storage time t_{s1} of transistor T_1 is reduced, or the total storage time, since t_{s2} does not vary. It can be seen that for sufficiently low values of R_1, the storage time t_{s1} stabilises itself. Resistor R_2 influences the storage time t_{s2} of transistor T_2. The influence of this resistor is very important and the use of a very low resistance value enables the total storage time of the Darlington to be considerably reduced.
The use of low value resistors for R_1 and R_2 is a simple and effective method of reducing the storage time. It should be noted that the use of a low value for R_2 means that the transistor T_1 has to be slightly increased in size since it also has to provide the current for R_2. However, the power dissipated in this resistor remains low since the voltage V_{BE2} across it is of the order of 1V.

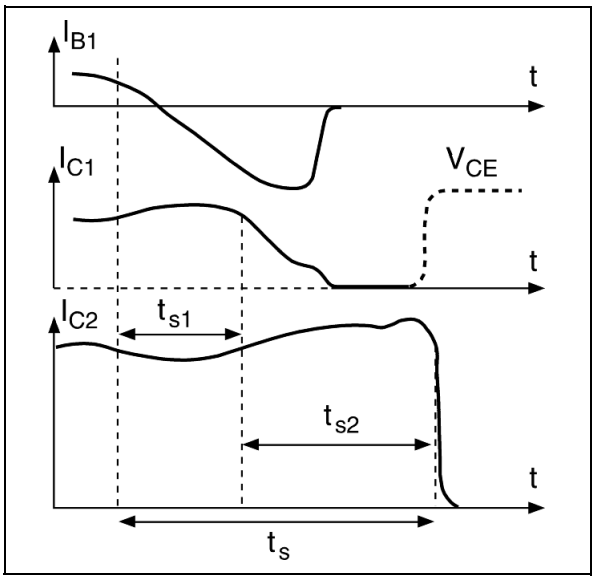

Figure 13: Typical waveforms at turn-off of a Darlington. It can be seen that the storage time t_s of the Darlington is the sum of the storage time t_{s1} and t_{s2} of the two transistors T_1 and T_2.

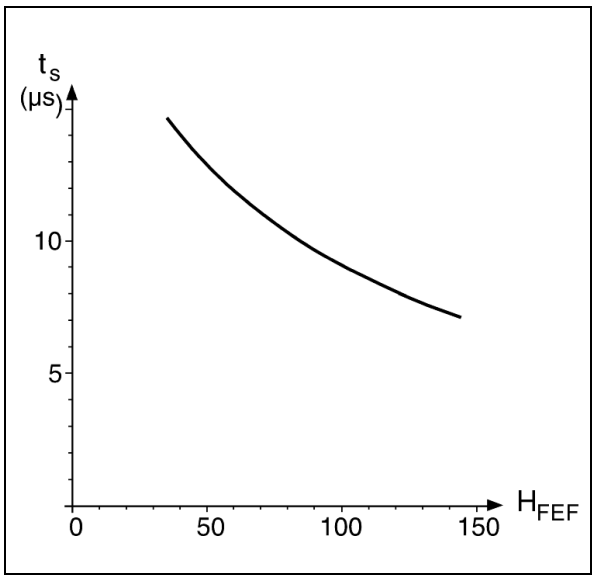

Figure 14: Evolution of the storage time of a Darlington as a function of the forced gain $D(H_{FEF}=I_C/I_{B1})$. This influences only the storage time of the first transistor, which increases rapidly as the transistor is highly saturated.

1.3.3. Influence Of Negative Voltage On The Base Of T_1.

A negative voltage applied to the base of T_1 enables the amplitude of the reverse base current I_{Boff} to be increased, thus to reduce the storage time t_{s1} and, because of this, the total storage time of the Darlington. It can be seen, however, that for ratios of I_{Boff}/I_{Bon}, greater than a few units, the reduction in storage time is low.

In order to reduce even further the storage time of the Darlington, it is necessary to react on the storage time t_{s2} of transistor T_2. We have thus chosen to impart to T_2 the advantages of the negative voltage applied to the base of T_1 by means of discharge diode D_1 (figure 15).

Diode D_1 is connected in anti-parallel with the base emitter junction of transistor T_1. In order to render this diode conducting, and consequently to evacuate the carriers stored in the base of T_2, the voltage at the emitter of T_1 must be greater than that at the base of the same transistor. However, this can only occur when the base emitter junction of the transistor T_1 is completely cut off. The negative voltage is therefore only applied to transistor T_2 when transistor T_1 is cut off. Despite the fact the switching of the two transistors always occur in cascade, the presence of diode D_1 enables a considerable reduction in the storage time of the Darlington to be achieved.

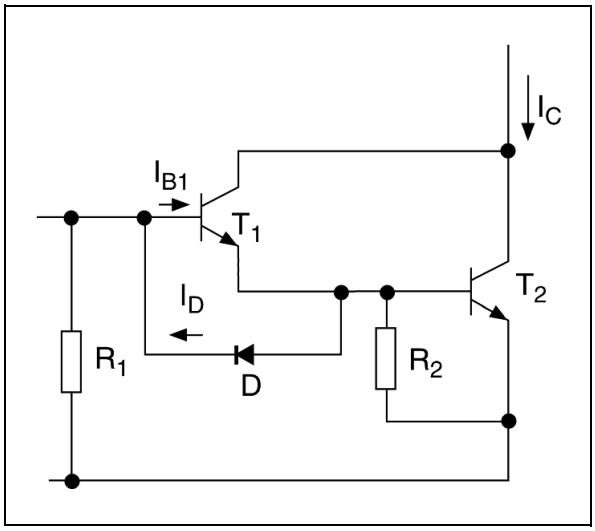

Figure 15: Diode D enables T_2 to benefit from the negative voltage applied to the base of T_1. However, the diode can only conduct when the emitter-base junction of T_1 is cut-off.

1.4. Fall Time.

In the switching mode, the fall time of the collector current is of great importance, since the majority of the turn-off switching losses take place during this time. In a Darlington, the fall time of the collector current is only dependent on transistor T_2 since transistor T_1 is already cut off.

The parameters which influence the fall time t_f of the collector current of a Darlington are the same as those which condition the fall time of T_2 only, operating under the same conditions. In a power transistor, the optimum fall time t_f is reached when simultaneous cut off of the emitter base and collector base junctions is achieved. Because of this, the fall time of the collector current of the power transistor depends on the amplitude and the slope of the reverse base current.

The fall time t_f of a Darlington depends essentially on the waveform of the reverse base current I_{Boff} of transistor T_2.

1.4.1. Influence Of The Reverse Base Current Of T_2.

The waveform of the reverse base current of transistor T_2 is a determining factor in the fall time of the Darlington collector current. A simple method of controlling the reverse base current of transistor T_2 consists of inserting a small inductance L_B in series with the base of transistor T_1. As soon as the transistor T_1 begins to turn off and its collector current diminishes, the inductance produces a negative extra voltage on the cathode of the Diode D_1 and tends to constant the current flowing through it.

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