General Description

1. Introduction

The VCT 49xxI is an IC family of high-quality single-chip TV processors. Modular design and deep-submicron technology allow the economic integration of features in all classes of single-scan TV sets. The VCT 49xxI family is based on functional blocks contained and approved in existing products like DRX 396xA, MSP 34x5G, VSP 94x7B, DDP 3315C, and SDA 55xx.

Each member of the family contains the entire IF, audio, video, display, and deflection processing for 4:3 and 16:9 50/60-Hz mono and stereo TV sets. The integrated microcontroller is supported by a powerful OSD generator with integrated Teletext & CC acquisition including on-chip page memory.

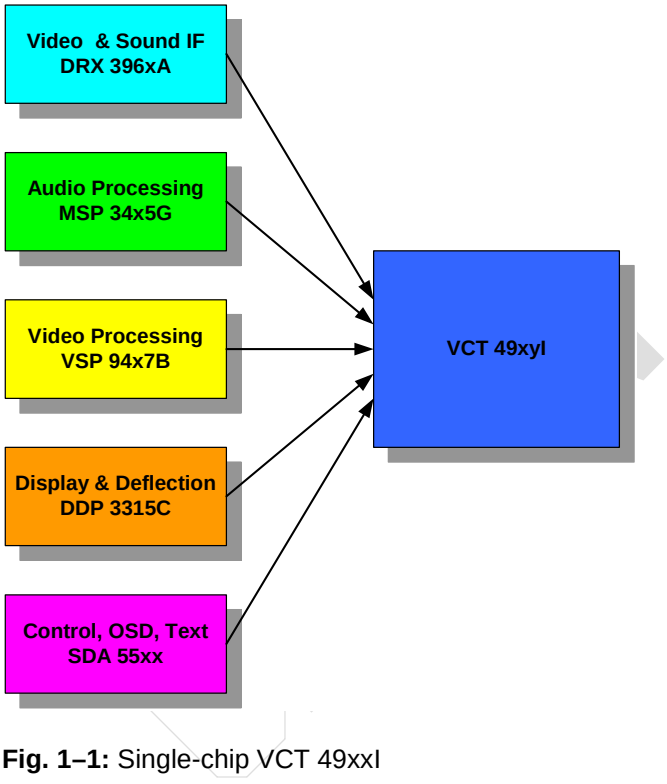

Fig. 1–1: Single-chip VCT 49xxI

1.1. Features

The VCT 49xxI family offers a rich feature set, covering the whole range of state-of-the-art 50/60-Hz TV applications.

- PSSDIP88-1/-2 package
- PMQFP144-2 package
- Submicron CMOS technology
- Low-power standby mode
- Single 20.25-MHz reference crystal
- 8-bit 8051 instruction set compatible CPU
- Up to 256 kB on-chip program ROM
- WST, PDC, VPS, and WSS acquisition
- Closed Caption and V-chip acquisition
- Up to 10 pages on-chip teletext memory
- Multi-standard QSS IF processing with single SAW
- FM Radio and RDS with standard TV tuner
- TV-sound demodulation:
  - all A2 standards
  - all NICAM standards
  - BTSC/SAP with MNR (DBX optional)
  - EIA-J
- Baseband sound processing for loudspeaker channel:
  - volume
  - bass and treble
  - loudness
  - balance
  - spatial effect (e.g. pseudo stereo)
  - Micronas AROUND (virtual Dolby optional)
  - Micronas BASS
- CVBS, S-VHS, YC_rC_b and RGB inputs
- 4H adaptive comb filter (PAL/NTSC)
- multi-standard color decoder (PAL/NTSC/SECAM)
- Nonlinear horizontal scaling “panorama vision”
- Luma and chroma transient improvement (LTI, CTI)
- Non-linear color space enhancement (NCE)
- Dynamic black level expander (BLE)
- Scan velocity modulation output
- Soft start/stop of H-drive
- Vertical angle and bow correction
- Average and peak beam current limiter
- Nonlinear and dynamic EHT compensation
- Black switch off procedure (BSO)

1.2. Chip Architecture

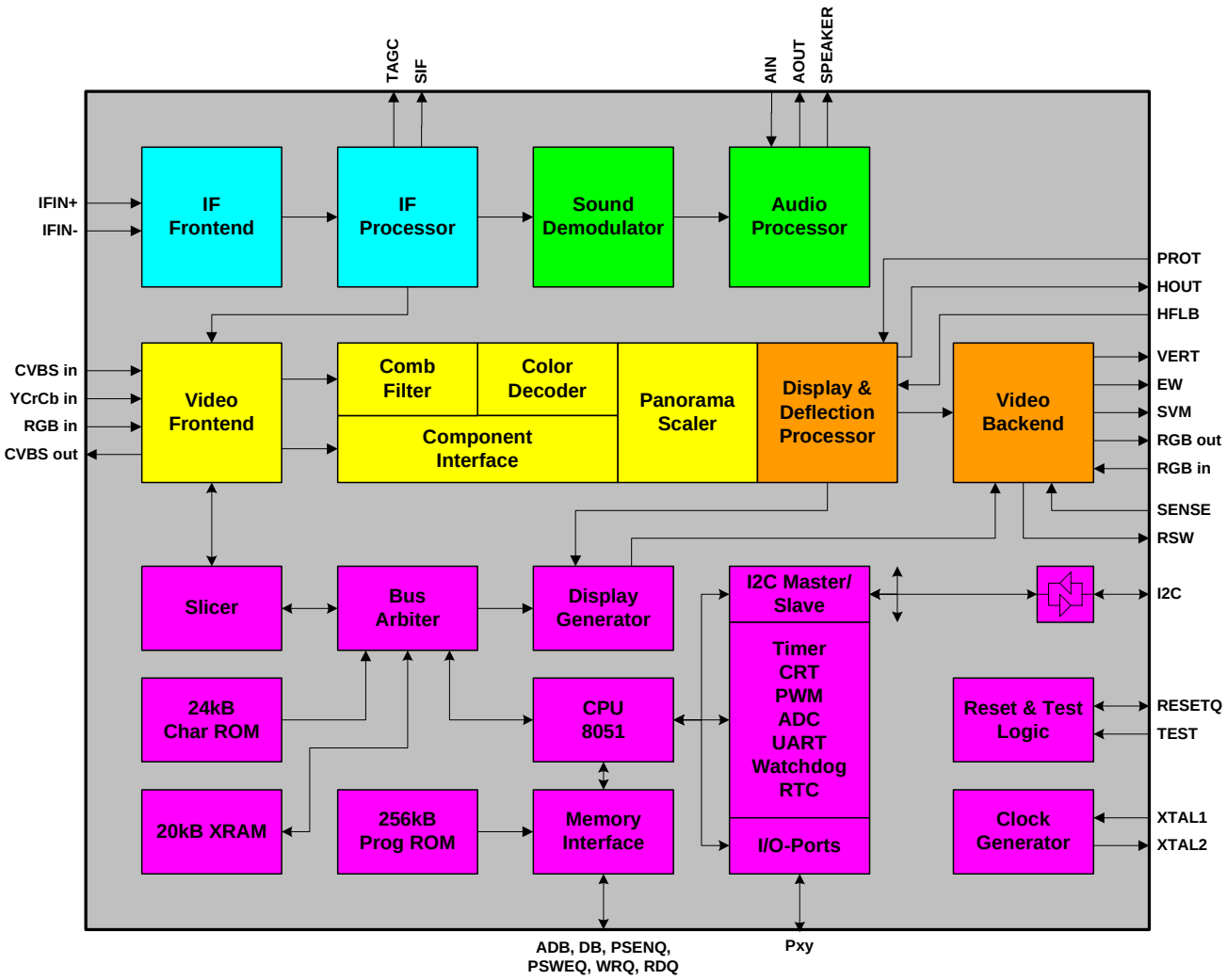

Fig. 1–2: Block diagram of the VCT 49xxI

1.3. System Application

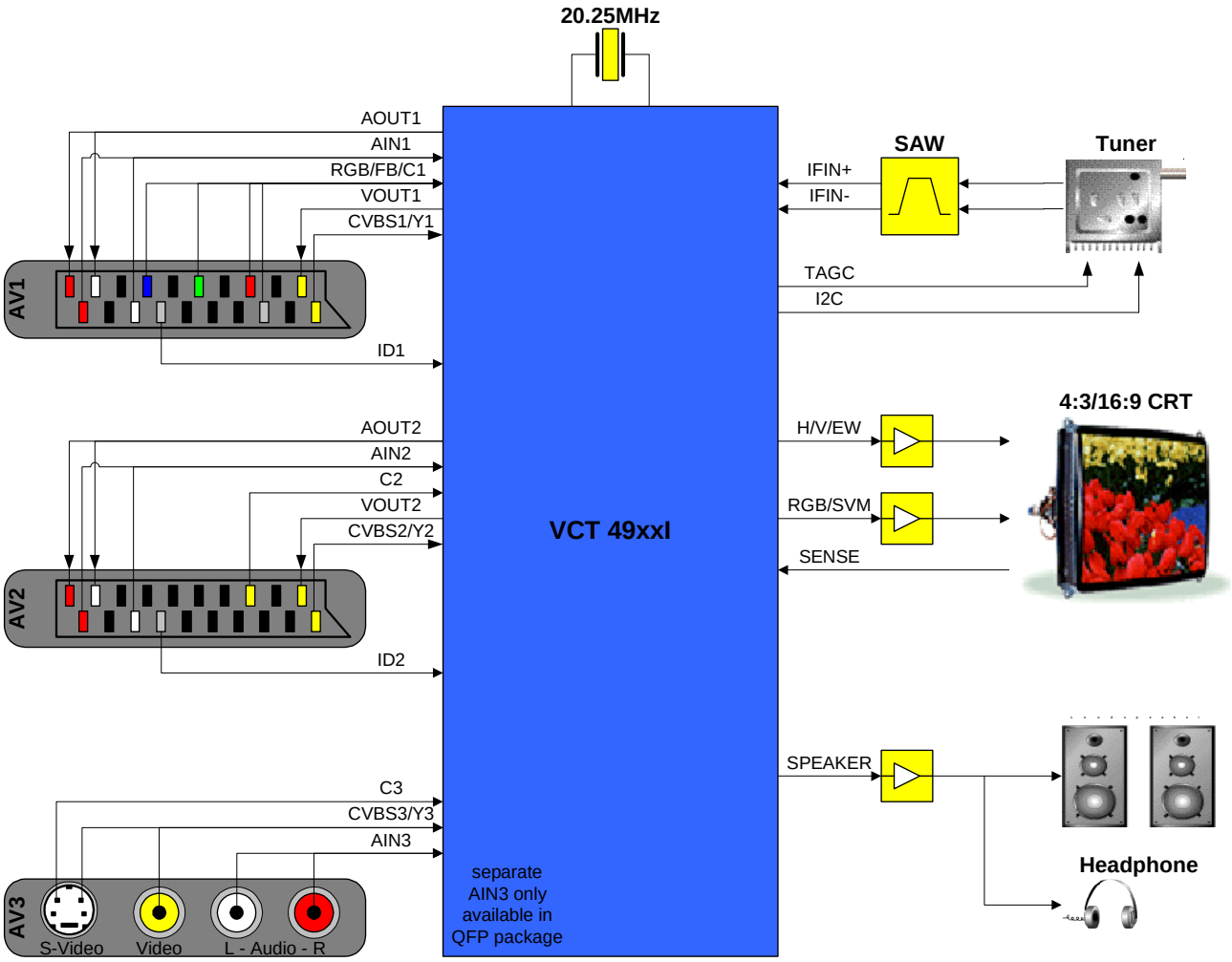

Fig. 1–3: Stereo TV set with VCT 49xxI

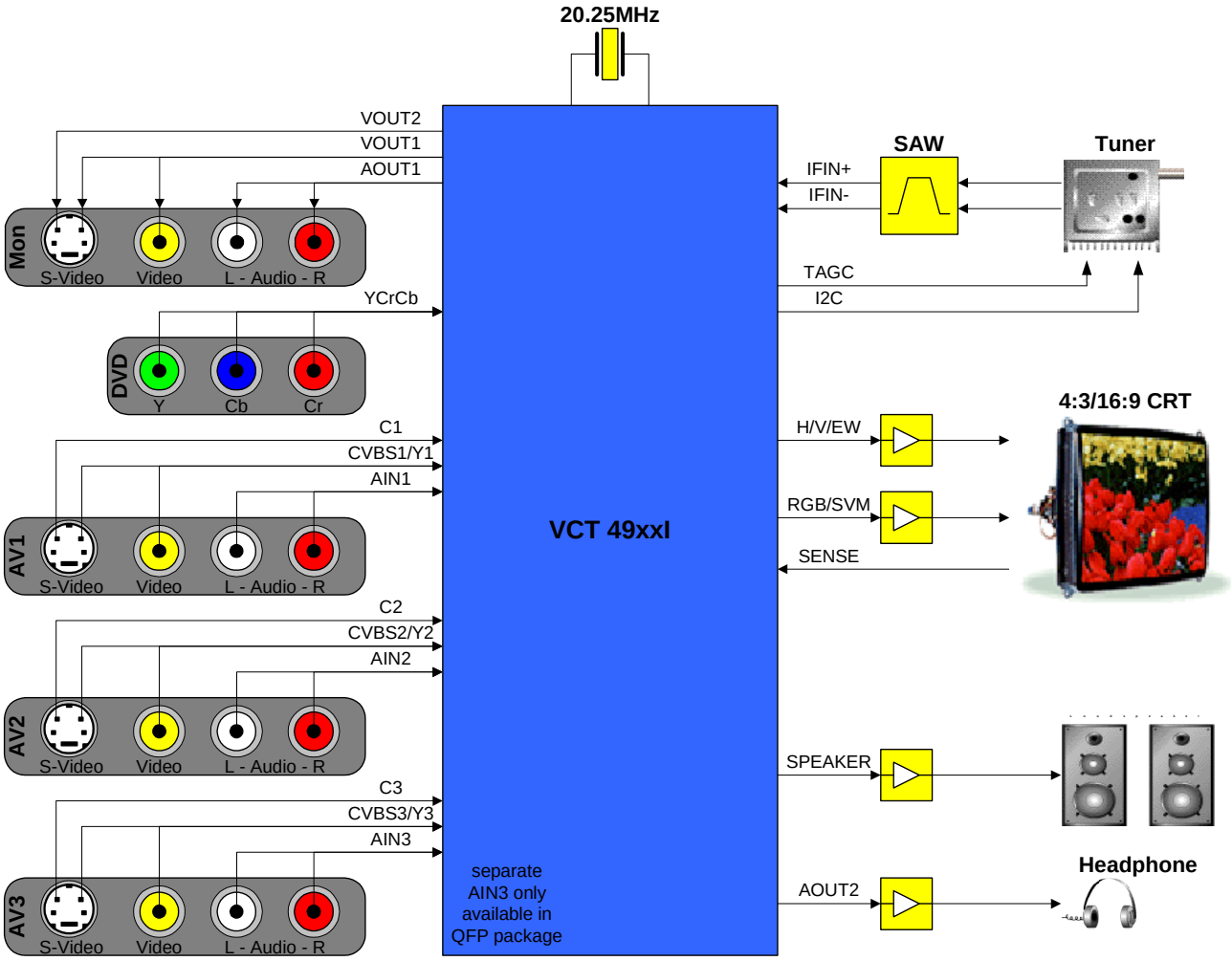

Fig. 1–4: Stereo TV set with VCT 49xxI

3. Control Interface

Table 3–1: I2C Slave Device Addresses

Block	Device Address	
	Write	**Read**
DRX	h'8E	h'8F
MSP	h'8C	h'8D
VSP	h'B0	h'B1
DDP	h'BC	h'BD
TVT	programmable	

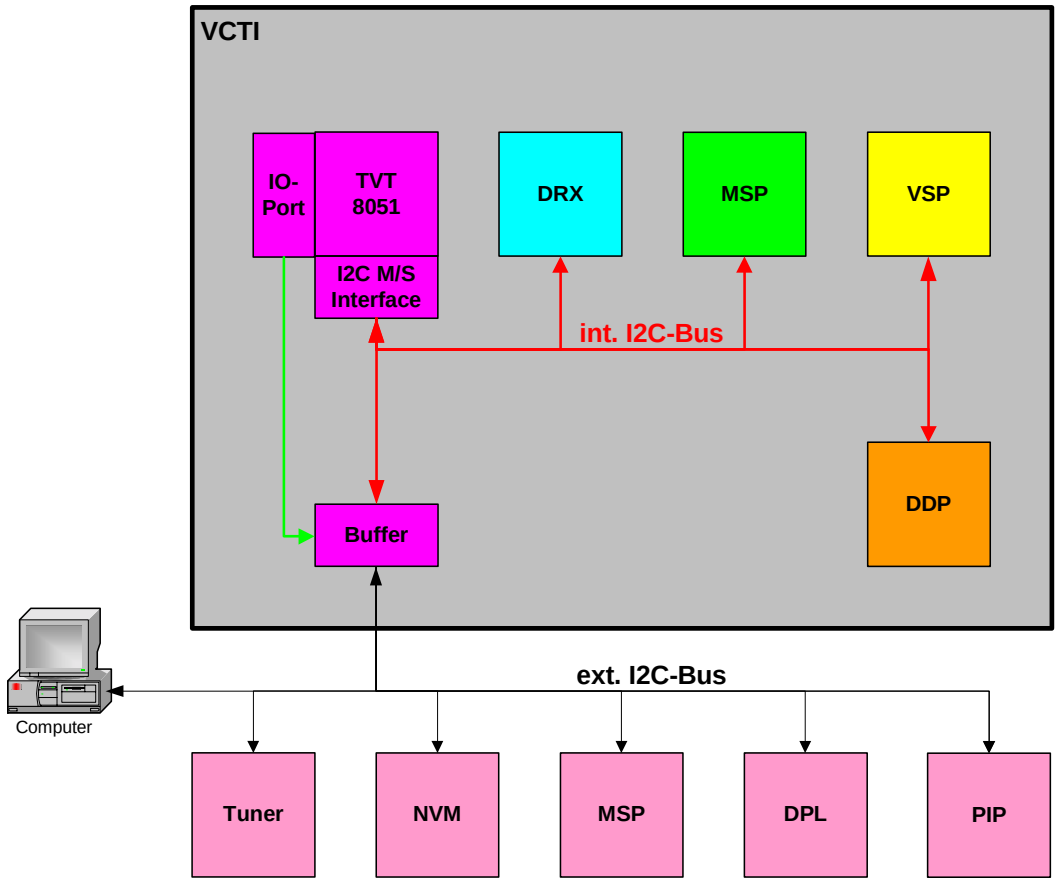

Fig. 3–1: I^2C Environment

4. Specifications

4.1. Outline Dimensions

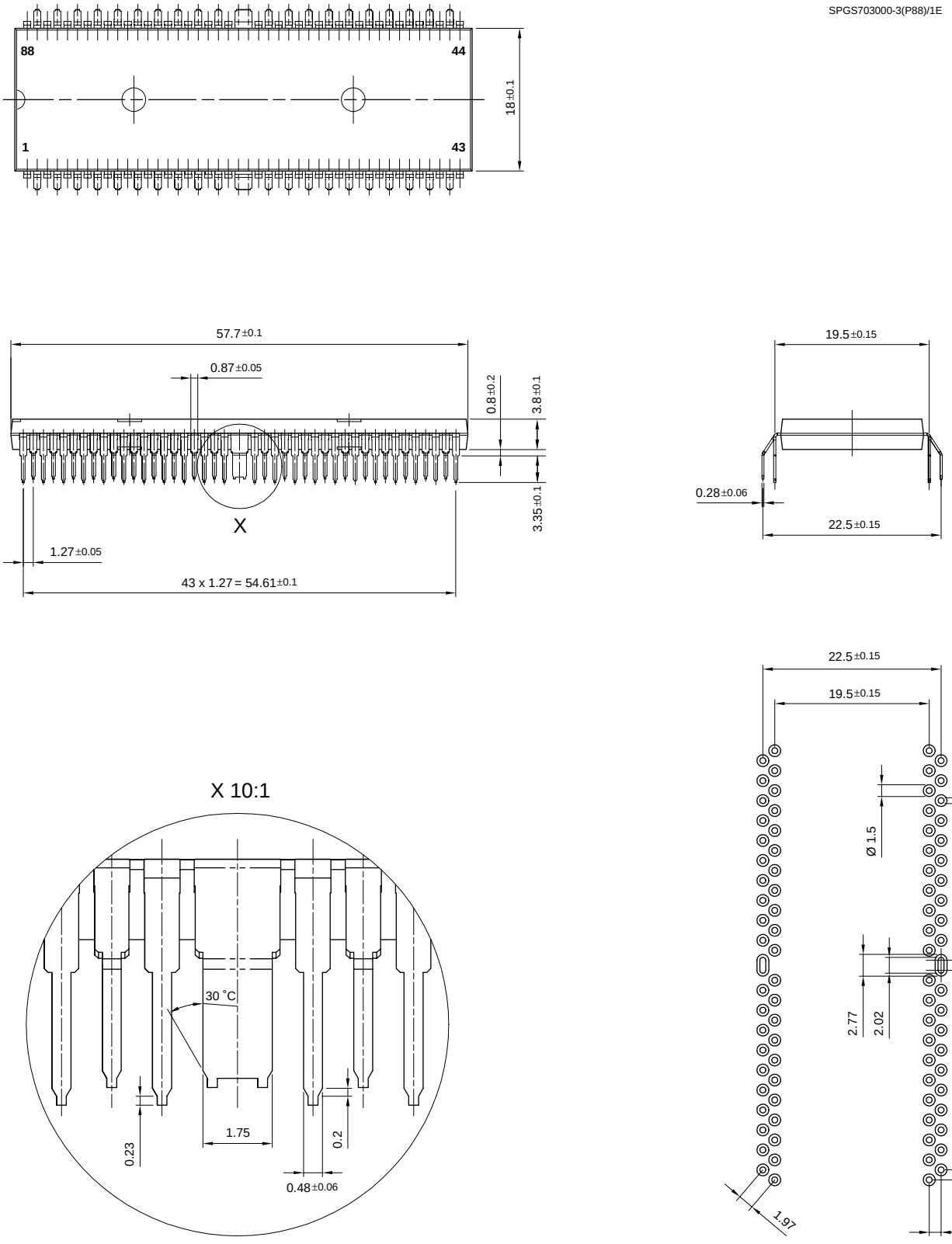

Fig. 4–1:
88-Pin Plastic Staggered Shrink Dual Inline Package
(PSSDIP88-1/-2)
Weight approximately 9.6 g
Dimensions in mm

Pin Connections and Short Descriptions

NC = not connected
LV = if not used, leave vacant
OBL = obligatory; connect as described in circuit diagram
IN = Input Pin
OUT = Output Pin
SUPPLY = Supply Pin

Pin No.		Pin Name	Type	Connection	Short Description
PSSDIP 88-pin	PMQFP-2 144-pin			(If not used)	
1	128	GND	SUPPLY	OBL	Ground Platform
2	129	VSUP5.0BE	SUPPLY	OBL	Supply Voltage Analog Video Back-end, 5.0 V
3	130	TEST	IN	GND	Test Input, reserved for Test
4	131	VERT+	OUT	LV	Differential Vertical Sawtooth Output
5	132	VERT-	OUT	LV	Differential Vertical Sawtooth Output
6	133	EW	OUT	LV	Vertical Parabola Output
7	134	RSW2	OUT	LV	Range Switch 2 Output
8	135	RSW1	OUT	LV	Range Switch 1 Output
9	136	SENSE	IN	GND	Sense ADC Input
10	137	GNDM	IN	GND	Reference Ground for Sense ADC
11	138	FBIN	IN	GND	Fast Blank Input, Back-end
12	139	RIN	IN	GND	Analog Red Input, Back-end
13	140	GIN	IN	GND	Analog Green Input, Back-end
14	141	BIN	IN	GND	Analog Blue Input, Back-end
15	142	SVMOUT	OUT	VSUP5.0BE	Scan Velocity Modulation Output
16	143	ROUT	OUT	VSUP5.0BE	Analog Red Output
17	144	GOUT	OUT	VSUP5.0BE	Analog Green Output
18	1	BOUT	OUT	VSUP5.0BE	Analog Blue Output
19	2	VRD		OBL	Reference Voltage for RGB DACs
20	3	XREF		OBL	Reference Current for RGB DACs
21	4	VSUP3.3BE	SUPPLY	OBL	Supply Voltage Analog Video Back-end, 3.3 V
22	5	GND	SUPPLY	OBL	Ground Platform
23	6	GND	SUPPLY	OBL	Ground Platform
24	7	VSUP3.3IO	SUPPLY	OBL	Supply Voltage I/O Ports, 3.3 V
25	8	VSUP3.3DAC	SUPPLY	OBL	Supply Voltage Video DACs, 3.3 V
26	9	GNDDAC	SUPPLY	OBL	Ground Video DACs
27	10	SAFETY	IN	GND	Safety Input

Pin No. PSSDIP 88-pin	Pin No. PMQFP-2 144-pin	Pin Name	Type	Connection (If not used)	Short Description
28	11	HFLB	IN	HOUT	Horizontal Flyback Input
29	12	HOUT	OUT	LV	Horizontal Drive Output
30	13	VPROT	IN	GND	Vertical Protection Input
	37	PWMV	OUT	LV	PWM Vertical Output
	38	DFVBL	OUT	LV	Dynamic Focus Vertical Blanking Output
31	39	SDA	IN/OUT	OBL	I^2C Bus Data Input/Output
32	40	SCL	IN/OUT	OBL	I^2C Bus Clock Input/Output
33	41	P21	IN/OUT	LV	Port 2, Bit 1 Input/Output
34	42	P20	IN/OUT	LV	Port 2, Bit 0 Input/Output
35	43	P17	IN/OUT	LV	Port 1, Bit 7 Input/Output
36	44	P16	IN/OUT	LV	Port 1, Bit 6 Input/Output
37	45	P15	IN/OUT	LV	Port 1, Bit 5 Input/Output
38	46	P14	IN/OUT	LV	Port 1, Bit 4 Input/Output
39	47	P13	IN/OUT	LV	Port 1, Bit 3 Input/Output
40	48	P12	IN/OUT	LV	Port 1, Bit 2 Input/Output
41	49	P11	IN/OUT	LV	Port 1, Bit 1 Input/Output
42	50	P10	IN/OUT	LV	Port 1, Bit 0 Input/Output
43	53	VSUP3.3FE	SUPPLY	OBL	Supply Voltage Analog Video Front-end, 3.3 V
44	54	GND	SUPPLY	OBL	Ground Platform
45	55	GND	SUPPLY	OBL	Ground Platform
46	56	VSUP1.8FE	SUPPLY	OBL	Supply Voltage Analog Video Front-end, 1.8 V
47	57	VOUT3	OUT	LV	Analog Video 3 Output
48	58	VOUT2	OUT	LV	Analog Video 2 Output
49	59	VOUT1	OUT	LV	Analog Video 1 Output
50	60	VIN1	IN	GND	Analog Video 1 Input
51	61	VIN2	IN	GND	Analog Video 2 Input
52	62	VIN3	IN	GND	Analog Video 3 Input
53	63	VIN4	IN	GND	Analog Video 4 Input
54	64	VIN5	IN	GND	Analog Video 5 Input
55	65	VIN6	IN	GND	Analog Video 6 Input
56	66	VIN7	IN	GND	Analog Video 7 Input
57	67	VIN8	IN	GND	Analog Video 8 Input
58	68	VIN9	IN	GND	Analog Video 9 Input

Pin No. PSSDIP 88-pin	Pin No. PMQFP-2 144-pin	Pin Name	Type	Connection (If not used)	Short Description
59	69	VIN10	IN	GND	Analog Video 10 Input
60	70	VIN11	IN	GND	Analog Video 11 Input
61	98	P23	IN/OUT	LV	Port 2, Bit 3 Input/Output
62	99	P22	IN/OUT	LV	Port 2, Bit 2 Input/Output
63	100	XTAL2	OUT	OBL	Analog Crystal Output
64	101	XTAL1	IN	OBL	Analog Crystal Input
65	102	VSUP1.8DIG	SUPPLY	OBL	Supply Voltage Digital Core, 1.8 V (main and standby supply)
66	103	GND	SUPPLY	OBL	Ground Platform
67	104	GND	SUPPLY	OBL	Ground Platform
68	105	VSUP3.3DIG	SUPPLY	OBL	Supply Voltage Digital Core, 3.3 V (main and standby supply)
69	106	VSUP5.0IF	SUPPLY	OBL	Supply Voltage Analog IF Front-end, 5.0 V
70	107	GNDIF	SUPPLY	OBL	Ground Analog IF Front-end
71	108	RESETQ	IN/OUT	OBL	$\overline{\text{Reset}}$ Input/Output
72	109	IFIN+	IN	$VREF_{IF}$	Differential IF Input
73	110	IFIN-	IN	$VREF_{IF}$	Differential IF Input
74	111	VREFIF		OBL	Reference Voltage, IF ADC
75	112	TAGC	OUT	LV	Tuner AGC Output
76	113	AIN1R / SIF	IN/OUT	GND	Analog Audio 1 Input, Right Analog 2nd Sound IF Output
77	114	AIN1L	IN	GND	Analog Audio 1 Input, Left
78	115	AIN2R	IN	GND	Analog Audio 2 Input, Right
79	116	AIN2L	IN	GND	Analog Audio 2 Input, Left
	117	AIN3R	IN	GND	Analog Audio 3 Input, Right
	118	AIN3L	IN	GND	Analog Audio 3 Input, Left
	119	AOUT2R	OUT	LV	Analog Audio 2 Output, Right
	120	AOUT2L	OUT	LV	Analog Audio 2 Output, Left
80		AIN3R / AOUT2R	IN / OUT	LV	Analog Audio 3 Input, Right Analog Audio 2 Output, Right
81		AIN3L / AOUT2L	IN / OUT	LV	Analog Audio 3 Input, Left Analog Audio 2 Output, Left
82	121	AOUT1R	OUT	LV	Analog Audio 1 Output, Right
83	122	AOUT1L	OUT	LV	Analog Audio 1 Output, Left
84	123	SPEAKERR	OUT	LV	Analog Loudspeaker Output, Right

Pin No. PSSDIP 88-pin	Pin No. PMQFP-2 144-pin	Pin Name	Type	Connection (If not used)	Short Description
85	124	SPEAKERL	OUT	LV	Analog Loudspeaker Output, Left
86	125	VREFAU		OBL	Reference Voltage, Audio
87	126	VSUP8.0AU	SUPPLY	OBL	Supply Voltage Analog Audio, 8.0 V
88	127	GND	SUPPLY	OBL	Ground Platform
	71	P37 / 656IO7	IN/OUT	LV	Port 3, Bit 7 Input/Output Digital 656 Bus 7 Input/Output
	72	P36 / 656IO6	IN/OUT	LV	Port 3, Bit 6 Input/Output Digital 656 Bus 6 Input/Output
	73	P35 / 656IO5	IN/OUT	LV	Port 3, Bit 5 Input/Output Digital 656 Bus 5 Input/Output
	74	P34 / 656IO4	IN/OUT	LV	Port 3, Bit 4 Input/Output Digital 656 Bus 4 Input/Output
	75	P33 / 656IO3	IN/OUT	LV	Port 3, Bit 3 Input/Output Digital 656 Bus 3 Input/Output
	76	GNDEIO	SUPPLY	OBL	Ground Extended I/O Ports
	77	VSUP3.3EIO	SUPPLY	OBL	Supply Voltage Extended I/O Ports, 3.3 V
	78	P32 / 656IO2	IN/OUT	LV	Port 3, Bit 2 Input/Output Digital 656 Bus 2 Input/Output
	79	P31 / 656IO1	IN/OUT	LV	Port 3, Bit 1 Input/Output Digital 656 Bus 1 Input/Output
	80	P30 / 656IO0	IN/OUT	LV	Port 3, Bit 0 Input/Output Digital 656 Bus 0 Input/Output
	81	P26 / 656VIO	IN/OUT	LV	Port 2, Bit 6 Input/Output Digital 656 Vsync Input/Output
	82	P25 / 656HIO	IN/OUT	LV	Port 2, Bit 5 Input/Output Digital 656 Hsync Input/Output
	83	P24 / 656CLKIO	IN/OUT	LV	Port 2, Bit 4 Input/Output Digital 656 Clock Input/Output
	31	ADB19	OUT	LV	Address Bus 19 Output
	21	ADB18	OUT	LV	Address Bus 18 Output
	19	ADB17	OUT	LV	Address Bus 17 Output
	22	ADB16	OUT	LV	Address Bus 16 Output
	23	ADB15	OUT	LV	Address Bus 15 Output
	18	ADB14	OUT	LV	Address Bus 14 Output
	17	ADB13	OUT	LV	Address Bus 13 Output
	26	ADB12	OUT	LV	Address Bus 12 Output
	14	ADB11	OUT	LV	Address Bus 11 Output

Pin No. PSSDIP 88-pin	Pin No. PMQFP-2 144-pin	Pin Name	Type	Connection (If not used)	Short Description
	96	ADB10	OUT	LV	Address Bus 10 Output
	15	ADB9	OUT	LV	Address Bus 9 Output
	16	ADB8	OUT	LV	Address Bus 8 Output
	27	ADB7	OUT	LV	Address Bus 7 Output
	28	ADB6	OUT	LV	Address Bus 6 Output
	29	ADB5	OUT	LV	Address Bus 5 Output
	30	ADB4	OUT	LV	Address Bus 4 Output
	84	ADB3	OUT	LV	Address Bus 3 Output
	85	ADB2	OUT	LV	Address Bus 2 Output
	86	ADB1	OUT	LV	Address Bus 1 Output
	87	ADB0	OUT	LV	Address Bus 0 Output
	88	DB0	IN/OUT	LV	Data Bus 0 Input/Output
	89	DB1	IN/OUT	LV	Data Bus 1 Input/Output
	90	DB2	IN/OUT	LV	Data Bus 2 Input/Output
	91	DB3	IN/OUT	LV	Data Bus 3 Input/Output
	92	DB4	IN/OUT	LV	Data Bus 4 Input/Output
	93	DB5	IN/OUT	LV	Data Bus 5 Input/Output
	94	DB6	IN/OUT	LV	Data Bus 6 Input/Output
	95	DB7	IN/OUT	LV	Data Bus 7 Input/Output
	32	RDQ	OUT	LV	$\overline{\text{Data Read Enable}}$ Output
	33	WRQ	OUT	LV	$\overline{\text{Data Write Enable}}$ Output
	34	OCF	OUT	LV	Opcode Fetch Output
	35	ALE	OUT	LV	Address Latch Enable Output
	36	RSTQ	OUT	LV	$\overline{\text{Internal CPU Reset}}$ Output
	97	PSENQ	OUT	LV	$\overline{\text{Program Store Enable}}$ Output
	20	PSWEQ	OUT	LV	$\overline{\text{Program Store Write Enable}}$ Output
	51	XROMQ	IN	OBL	$\overline{\text{External ROM Enable}}$ Input
	52	EXTIFQ	IN	LV	$\overline{\text{Enable External Interface}}$ Input
	24	STOPQ	IN	LV	$\overline{\text{Stop CPU}}$ Input
	25	ENEQ	IN	LV	$\overline{\text{Enable Emulation}}$ Input

Pin Descriptions

Supply Pins

VSUP1.8DIG – Supply Voltage 1.8 V
This pin is main and standby supply for the digital core logic of controller, video, display and deflection processing.

VSUP1.8FE – Supply Voltage 1.8 V
This pin is main supply for the analog video front-end.

VSUP3.3FE – Supply Voltage 3.3 V
This pin is main supply for the analog video front-end.

VSUP3.3IO – Supply Voltage 3.3 V
This pin is main and standby supply for the digital I/O-ports.

VSUP3.3DIG – Supply Voltage 3.3 V
This pin is main supply for the digital core logic of IF and audio processing and digital video back-end.

VSUP3.3BE – Supply Voltage 3.3 V
This pin is main supply for the analog video back-end.

VSUP5.0BE – Supply Voltage 5.0 V
This pin is main supply for the analog video back-end.

VSUP8.0AU – Supply Voltage 8.0 V
This pin is main supply for the analog audio processing.

GND – Ground Platform
This pin is main ground for all above supplies.

VSUP3.3DAC – Supply Voltage 3.3 V
This pin is main supply for the video DACs.

GNDDAC – Ground for 3.3 V Video DAC Supply

VSUP5.0IF – Supply Voltage 5.0 V
This pin is main supply for the analog IF front-end.

GNDIF – Ground for 5.0 V IF Supply

VSUP3.3EIO – Supply Voltage 3.3 V
This pin is main and standby supply for the extended digital I/O-ports available in QFP package only. It is internally connected to **VSUP3.3IO.**

GNDEIO – Ground for 3.3 V Extended I/O Supply
It is internally connected to GND.

Application Note:
All **GND** pins must be connected to a low-resistive ground plane underneath the IC. All supply pins must be connected separately with short and low-resistive lines to the power supply. Decoupling capacitors from **VSUPxx** to **GND** have to be placed as closely as possible to these pins. It is recommended to use more than one capacitor. By choosing different values, the frequency range of active decoupling can be extended.

IF Pins

VREFIF – Reference Voltage for Analog IF (Fig. 4–9)
This pin must be connected to **GNDIF** via a circuitry according to the application circuit. Low inductance caps are necessary.

IFIN+, IFIN- – Balanced IF Input (Fig. 4–6)
These pins must be connected to the SAW filter output. The SAW filter has to be placed as close as possible. The layout of the IF input should be symmetrical with respect to **GNDIF**.

SIF – 2nd Sound IF Output (Fig. 4–8)
Output level is set via I^2C-Bus. An appropriate sound processor (e.g. MSP) can be connected to this pin. This pin is also configurable as audio input (see Fig. 4–10).

TAGC – Tuner AGC Output (Fig. 4–7)
This pin controls the delayed tuner AGC. As it is a noise-shaped-I-DAC output, it has to be connected according to the application circuit.

Audio Pins

VREFAU – Reference Voltage for Analog Audio (Fig. 4–14)
This pin serves as the internal ground connection for the analog audio circuitry. It must be connected to the **GND** pin with a 3.3 µF and a 100 nF capacitor in parallel. This pins shows a DC level of typically 3.77 V.

AIN1 L – Audio 1 Inputs (Fig. 4–10)
The analog input signal for audio 1 is fed to this pin. Analog input connection must be AC coupled.

AIN1 R – Audio 1 Inputs (Fig. 4–10)
The analog input signal for audio 1 is fed to this pin. Analog input connection must be AC coupled. This pin is also configurable as sound IF output (see Fig. 4–8).

AIN2 R/L – Audio 2 Inputs (Fig. 4–10)
The analog input signal for audio 2 is fed to this pin. Analog input connection must be AC coupled.

AIN3 R/L – Audio 3 Inputs (Fig. 4–10)
The analog input signal for audio 3 is fed to this pin. Analog input connection must be AC coupled.

AOUT1 R/L – Audio 1 Outputs (Fig. 4–11)
Output of the analog audio 1 signal. Connections to these pins are intended to be AC coupled.

AOUT2 R/L – Audio 2 Outputs (Fig. 4–11)
Output of the analog audio 2 signal. Connections to these pins are intended to be AC coupled.

SPEAKER R/L – Loudspeaker Outputs (Fig. 4–13)
Output of the loudspeaker signal. A 1 nF capacitor to **GND** must be connected to these pins. Connections to these pins are intended to be AC-coupled.

Video Pins

VIN 1–11 – Analog Video Input (Fig. 4–15)
These are the analog video inputs. A CVBS, S-VHS, YCrCb or RGB/FB signal is converted using the luma, chroma and component AD converters. The input signals must be AC-coupled by 100nF. In case of an analog fast blank signal carrying alpha blending information the input signal must be DC-coupled.

VOUT 1-3 – Analog Video Output (Fig. 4–16)
The analog video inputs that are selected by the video source select matrix are output at these pins.

RIN, GIN, BIN – Analog RGB Input (Fig. 4–17)
These pins are used to insert an external analog RGB signal, e.g. from a SCART connector which can be switched to the analog RGB outputs with the fast blank signal. Separate brightness and contrast settings for the external analog signals are provided.

FBIN – Fast Blank Input (Fig. 4–18)
This pin is used to switch the RGB outputs to the external analog RGB inputs. The active level (low or high) can be selected by software.

ROUT, GOUT, BOUT – Analog RGB Output (Fig. 4–19)
These pins are the analog Red/Green/Blue outputs of the back-end. The outputs are current sinks.

SVMOUT – Scan Velocity Modulation Output (Fig. 4–19)
This output delivers the analog SVM signal. The D/A converter is a current sink like the RGB D/A converters. At zero signal the output current is 50% of the maximum output current.

VRD – DAC Reference Decoupling (Fig. 4–20)
Via this pin the RGB-DAC reference voltage is decoupled by an external capacitor. The DAC output currents depend on this voltage, therefore a pulldown transistor can be used to shut off all beam currents. A decoupling capacitor of 4.7 µF in parallel to 100 nF (low inductance) is required.

XREF – DAC Current Reference (Fig. 4–20)
External reference resistor for DAC output currents, typical 10 kΩ to adjust the output current of the D/A converters. (see recommended operating conditions). This resistor has to be connected to ground as closely as possible to the pin.

4.3.5. CRT Pins

VPROT – Vertical Protection Input (Fig. 4–22)
The vertical protection circuitry prevents the picture tube from burn-in in the event of a malfunction of the vertical deflection stage. If the peak-to-peak value of the sawtooth signal from the vertical deflection stage is too small, the RGB output signals are blanked.

SAFETY – Safety Input (Fig. 4–22)
This input has two thresholds. A signal between the lower and upper threshold means normal function. A signal below the lower threshold or above the upper threshold is detected as malfunction and the RGB signals will be blanked.

HOUT – Horizontal Drive Output (Fig. 4–21)
This open source output supplies the drive pulse for the horizontal output stage. An external pulldown resistor has to be used. The polarity and gating with the flyback pulse are selectable by software.

HFLB – Horizontal Flyback Input (Fig. 4–22)
Via this pin the horizontal flyback pulse is supplied to the VCT 49xxI.

VERT+, VERT– – Vertical Sawtooth Output (Fig. 4–23)
These pins supply the symmetrical drive signal for the vertical output stage. The drive signal is generated with 15-bit precision. The analog voltage is generated by a 4 bit current-DAC with an external resistor of 6.8 kΩ and uses digital noise shaping.

EW – East-West Parabola Output (Fig. 4–24)
This pin supplies the parabola signal for the East-West correction. The drive signal is generated with 15 bit precision. The analog voltage is generated by a 4 bit current-DAC with an external resistor of 6.8 kΩ and uses digital noise shaping.

PWMV – PWM Vertical Output (Fig. 4–35)
This pin provides an adjustable vertical parabola with 7 bit resolution and appr. 79.4 kHz PWM frequency.

DFVBL – Dynamic Focus Vertical Blanking (Fig. 4–35)
This pin supplies the blank pulse for dynamic focus during vertival blanking period or a free programmable horizontal pulse for horizontal dynamic focus generation.

SENSE – Measurement ADC Input (Fig. 4–27)
This is the input of the analog to digital converter for the picture and tube measurement. Three measurement ranges are selectable with RSW1 and RSW2.

GNDM – Measurement ADC Reference Input
This is the reference ground for the measurement A/D converter. Connect this pin to GND.

RSW1 – Range Switch1 for Measuring ADC (Fig. 4–25)
These pin is an open drain pulldown output. During cutoff and white drive measurement the switch is off. During the rest of time it is on. The RSW1 pin can be used as second measurement ADC input for picture beam current measurement.

RSW2 – Range Switch2 for Measuring ADC (Fig. 4–26)
These pin is an open drain pulldown output. During cutoff measurement the switch is off. During white drive measurement the switch is on. Also during the rest of time it is on. It is used to set the range for white drive current measurement.

4.3.6. Controller Pins

XTAL1 – Crystal Input and **XTAL2** Crystal Output (Fig. 4–28)
These pins connect a 20.25 MHz crystal to the internal oscillator. An external clock can be fed into XTAL1.

RESETQ – Reset Input/Output (Fig. 4–29)
A low level on this pin resets the VCT 49xxI. The internal CPU can pull down this pin to reset external devices connected to this pin.

TEST – Test Input (Fig. 4–30)
This pin enables factory test modes. For normal operation, it must be connected to ground.

SCL – I^2C Bus Clock (Fig. 4–31)
This pin delivers the I^2C bus clock line. The signal can be pulled down by external slave ICs to slow down data transfer.

SDA – I^2C Bus Data (Fig. 4–31)
This pin delivers the I^2C bus data line.

P10–**P13, P20**–**P23** – I/O Port (Fig. 4–32)
These pins provide CPU controlled I/O ports.

P14–**P17** – I/O Port (Fig. 4–33)
These pins provide CPU controlled I/O ports. Additionally they can be used as analog inputs for the controller ADC.

P24–**P26, P30**–**P37** – I/O Port (Fig. 4–34)
These pins provide CPU controlled I/O ports.

ADB0–**ADB19** – Address Bus Output (Fig. 4–35)
These 20 lines provide the CPU address bus output to access external memory.

DB0–**DB7** – Data Bus Input/Output (Fig. 4–36)
These 8 lines provide the bidirectional CPU data bus to access external memory.

WRQ – $\overline{\text{Data Write Enable}}$ Output (Fig. 4–35)
This pin controls the direction of data exchange between the CPU and the external data memory device (SRAM).

RDQ – $\overline{\text{Data Read Enable}}$ Output (Fig. 4–35)
This pin is used to enable the output driver of the external data memory device (SRAM) for read access.

PSENQ – $\overline{\text{Program Store Enable}}$ Output (Fig. 4–35)
This pin is used to enable the output driver of the external program memory device (ROM/FLASH) for read access.

PSWEQ – $\overline{\text{Program Store Write Enable}}$ Output (Fig. 4–35)
This pin is used to write into the external program flash memory device.

XROMQ – $\overline{\text{External ROM Enable}}$ Input (Fig. 4–37)
This pin must be pulled low to access the external program memory. **XROMQ** has an internal pull-up resistor.

EXTIFQ – $\overline{\text{Enable External Memory Interface}}$ Input (Fig. 4–37)
This pin must be pulled low to enable the external memory interface. **EXTIFQ** has an internal pull-up resistor.

STOPQ – $\overline{\text{Stop}}$ CPU Input (Fig. 4–37)
Applying a low level during the input phase freezes the realtime relevant internal peripherals such as timers and interrupt controller. **STOPQ** has an internal pull-up resistor.

ENEQ – $\overline{\text{Enable Emulation}}$ Input (Fig. 4–37)
Only if this pin is set to low level, STOPQ and OCF are operational. **ENEQ** has an internal pull-up resistor.

ALE – Address Latch Enable Output (Fig. 4–35)
This signal indicates changes on the address bus.

OCF – Opcode Fetch Output (Fig. 4–35)
A high level driven by the CPU during output phase indicates the beginning of a new instruction.

RSTQ – $\overline{\text{Internal CPU Reset}}$ Input/Output (Fig. 4–38)
This pin is used for emulation purpose only. A low level on this pin resets the CPU. It also indicates an internal reset of the CPU.

Pin Configuration

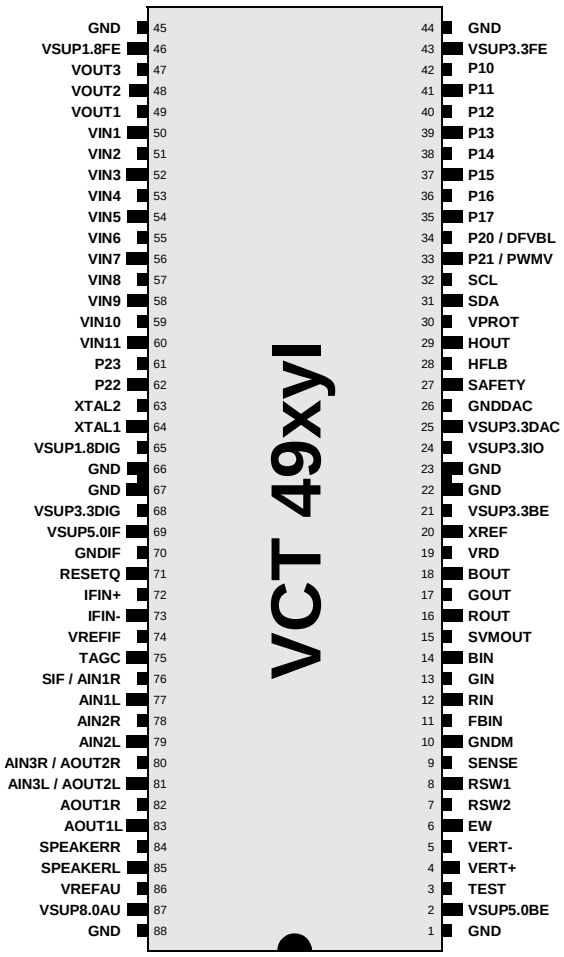

Fig. 4–3: PSSDIP88-1 package

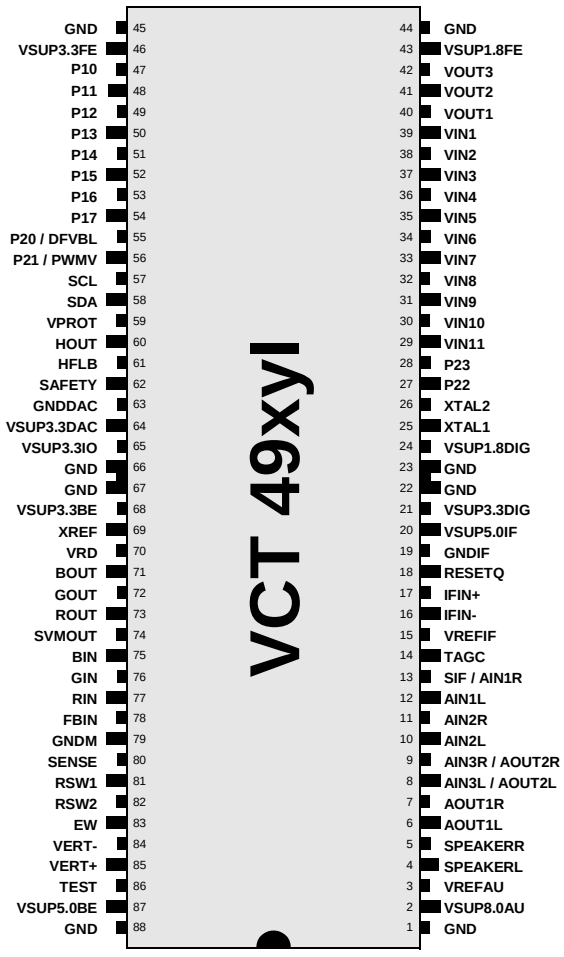

Fig. 4–4: PSSDIP88-2 package (pinning mirrored)