Preliminary

MB8264A-12-W, MB8264A-15-W

NMOS 65,536-Bit Dynamic Random Access Memory With Wide Temperature Range

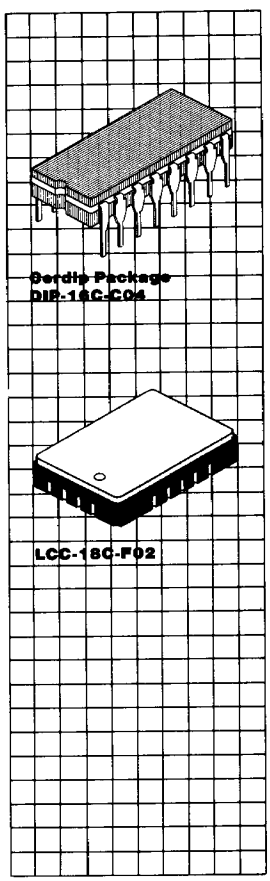
Description

The MB8264A-W is a 64K x 1 dynamic RAM intended for operation over the case temperature range −55°C to 110°C. The part is also available with Fujitsu's 883B high reliability screening.

The MB8264A-W design has been optimized for high speed high performance applications such as mainframe memory, buffer memory, and peripheral storage where low power dissipation, compact layout, or wide temperature range operation are required.

The MB8264A-W has fully TTL compatible inputs and output. It operates on a single +5 V ±10% power supply. An on chip substrate bias generator provides high performance operation. The MB8264A-W contains on-chip latches for the address inputs and for the data input.

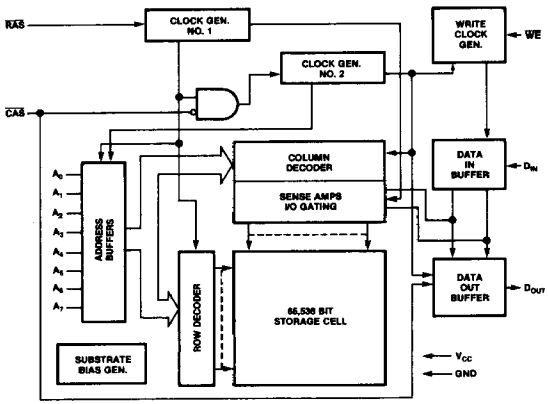
The MB8264A-W is fabricated with Fujitsu's advanced silicon gate NMOS double layer polysilicon process. This process along with the use of single transistor storage cells permits maximum circuit density and minimum chip size. Multiplexed row and column addressing allows the MB8264A-W to be packaged in a standard 16-pin DIP.

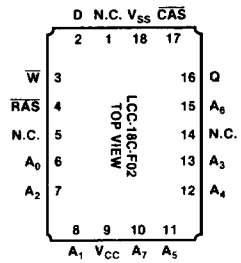


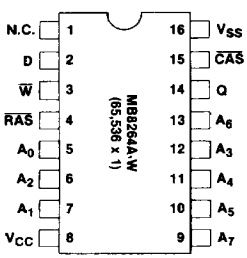
Features

- Wide Temperature Range
  TC = −55°C to 110°C
- 65,536 x 1 organization
- Row Access Time:
  120 ns max. (MB8264A-12-W)
  150 ns max. (MB8264A-15-W)
- Cycle Time:
  230 ns min. (MB8264A-12-W)
  260 ns min. (MB8264A-15-W)
- Low Power (Active)
  305 mW max. (MB8264A-12-W)
  275 mW max. (MB8264A-15-W)
  33 mW max. (Standby)
- 1 ms/128 cycle refresh
- $\overline{RAS}$-Only and Hidden Refresh
- Read-Modify-Write capability
- Page Mode capability
- Common I/O capability using the early write operation
- Output unlatched at cycle end allows extended page boundary
- t_{AR}, t_{WCR}, t_{DHR} are eliminated
- 883B processing available

Block Diagram and Pin Assignments







Capacitance
(T_A = 25 °C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 ~ A_7, D	C_{IN1}	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	C_{IN2}	—	8	pF
Output Capacitance D_{OUT}	C_{OUT}	—	7	pF

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature (case)
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	−55 °C to +110 °C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

AC Characteristics
(Recommended operating conditions unless otherwise noted.)
(Notes 1, 2, 3)

Parameter	Notes	Symbol	MB8264A -12-A Min	MB8264A -12-A Max	MB8264A -15-W Min	MB8264A -15-W Max	Unit
Time between Refresh		t_{REF}	—	1	—	1	ms
Random Read/Write Cycle Time		t_{RC}	230	—	260	—	ns
Read-Write Cycle Time		t_{RWC}	265	—	280	—	ns
Page Mode Cycle Time		t_{PC}	120	—	145	—	ns
Page Mode Read-Write Cycle Time		t_{PRWC}	155	—	180	—	ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}	—	120	—	150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}	—	60	—	75	ns
Output Buffer Turn off Delay		t_{OFF}	0	35	0	40	ns
Transition Time		t_T	3	50	0	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	100	—	100	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	120	10000	150	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	60	—	75	—	ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	50	—	60	—	ns
$\overline{CAS}$ Precharge Time (All cycles except page mode)		t_{CPN}	30	—	30	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	60	10000	75	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	120	—	150	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	20	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	ns
Row Address Set Up Time		t_{ASR}	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	10	—	15	—	ns
Column Address Set Up Time		t_{ASC}	0	—	0	—	ns
Column Address Hold Time		t_{CAH}	15	—	20	—	ns
Read Command Set Up Time		t_{RCS}	0	—	0	—	ns
Read Command Hold Time Reference to $\overline{CAS}$	10	t_{RCH}	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	10	t_{RRH}	20	—	20	—	ns
Write Command Set Up Time	9	t_{WCS}	0	—	0	—	ns
Write Command Hold Time		t_{WCH}	25	—	30	—	ns
Write Command Pulse Width		t_{WP}	25	—	30	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	40	—	45	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	40	—	45	—	ns
Data In Set Up Time		t_{DS}	0	—	0	—	ns
Data In Hold Time		t_{DH}	25	—	30	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	9	t_{CWD}	50	—	60	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	9	t_{RWD}	110	—	120	—	ns

Notes:

1) An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2) AC characteristics assume t_T = 5 ns.
3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5) Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6) Measured with a load equivalent to 2 TTL loads and 100 pF.
7) Operation within the t_{RCD} (max) limit insures that t_{RAC} can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8) t_{RCD} (min) = t_{RAH} (min) + 2t_T (t_T = 5 ns) + t_{ASC} (min).
9) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
   If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
10) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB8264A-12-W	I_{CC1}		55	mA
	MB8264A-15-W			50	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		I_{CC2}		6	mA
REFRESH CURRENT* Average Power Supply Current ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; t_{RC} = min)	MB8264A-12-W	I_{CC3}		40	mA
	MB8264A-15-W			35	
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} = min)	MB8264A-12-W	I_{CC4}		40	mA
	MB8264A-15-W			35	
INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \le V_{IN} \le 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$, all other pins not under test = 0V)		$I_{I(L)}$	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0 \le V_{OUT} \le 5.5$)		$I_{O(L)}$	−10	10	μA
OUTPUT LEVELS Output High Voltage (I_{OH} = −5mA)		V_{OH}	2.4		V
Output Low Voltage (I_{OL} = 4.2mA)		V_{OL}		0.4	V

Note *: I_{CC} is dependent on output loading cycle rates. Specified values are obtained with the output open.

Description

Address Inputs

A total of sixteen binary input address bits are required to decode any 1 of 65,536 storage cell locations within the MB8264A-W. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stabled on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates read mode; logic low dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data is written into the MB8264A-W during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from the transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from the transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode

Page mode operation permits strobing the row-address into the MB8264A-W while maintaining $\overline{RAS}$ at a logic low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

RAS-Only Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

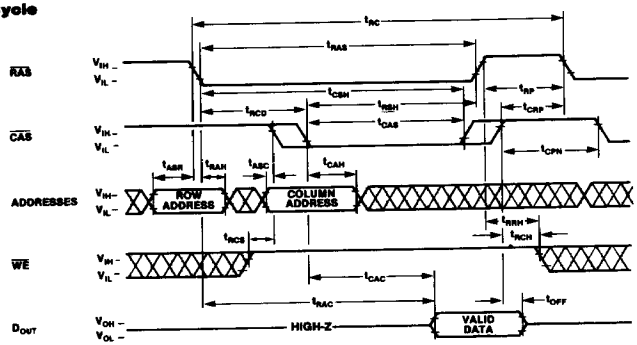
Hidden Refresh

$\overline{RAS}$-ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

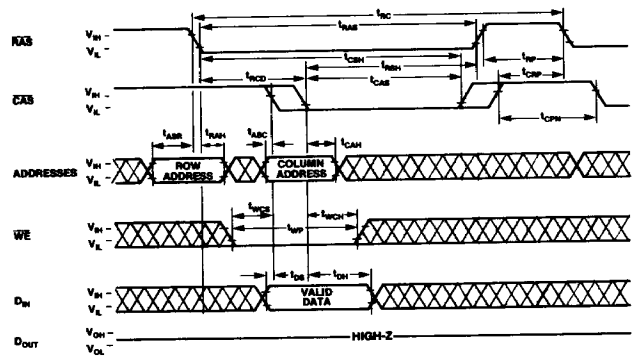
Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

Timing Diagrams

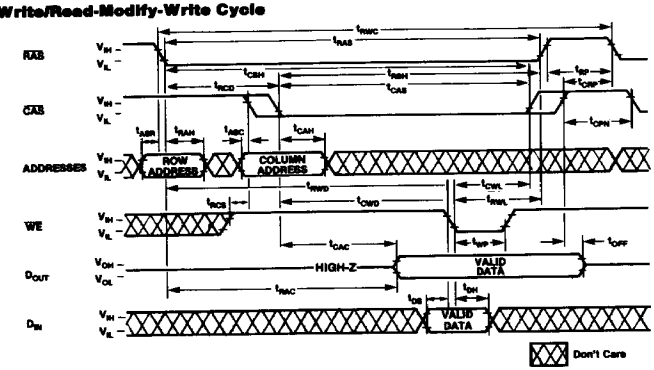
Read Cycle



Write Cycle (Early Write)

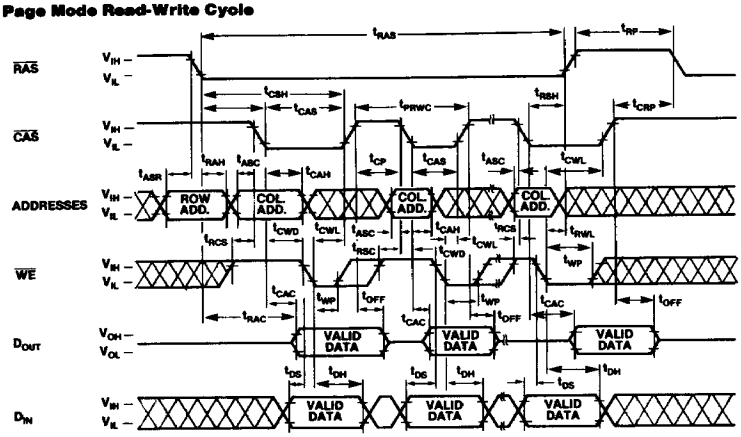


Read-Write/Read-Modify-Write Cycle



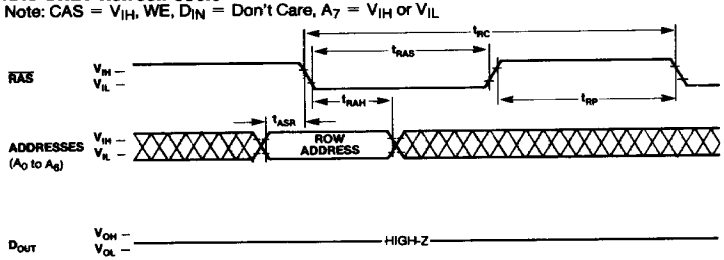
Timing Diagrams, Continued

Page Mode Read-Write Cycle

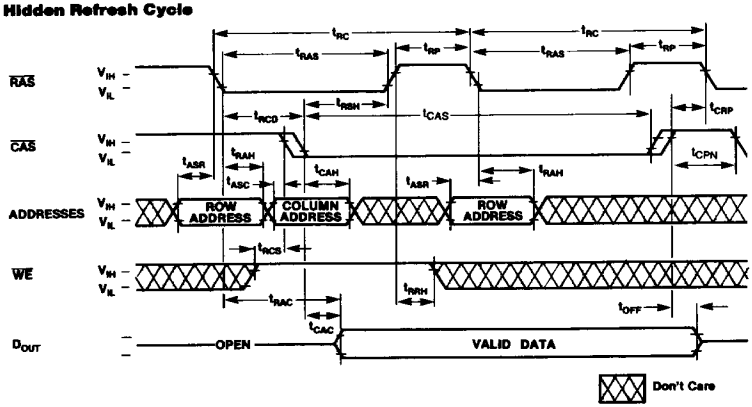


RAS-ONLY Refresh Cycle

Note: CAS = V_{IH}, WE, D_{IN} = Don't Care, A_7 = V_{IH} or V_{IL}

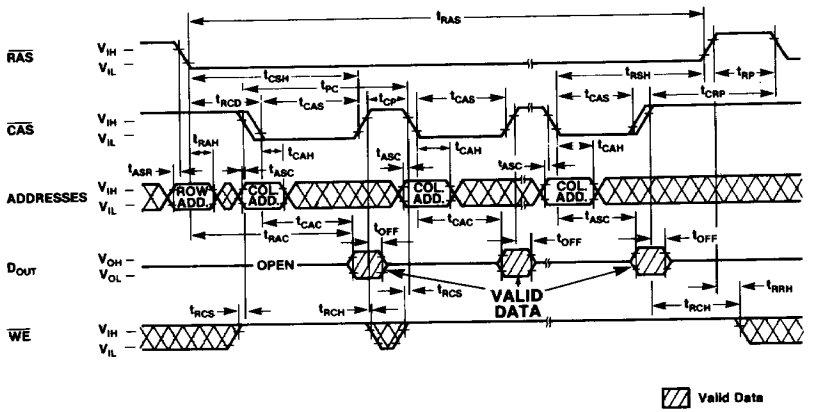


Hidden Refresh Cycle



Timing Diagrams, Continued

Page Mode Read Cycle



Page Mode Write Cycle