# Power Management Unit for Imaging Modules

# ADP5020

## FEATURES

**Input voltage range: 2.4 V to 5.5 V**
**Low standby current: 1 µA**
**Switching frequency: 3 MHz**
**I²C interface**
**Synchronous Buck 1 regulator: 600 mA**
**Synchronous Buck 2 regulator: 250 mA**
**Low dropout regulator (LDO): 150 mA**
**Internal compensation**
**Internal soft start**
**Thermal shutdown**
**20-lead 4 mm × 4 mm LFCSP**

## APPLICATIONS

**Digital cameras, handsets**
**Mobile TVs**

## TYPICAL APPLICATIONS CIRCUIT

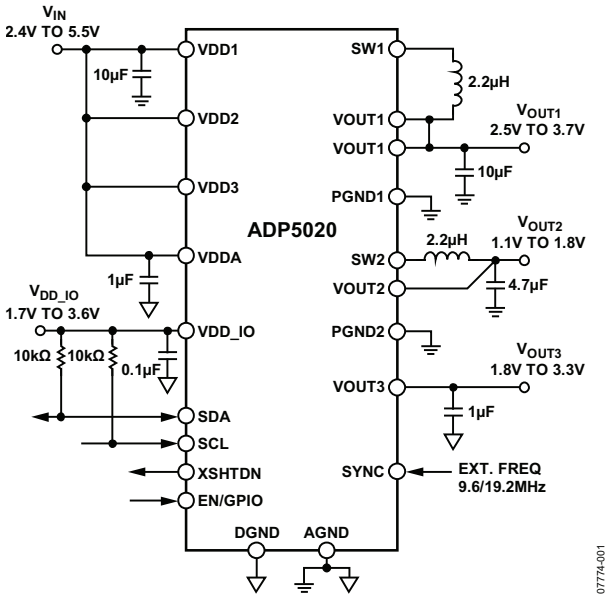


*Figure 1.*

## GENERAL DESCRIPTION

The ADP5020 provides a highly integrated power solution that includes all of the power circuits necessary for a digital imaging module. It comprises two step-down dc-to-dc converters, one LDO, and a power sequence controller. All dc-to-dc converters integrate power pMOSFETs and nMOSFETs, making the system simpler and more compact and reducing the cost. The ADP5020 has digitally programmed output voltages and buck converters that can source up to 600 mA. A fixed frequency operation of 3 MHz enables the use of tiny inductors and capacitors. The buck converters use a voltage mode, constant-frequency PWM control scheme, and the synchronous rectification is implemented to reduce the power loss. The Buck 1 regulator operates at up to 93% efficiency.

The ADP5020 provides high performance, reduces component count and size, and is lower in cost when compared to conventional designs.

The ADP5020 runs on input voltage from 2.4 V to 5.5 V and supports one-cell lithium-ion (Li+) batteries. The high performance LDO maximizes noise suppression. The ADP5020 can be activated via an I²C® interface or through a dedicated enable input. During logic-controlled shutdown, the input is disconnected from the output source, and the part draws 1 µA typical from the input source. Other key features include undervoltage lockout to prevent deep-battery discharge and soft start to prevent input current overshoot at startup. The ADP5020 is available in a 20-lead LFCSP.

**Rev. 0**


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## REVISION HISTORY

**4/09—Revision 0: Initial Version**

# FUNCTIONAL BLOCK DIAGRAM

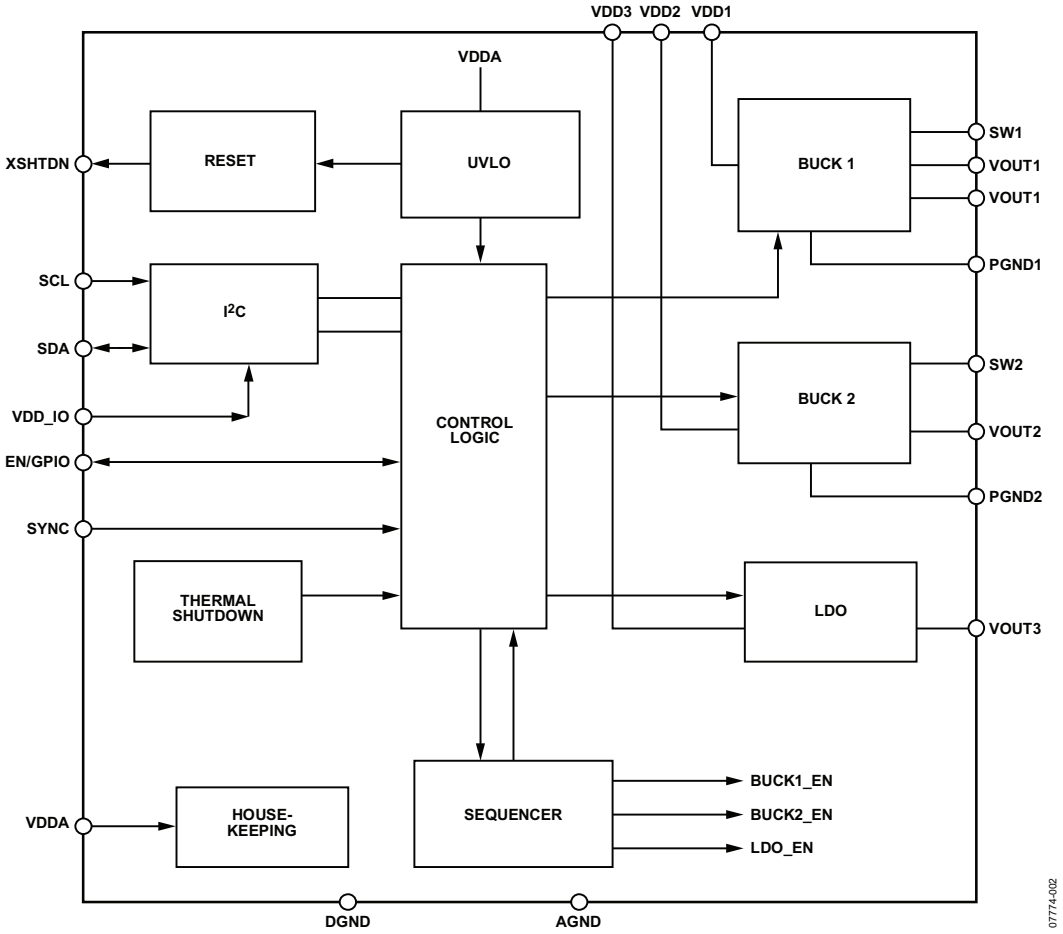


*Figure 2.*

# SPECIFICATIONS

$T_J$ = −40°C to +125°C, $V_{DDx}$ = 3.6 V, $V_{DD\_IO}$ = 1.8 V, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OPERATING RANGE | | | | | | |
| VDDx Operating Voltage Range | $V_{DD}$ | | 2.4 | | 5.5 | V |
| Logic I/O Operating Voltage Range[1] | $V_{DD\_IO}$ | | 1.7 | | 3.6 | V |
| EN, SDA, SCL CHARACTERISTICS | | | | | | |
| Low Level Input Voltage | $V_{IL}$ | | | | $0.3 \times V_{DD\_IO}$ | V |
| High Level Input Voltage | $V_{IH}$ | | $0.7 \times V_{DD\_IO}$ | | | V |
| INPUT LOGIC CURRENT | $I_{LK}$ | Internal pull-down, 1 MΩ | −1 | | +6 | µA |
| XSHTDN, EN/GPIO | | | | | | |
| Low Level Output Voltage | $V_{OL}$ | $I_{RST}$ = +3 mA | | | $0.2 \times V_{DD\_IO}$ | V |
| High Level Output Voltage | $V_{OH}$ | $I_{RST}$ = −3 mA | $0.8 \times V_{DD\_IO}$ | | | V |
| OUTPUT LOGIC LEAKAGE CURRENT | $I_{LK}$ | | | | 1 | µA |
| UNDERVOLTAGE LOCKOUT THRESHOLD | | | | | | |
| Falling | $V_{UVLOF}$ | Referenced to $V_{DDA}$ | 1.8 | 2.0 | | V |
| Rising | $V_{UVLOR}$ | Referenced to $V_{DDA}$ | | 2.2 | 2.4 | V |
| POWER-ON RESET THRESHOLD | | | | | | |
| Falling | $V_{PORF}$ | Referenced to $V_{DDA}$ | 1.0 | 1.4 | | V |
| Rising | $V_{PORR}$ | Referenced to $V_{DDA}$ | | 1.6 | 1.7 | V |
| UVLO GLITCH DEBOUNCE TIME | | $V_{DD}$ > POR levels | | 50 | | µs |
| SHUTDOWN OUTPUT DURATION[2] | $t_{XSHTDN}$ | XSHTDN line driven low | | 1 | | ms |
| POWER GOOD (POK) ACTIVATION DELAY TIME[3] | | | | | | |
| EN to First Regulator | $t_{REG1}$ | | | 5 | | ms |
| First to Second Regulator | $t_{REG2}$ | | | 5 | | ms |
| Second to Third Regulator | $t_{REG3}$ | | | 5 | | ms |
| NO LOAD CURRENT CHARACTERISTICS | | | | | | |
| Standby Current | $I_{Q(STNBY)}$ | EN = 0 | | 1 | 5 | µA |
| Lockout Current | $I_{LOCK}$ | EN = 0, $V_{DDA} < V_{UVLOF}$ | | 1 | 1 | µA |
| Operating Quiescent Current, Switching[4] | $I_Q$ | $I_{LOAD}$ = 0 mA | | 10 | 15 | mA |
| THERMAL CHARACTERISTICS | | | | | | |
| Thermal Shutdown, $T_J$ Rising | $T_{SD}$ | | | 150 | | °C |
| Thermal Shutdown Hysteresis | | | | 30 | | °C |
| HOUSEKEEPING BLOCK | | | | | | |
| Power Good Threshold | $V_{PG}$ | | 70 | 80 | 90 | % |

[1] The $V_{DD\_IO}$ voltage must be less than or equal to the level on the $V_{DDx}$ supply lines.
[2] Shutdown output duration is automatic when using the EN pin. To get this delay when using I²C, FORCE_XS must be set to 1.
[3] Activation delays apply only when the device is activated through the EN pin or the EN_ALL bit (Address 0x03[4]); the sequencer controls the turning on of the regulators.
[4] The quiescent current is calculated as though all regulators are powered up.

## SWITCHING SPECIFICATIONS

**Table 2.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SWITCHING FREQUENCY | | | | | | |
| CH1 | $f_{SW1}$ | Sync disabled | 2.5 | 3 | 3.6 | MHz |
| CH2 | $f_{SW2}$ | Sync disabled | 2.5 | 3 | 3.6 | MHz |
| SYNC CLOCK DIVIDER RATIO | | | | | | |
| | $RATIO_{DIV}$ | SYNC_9P6 = 1 | | 3 | | |
| | $RATIO_{DIV}$ | SYNC_19P2 = 1 | | 6 | | |
| SYNC CHARACTERISTICS | | | | | | |
| Frequency Range | | | | | | |
| | $f_{SYNC1}$ | | | 9.6 | | MHz |
| | $f_{SYNC2}$ | | | 19.2 | | MHz |
| Frequency Duty Cycle | $f_{SYNCDUTY}$ | | 40 | 50 | 60 | % |
| Signal | | | | | | |
| DC Coupling Level | | | | | | |
| Low Level Input Voltage | $V_{IL}$ | | | | $0.3 \times V_{DD\_IO}$ | V |
| High Level Input Voltage | $V_{IH}$ | | $0.7 \times V_{DD\_IO}$ | | | V |
| DC Coupling | $V_{SYNC}$ | | 0 | | $V_{DD\_IO}$ | V |
| AC Coupling Level | $V_{CAC-PP}$ | Sine wave, peak-to-peak | 0.5 | 1.0 | $V_{DD\_IO}$ | V |
| AC Coupling Capacitor | | | | 10 | | nF |
| Input Current | $I_{SYNC}$ | SYNC_9P6 = 1, or SYNC_19P2 = 1 | | 50 | | µA |

## DC-TO-DC CONVERSION SPECIFICATIONS, BUCK 1 REGULATOR

**Table 3.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | | | | | | |
| Range[1] | $V_{OUT1}$ | 3-bit range | 2.5 | | 3.7 | V |
| Initial Accuracy | | $T_A$ = 25°C, $V_{DD1}$[2], $V_{OUT1}$ = 3.3 V, $I_{LOAD}$ = 20 mA | −1 | | +1 | % |
| Total Accuracy | | $V_{DD1}$[3], $I_{LOAD}$ = 50 mA to 600 mA | −5 | | +4 | % |
| VOUT1 REGULATION | | | | | | |
| Load Regulation | | $I_{LOAD}$ = 20 mA to 600 mA | | 0.2 | | % |
| Line Regulation | | $V_{DDA}$ = 1.8 V, $V_{DD1}$[2,3] | | 0.15 | | % |
| CURRENT | | | | | | |
| Maximum Output Current | $I_{BK1MAX}$ | $V_{DD1}$[3], $V_{OUT1}$ = 2.5 V to 3.7 V | | | 600 | mA |
| Quiescent Current | $I_{QBK1}$ | $I_{LOAD}$ = 0 mA | | 4 | 6 | mA |
| POWER | | | | | | |
| Low-Side Power nMOSFET | $R_{DSON1}$ | $I_D$ = 400 mA | | 175 | 250 | mΩ |
| High-Side Power pMOSFET | $R_{DSON1}$ | $I_D$ = 400 mA | | 250 | 400 | mΩ |
| SWITCH CURRENT LIMIT | $I_{CL1}$ | | 0.8 | 1.2 | 1.6 | A |
| MINIMUM ON TIME | $t_{MIN1}$ | | | 55 | | ns |
| MAXIMUM DUTY CYCLE | $D_{MAX1}$ | | | 88 | 95 | % |
| SOFT START TIME | $t_{SS1}$ | | | 1.4 | | ms |
| $C_{OUT}$ DISCHARGE SWITCH ON RESISTANCE | $R_{DIS1}$ | | 0.7 | 1 | 1.3 | kΩ |

[1] See Table 13 (the BUCK1_VSEL register, Address 0x01) for details.
[2] $V_{DD1}$ = 3.1 V to 5.5 V, $I_{LOAD}$ is less than 200 mA. For tight regulation, the supply voltage must be 0.6 V higher than the output voltage.
[3] $V_{DD1}$ = 3.7 V to 5.5 V, $I_{LOAD}$ is more than 200 mA. For tight regulation, the supply voltage must be 1.2 V higher than the output voltage.

## DC-TO-DC CONVERSION SPECIFICATIONS, BUCK 2 REGULATOR

**Table 4.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | | | | | | |
| Adjustable Range[1] | $V_{OUT2}$ | 4-bit range | 1.1 | | 1.8 | V |
| Initial Accuracy | | $T_A$ = 25°C, $V_{DD2}$ = 3.6 V, $V_{OUT2}$ = 1.2 V, $I_{LOAD}$ = 20 mA | −1 | | +1 | % |
| Total Accuracy | | $V_{DD2}$ = 2.5 V to 5 V, $I_{LOAD}$ = 10 mA to 250 mA | −5 | | +4 | % |
| Load Regulation | | $I_{LOAD}$ = 10 mA to 250 mA | | 0.2 | | % |
| Line Regulation | | $V_{DDA}$ = 1.8 V, $V_{DD2}$ = 2.5 V to 5 V | | 0.15 | | % |
| CURRENT | | | | | | |
| Maximum Output Current | $I_{BK2MAX}$ | | | | 250 | mA |
| Quiescent Current | $I_{QBK2}$ | $I_{LOAD}$ = 0 mA | | 4 | 6.5 | mA |
| POWER | | | | | | |
| Low-Side Power nMOSFET | $R_{DSON2}$ | $I_D$ = 200 mA | | 240 | 330 | mΩ |
| High-Side Power pMOSFET | $R_{DSON2}$ | $I_D$ = 200 mA | | 300 | 450 | mΩ |
| SWITCH CURRENT LIMIT | $I_{CL2}$ | | 360 | 630 | 850 | mA |
| MINIMUM ON TIME | $t_{MIN2}$ | | | 55 | | ns |
| MAXIMUM DUTY CYCLE | $D_{MAX2}$ | | | 87.5 | 90 | % |
| SOFT START TIME | $t_{SS2}$ | | | 900 | | µs |
| $C_{OUT}$ DISCHARGE SWITCH ON RESISTANCE | $R_{DIS2}$ | | 0.7 | 1 | 1.3 | kΩ |

[1] See Table 14 (the BUCK2_LDO_VSEL register, Address 0x02) for details.

## VOUT3 SPECIFICATIONS, LOW DROPOUT (LDO) REGULATOR

**Table 5.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT VOLTAGE | | | | | | |
| Adjustable Range[1] | $V_{OUT3}$ | 100 mV step, 4-bit range | 1.8 | | 3.3 | V |
| Initial Accuracy | | $T_A$ = 25°C, $V_{DD3}$ = 3.6 V, $V_{OUT3}$ = 1.8 V, $I_{LOAD}$ = 10 mA | −1.5 | | +1.5 | % |
| Total Accuracy | | $V_{DD3}$ = 2.5 V to 5 V, $I_{LOAD}$ = 0 mA to 150 mA | −5 | | +4 | % |
| Load Regulation | | $I_{LOAD}$ = 10 mA to 100 mA | | 0.45 | 0.75 | % |
| Line Regulation | | $I_{LOAD}$ = 100 mA[2] | | 0.15 | 0.30 | % |
| CURRENT | | | | | | |
| Maximum Output Current | $I_{LDOMAX}$ | | | | 150 | mA |
| Dropout Voltage | $V_{LDODROP}$ | At 100 mA, $V_{OUT3}$ = 3.3 V | | 70 | 100 | mV |
| Quiescent Current | $I_Q$ | $I_{LOAD}$ = 0 mA | | 45 | 85 | µA |
| Short-Circuit Current Limit | | | 200 | 400 | 600 | mA |
| Power Supply Rejection Ratio | PSRR | | | | | |
| | | f = 1 kHz, $V_{DD3}$ = 5 V, $V_{OUT3}$ = 3.3 V, $I_{LOAD}$ = 50 mA | | 47 | | dB |
| | | f = 10 kHz, $V_{DD3}$ = 5 V, $V_{OUT3}$ = 3.3 V, $I_{LOAD}$ = 50 mA | | 44 | | dB |
| SOFT START TIME | $t_{SS2}$ | | | 70 | | µs |
| $C_{OUT}$ DISCHARGE SWITCH ON RESISTANCE | $R_{DIS8}$ | | 0.7 | 1 | 1.3 | kΩ |

[1] See Table 14 (the BUCK_LDO_VSEL register, Address 0x02) for details.
[2] $V_{DD3} > V_{OUT3} + L_{DODROP}$.