System Control

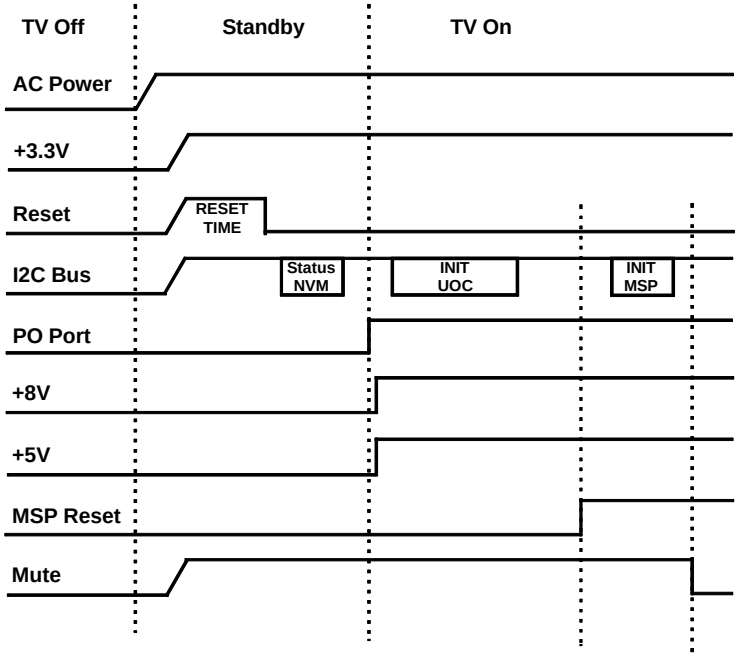
System control for the ITC008 is housed in the Ultimate One Chip IV001. User interface is via IR at pin 64 and key scan at pins 6 and 7 of IV001. The UOC operates on +3.3Vdc for system control half and 12Mhz system clock. An external EEPROM (IR001) is used to store alignment and user setup data.

Communication with the rest of the chassis and Alert Guard is via I2C. Besides Alert Guard, there are three devices that communicate with IV001:

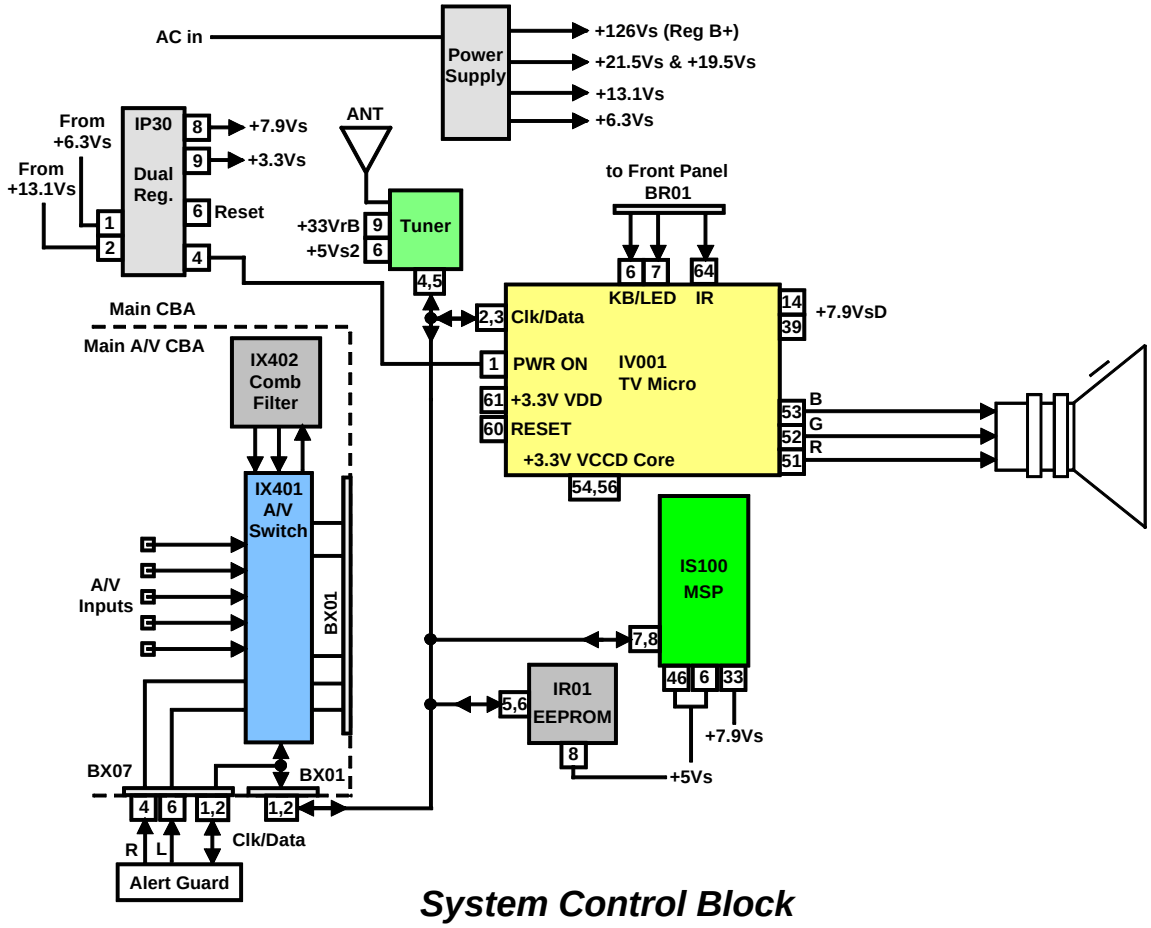
- Multi-Sound Processor (IS100)
- Video IC (IX401)
- Tuner

If communication is not established with these devices, IV001 will try three times to start and then will shutdown throwing an error code. This type of shutdown is considered a soft shutdown and can be disabled by accessing the service mode. When entering the service mode, acknowledgment checking is disabled allowing the set to start in the service mode.

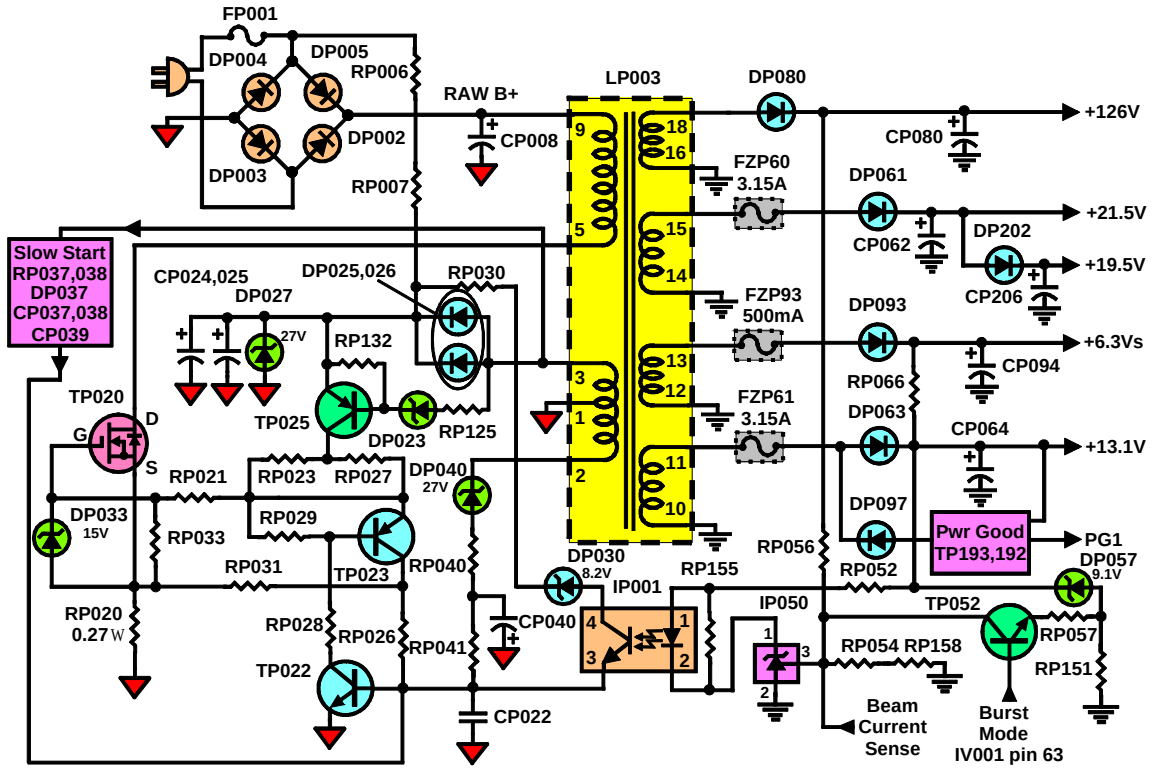
Because IV001 performs all major functions of the set, it is suggested great care be taken when determining a failure with IV001. All supply voltages and pin voltages should be checked prior to replacing IV001.



Power On Timing



System Control Block



Power Supply Block

Power Supply

The ITC008 power supply is similar to the one used in the TX809 chassis. One major difference is the ITC008 has five (5) major power supplies developed off the secondary of LP003, 126VDC, 21.5Vdc, 13.1Vdc, 19.5Vdc and the 6.3Vdc. Secondary regulation of the 13.1Vdc comes from IP30 dual voltage regulator producing the standby +3.3Vs for system control. See run supply for additional information about the +3.3Vs.

Raw B+ (150VDC) is generated by a full wave bridge rectifier (DP002/3/4/5) and is applied to LP003, pin 9 that serves as the B+ source for the output transistor TP020. Output transistor TP020 provides the drive to transformer LP003. The oscillator driver circuit consists of transistors TP022, TP023 and TP025. The output of the oscillator driver is applied to the gate of TP020 and turns on and off the output transistor. Opto Isolator (IP001) provides the regulation feedback from the secondary side of the supply. IP001 also provides electrical isolation between the primary and secondary side of the supply, isolating the HOT ground from Cold ground.

By tapping a voltage from the bridge rectifier and applying it to the oscillator driver via RP006 and RP007 initial startup is generated. The re-supply or run voltage for the oscillator driver comes from rectifying the pulse at pin 3 of LP003 via DP025 & DP026. The re-supply voltage is coupled back to IP001-4 via Zener DP030 and

serves as B+ for the phototransistor in IP001. The pulse from LP003, pin 3 is also applied to DP023 and is used to trigger the oscillator driver.

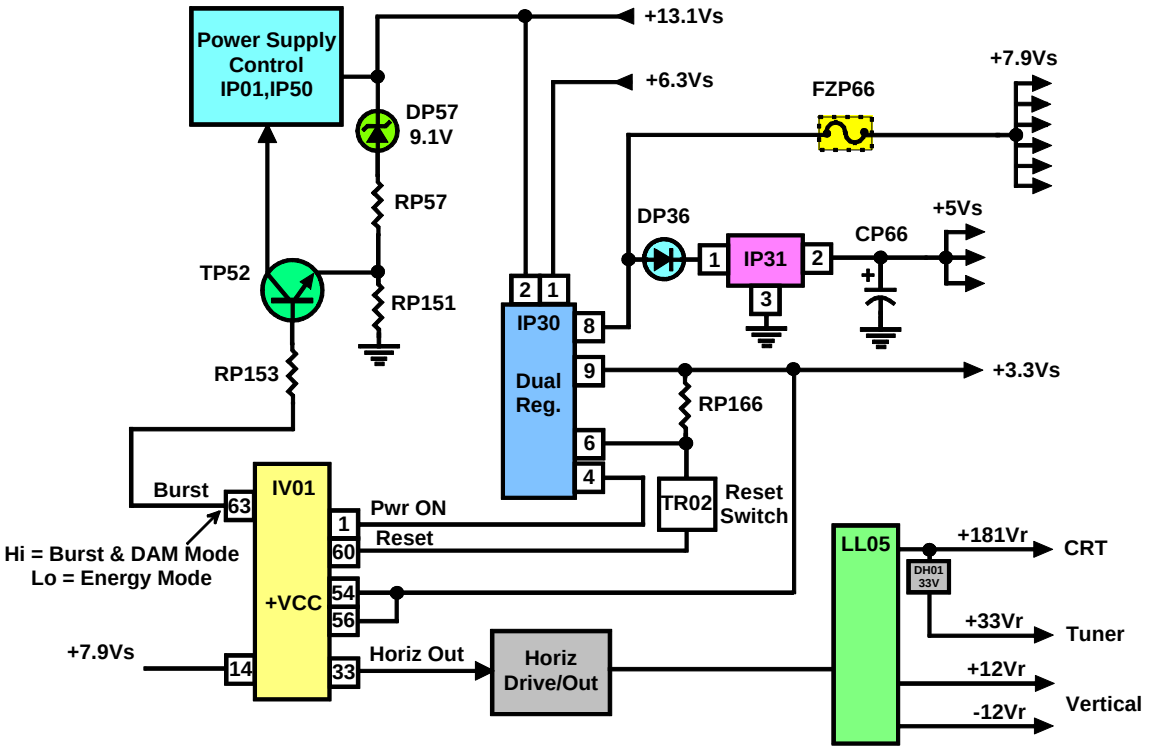
Turn off of TP020 occurs when the current through RP020 increases to the trigger point of TP022. Once the voltage drop across RP020 rises to the predetermined trigger point, the oscillator driver turns off, removing drive from TP020. Diode DP040 (27V zener) is used as a protective device to prevent runaway in the event of a failure in the regulation feedback path.

IP050 (precision shunt regulator) controls or regulates IP001 (opto isolator). The voltage applied to pin 3 determines the resistance of IP050. As the voltage on pin 3 of IP50 drops, the resistance decreases. This effectively pulls pin 2 of IP001 closer to ground turning on the photo diode harder. This generates more light and turns on the phototransistor harder. When the phototransistor is turned on harder, this pulls current away from the oscillator driver circuit causing the duty cycle of the power supply to increase (the output device stays on longer). With an increase in duty cycle, the supply outputs more power thus raising the secondary voltages.

There are three inputs to the regulator feedback circuit (IP050, pin 3). First, the 126Vdc is monitored to regulate the standby supply whenever the television is turned on. Second, when the set is turned off but still plugged in, +13.1Vdc is monitored to regulate the power supply via zener DP057 and TP052. During standby (set off) the system control microcomputer (IV001-63) outputs a Burst signal that turns on TP052. The impedance of the standby switch circuit (TP052) is much lower than the run regulation circuit (126Vdc). This allows the standby feedback voltage (+13.1V) to over ride any effect the run feedback voltage (126V) might have. Third, during operation (set on), a beam current sense voltage is applied to pin 3 of IP050. During a high beam current situation, pin 3 of IP050 is pulled down causing pin 1 to fall. This turns on the opto coupler harder which causes the oscillator driver to increase the duty cycle thus pulling up the power supply. This is done to reduce the “breathing” effect during high beam current conditions.

The standby supply has two safety shutdowns. These are over voltage and over current shutdown. Over voltage shutdown occurs if the voltage developed at pin 3 of LP003 rises above 27 volts. Zener DP027 breaks over and shorts removing re-supply and start voltages. Over current protection is provided by RP020 in the source of TP020. Excessive current causes the voltage developed across RP020 to rise hi enough to turn on TP022, again turning TP023 shorting gate drive of TP020 to ground.

The ITC008 also uses circuit protectors (fuses) in the power circuits. The chart on page 30 shows the location and power supply associated with the device.



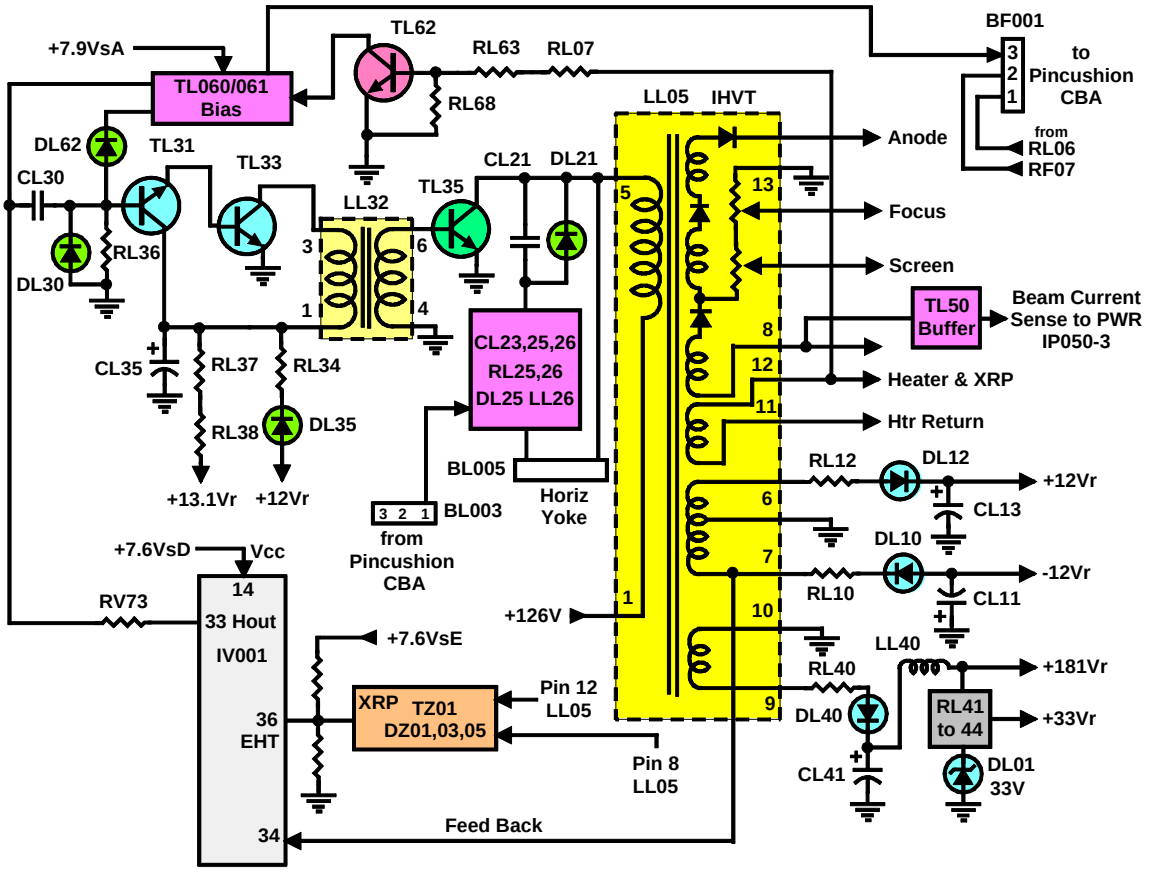
Switched Power Supply Block

Switched Power Supply

The switched supply consists of two (2) regulated supplies and four (4) scan derived supplies. The regulated supplies are +7.9Vs and +5Vs. IP30 (dual voltage regulator) produces the +7.9Vs and the +3.3Vs. The +5Vs is derived from IP31 (5V Reg) that is fed by the switched +7.9Vs. The non-switched +3.3Vs from pin 9 of IP30 is active as long as the +6.3Vs is present at pin 1. The +3.3Vs is used for IV01 (System Control) reset (IP30-6) and VCC pin 54,56.

The switched voltage from IP30 pin 8 (+7.9Vs) is activated when pin 4 goes high from the power on (IV01 pin 1). The Burst (High) from IV01-63 turns on TP52 increasing the stand-by supply current to compensate for the additional load during power up.

When IP30 gets the power on signal, +7.9Vs from pin 8 gets applied to pin 14 of IV01 supplying B+ for Horizontal drive. Horizontal drive from IV01 pin 33 drives the driver / Output stage of horizontal. The output stage drives LL05 producing four (4) scan derived supplies. The +181Vr is used for CRT drive and supplying DH001 (33V Zener). DH001 and it's associated circuit produce the tuner voltage +33Vr. Vertical + and – 12Vr are also developed by LL05.



Horizontal Block

Horizontal Deflection

Horizontal deflection starts with drive from IV001 pin 33. Drive is produced when the +7.6Vsd is present at pin 14 of IV001. The drive signal is coupled to TL31 via RV73 and CL30. The +13.1Vr provides B+ to TL31 and TL33 until the +12Vr comes up and re-supplies the B+. LL32 couples the drive signal to the output TL35. TL35 drives the fly-back transformer LL05, producing the scan-derived voltages. Feed back from pin 12 of LL05 is used as a slow start bias for TL31 and TL33.

The horizontal output signal is generated by means of an oscillator that is running at 25Mhz and is stabilized with 12Mhz reference. A digital control circuit that is locked to the reference signal of the color decoder determines the free running frequency of the oscillator. When IV001 is switched-on the horizontal output signal is suppressed and the oscillator is calibrated. When all sub-address bytes have been sent via I²C bus to IV001 and the frequency of the oscillator is correct, the horizontal drive signal is switched on. To obtain a smooth switching on and switching off of the horizontal output stage, an internal soft start/stop function is used. To protect the horizontal output transistor, the horizontal drive is immediately switched off when a power on reset is detected.

IV001 has a second control loop to guarantee the drive pulse for the horizontal output stage. The horizontal output is gated with the fly-back reference pulse (LFB pin 34), so that the horizontal output transistor cannot be switched on during that time.

All geometry alignments are done via I^2C bus commands except E/W alignment. X-ray protection is activated via EHT tracking (IV001 pin 36) when the level exceeds +3.9V. If the level exceeds +3.9V at pin 36, horizontal drive will be stopped at pin 33 shutting down horizontal drive and the set.

The horizontal drive output is an open collector configuration. Thus an AC coupled Darlington driver (TL31 and TL32) is used. Before startup, the capacitor CL35 is charged by +13.1Vr via RL37 and RL38. When the H drive signals are starting the T-on time is very short and the energy stored in CL35 is enough to supply the driver. Because the +12Vr supply is generated in forward mode the first pulses charge CL13. Once CL13 is charged the supply voltage for the driver is coming from the +12Vr via DL35 and RL 34.

E/W Correction

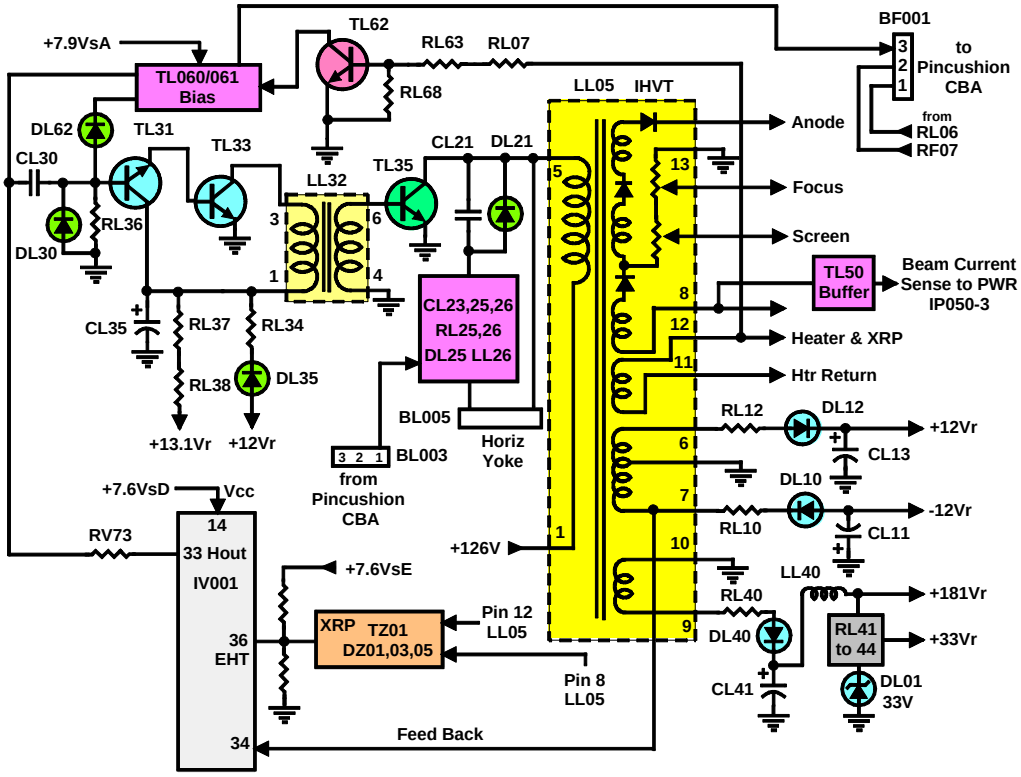
An external E/W correction-driving signal is produced by making use of synchronized vertical feedback signal derived from RF07 off pin 2 of BF001. The saw tooth is amplified and inverted before being fed into an integrator (IL101) to generate a parabola signal. PL141 acts as an E/W amplitude control by controlling the parabola signal amplitude. PL140 is part of the voltage divider that determines the DC level used for horizontal size alignment. The horizontal breathing is controlled by the beam current information via RL150 to the DC level biasing at PL140. The trapezium alignment is achieved by introducing the inverted saw tooth waveform to the parabola output signal.

A safety circuit RL112, RL113, DL113 DL114, CL110, CL114, CL123, RL110, DL117, DL118, RL117, RL118, and DL119 is to inhabit the H-drive and shut down the deflection circuit in the case of TL101 failure.

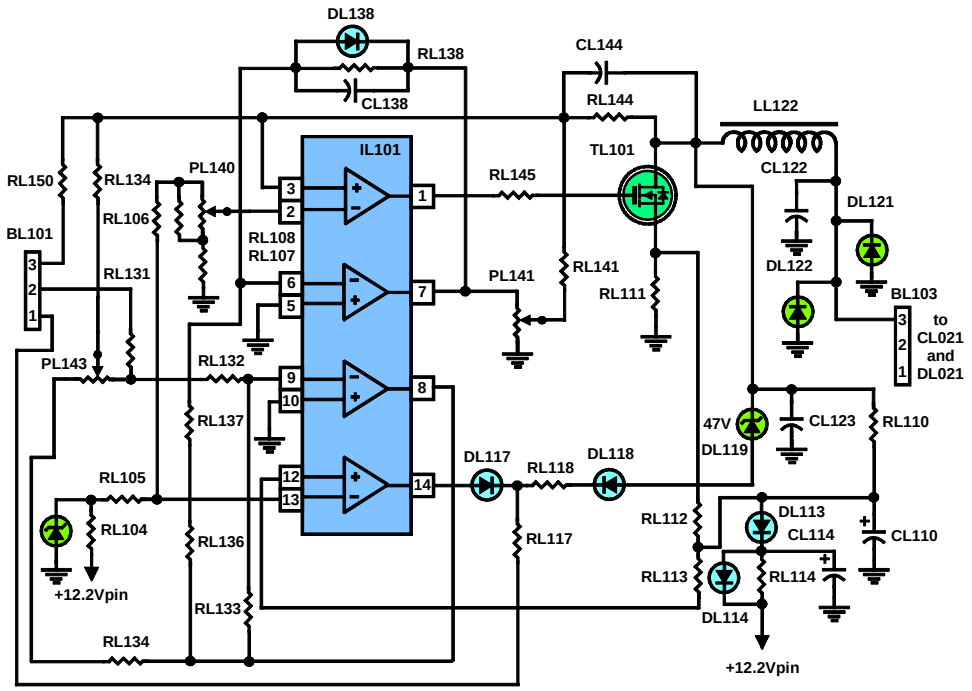
A diode modulator (DL21, CL21 (main CBA), DL121, DL122 and CL122 (Pincushion CBA) is used to modulate the horizontal deflection current with vertical frequency in order to obtain higher amplitude of deflection current in the middle and smaller amplitude on the top and bottom of the raster.

The resonant frequency LC product of bridge coil LL122 and CL122 in series connected with CL123 is the same as the product of tuning capacitor CL21 together with the deflection yoke. The capacitive divider CL21 and CL122 produces a retrace voltage across CL122. The integrated value of this voltage is corresponded by the

voltage across CL123. A maximum voltage across CL123 means the deflection current is minimal and vice versa.



Horizontal Block



E/W Correction Block

Vertical Deflection

The ITC008 vertical deflection circuit consists of vertical ramp generator in IV001 processor and a power stage IF001. The vertical ramp generator is in the TV processor IV001. The geometry parameters can be adjusted via the I^2C bus to control TV processor IV001. Four parameters Vertical Slope, Vertical Amplitude, Vertical Shift and S Correction are all controlled by software.

The power stage, IF001, is configured as differential amplifier and driven by the ramp current delivered by IV001 pin 21 and pin 22. The vertical ramp current (Ir) is imposed on the V-drive signals. So we have I+Ir and I-Ir from pin 21 and pin 22 respectively.

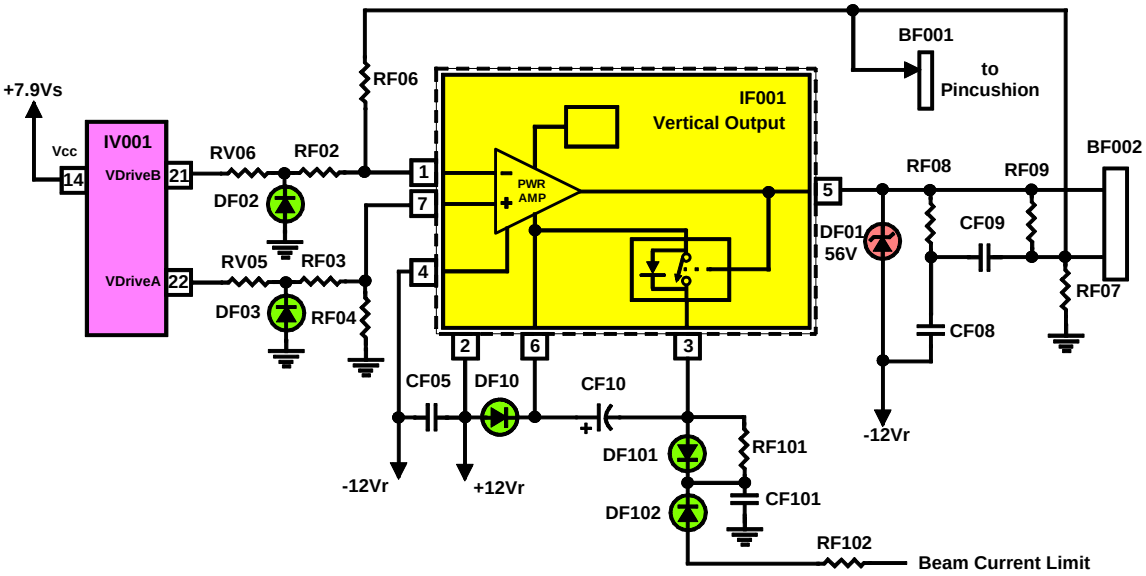
The fly-back supply voltage on pin 5 is 2 x Vsupply + |-Vsupply| and the maximum scanning supply voltage on pin 5 is Vsupply or -Vsupply. Pin 3 voltage is at -Vsupply and CF10 is charged to Vsupply + |-Vsupply| during scanning period. The fly-back generator switches pin 3 to Vsupply. Thus the total fly-back supply voltage is: 2 x Vsupply + |-Vsupply|.

CF08/09-RF08 is the zero-pole compensation to increase the phase margin of the amplifier while still maintaining expected bandwidth. RF08 is a fusible resistor to prevent overheating in the event of CF08/09 failure. This circuit also helps to protect the IC during picture tube arcing. DF01 also protects the vertical IC during picture tube arcing.

Resistor RF09 damps spurious oscillation in the VDC and reduces crosstalk from the HDC into the VDC.

RF07 is a current sensing resistor. The deflection current is proportional to the output voltage across RF07.

RF101, DF101, DF102, RF102 and CF101 act as a protection circuit to pull down the Beam Current Limit path as to suppress the video amplitude during vertical booster IC failure. This prevents CRT screen phosphor from burning by intense white line.



Vertical Block