STR-X6700 Series Off-Line Quasi-Resonant Switching Regulators

Introduction

The STR-X6700 series integrates a quasi-resonant control IC and a MOSFET with avalanche guarantee. In normal operation, the device provides high efficiency and low EMI noise with bottom-skip quasi-resonant operation during light output loads. Low power consumption is also achieved by Auto-standby mode (not available in the STR-X6729, STR-X6759N, or STR-X6768N) or manual standby mode (external trigger).

The device is supplied in a seven-pin fully-molded TO-3P-style package, which is suitable for downsizing and standardizing of an SMPS by reducing external component count and simplifying circuit design.

Features and benefits include the following:

- Auto standby mode (burst oscillation) or manual standby mode (UVLO intermittent oscillation) in the standby mode.
- In addition to the standard quasi-resonant operation, a bottom-skip mode is available for increased efficiency from light to medium load.
- Soft-start operation at start-up.
- Reduced switching noise (compared to conventional PWM hard-switching solution) with a step-drive function.
- Built-in avalanche-energy-guaranteed power MOSFET (to simplify surge-absorption circuit; no V_{DSS} derating is required).
- Overcurrent protection (OCP), overvoltage protection (OVP), overload protection (OLP), and maximum On-time control circuits are incorporated; OVP and OLP go into a latched mode.

The product lineup for the STR-X6700 series provides the options shown in table 1.

Contents

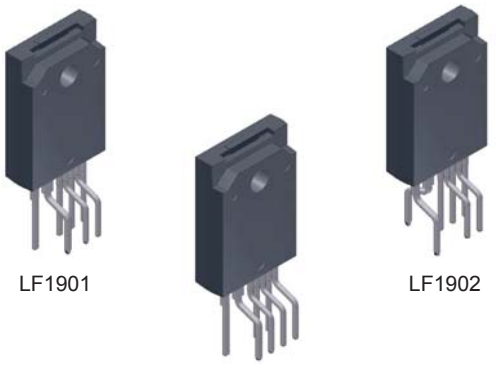


Figure 1. STR-X6700 series packages are fully molded TO-3P package types: LF1901 (STR-X6737 and STR-X6769), LF1902 (STR-X6729 and STR-X6768N), and LF1905 (STR-X6757 and STR-X6759N).

Table 1. Product Line-up

Type #	MOSFET V_{DSS} (V)	$R_{DS(on)}$ (Max) (Ω)	VAC Input (V)	P_{OUT}[a] (W)
STR-X6729[b]	450	0.189	120	460
STR-X6737	500	0.36	120	280
STR-X6757	650	0.62	Wide	165
			230	320
STR-X6759N[b]		0.385	Wide	250
			230	460
STR-X6768N[b]	800	1.00	Wide	150
			230	220
STR-X6769		0.66	Wide	210
			230	310

[a]The listed output power represents thermal ratings, and the peak output power, P_{OUT}, is obtained by 120% to 140% of the thermal rating value. In case of low output voltage and narrow on-duty cycle, the P_{OUT} (W) becomes lower than the above.
[b]Auto-standby mode not included.

All performance characteristics given are typical values for circuit or system baseline design only and are at the nominal operating voltage and an ambient temperature of 25°C, unless otherwise stated.

Pin functional descriptions

VCC Supply (pin 4)

Start-up circuit The start-up circuit detects the VCC pin voltage, and makes the control IC start and stop operation. The power supply of the control IC (VCC pin input) employs a circuit as shown in figure 2. At start-up, C3 is charged through a start-up resistor R2. The R2 value needs to be set for more than the hold current of the latch circuit (140 µA max.) and to operate at the minimum AC input.

If the value of R2 is too high, the C3 charge current will be reduced. Consequently, it will take longer to reach the Operation-Start voltage. The VCC pin voltage falls immediately after the control circuit starts its operation. The voltage drop can be reduced by increasing C3 capacitance. However, too large a C3 capacitance will cause an improperly long time to reach the Operation-Start voltage after the initial power turn on.

In general, SMPS performs its start-up operation properly with a value of C3 between 4.7 and 47 µF, and R2 between 47 and 150 kΩ for 120 V narrow or universal AC input, and 82 to 330 kΩ for 200 V narrow AC input.

As shown in figure 3, the circuit current is limited to 100 µA max (V_{CC} = 15 V, and resistor R2 with appropriate high resistance value for the circuit) until the control circuit starts its operation. Once the VCC pin voltage reaches 18.2 V, the control circuit starts its operation by the start-up circuit, and supply current is increased. Once the VCC pin voltage drops down to lower than the Operation-Stop voltage 9.7 V, the UVLO circuit operates to stop the control circuit, and the IC returns to its initial state.

Bias/drive winding After the control circuit starts its operation, the power supply is operated by rectifying and smoothing the voltage of the bias winding. Figure 4 shows the start-up voltage waveform of the VCC pin. The bias winding voltage does not immediately increase up to the set voltage after the control circuit starts its operation. That is why the VCC pin voltage starts dropping. The Operation-Stop voltage is set as low as 10.6 V (max), the bias winding voltage reaches a stabilized voltage before it drops to the Operation-Stop voltage, and the control circuit contiues its operation. The bias winding voltage, in normal power supply operation, is set for the voltage across C3 to be higher than the Operation-Stop voltage, $V_{CC(OFF)}$, 10.6 V (max.) and lower than the OVP-operation voltage, $V_{CC(OVP)}$, 25.5 V (min.).

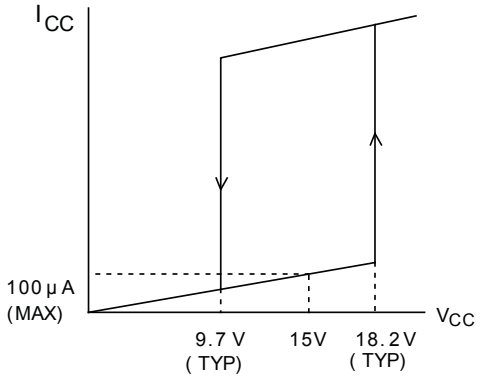


Figure 3. VCC pin current versus voltage

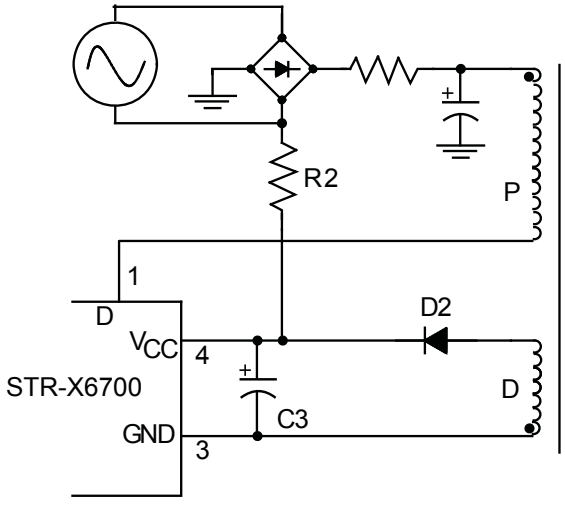


Figure 2. External start-up circuit.

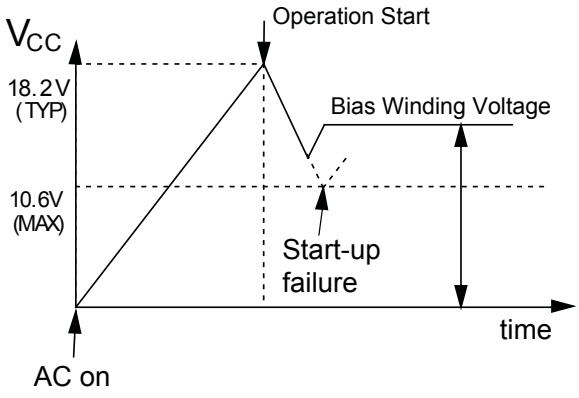


Figure 4. VCC pin voltage after start-up, capacitor C3 installed

In an actual power supply circuit, the VCC pin voltage might be changed by the value of secondary output current as shown in figure 5. C3 is fully charged by the surge voltage generated instantly after the MOSFET turns off. In order to prevent this, it is effective to add a resistor (R7) of several ohms to tens of ohms in series with the diode as shown in figure 5. The optimum value of the additional resistor is determined in accordance with the specifications of the transformer because the VCC pin voltage is determined by construction of the transformer.

Furthermore, the variation ratio of the VCC pin voltage becomes worse due to a loose coupling between primary and secondary windings of the transformer (the coupling between the bias winding and the stabilized output winding for the constant voltage control). Therefore, when designing a transformer, the winding position of the bias winding needs to be studied carefully.

Overvoltage protection (OVP) circuit If V_{CC}, referencing the GND pin, exceeds 27.7 V, the OVP circuit of the control IC starts its operation and the fault mode is latched by the latch circuit, the control IC stopping its oscillation. Generally, the VCC pin voltage is supplied from the bias winding of the transformer, and the voltage is in proportion to the output voltage; thus, the OVP circuit also operates in the case of overvoltage output of the secondary side, for example, when the voltage detection circuit is open. The secondary output voltage for the OVP operation ($V_{O(OVP)}$) is obtained from the following formula:

$$V_{O(OVP)} = \frac{V_{O(\text{normal operation})}}{V_{CC(\text{normal operation})}} \times 27.7\ \text{V} \quad (1)$$

Latch circuit OVP and OLP fault modes latch the oscillation output low, which stops the power supply circuit operation. The holding current of the latch circuit is 140 µA (max., T_A = 25°C) when the VCC pin voltage is at the Operation-Stop voltage minus 0.3 V.

In order to prevent malfunction caused by, for instance, noise, a delay time is programmed into a timer circuit, which prevents latch circuit operation until the OVP or OLP circuit keeps operating for more than a programmed time. During the latched mode, the internal regulator circuit keeps running, the circuit current is maintained at a high level, and the VCC pin voltage drops.

When the VCC pin voltage drops down to the Operation-Stop voltage (9.7 V (typ.)), the voltage starts rising again as the circuit current becomes less than 140 µA. When the VCC pin voltage reaches the Operation-Start voltage (18.2 V (typ.)), the circuit current increases, and the voltage drops again. Consequently, the VCC pin voltage is maintained between 9.7 V and 18.2 V in the latched mode. Figure 7 shows the voltage waveform in the latched mode. The latched mode is released by decreasing the VCC pin voltage to below 7.2 V, or in general, by shutting off the AC input.

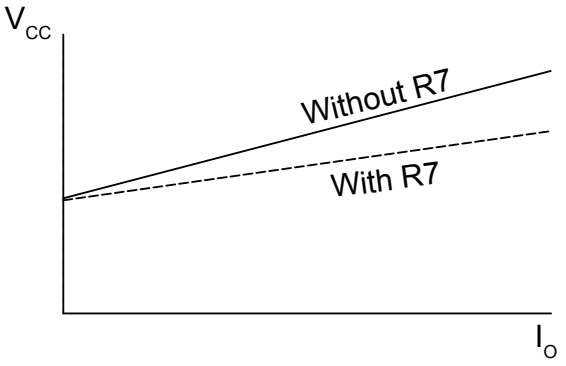


Figure 5. V_{CC} versus I_O (secondary load)

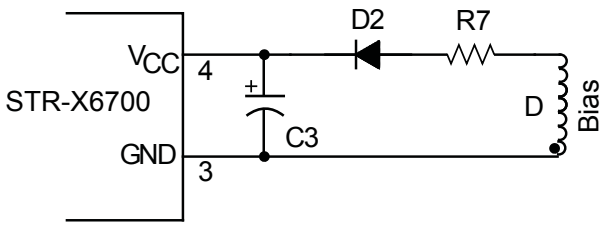


Figure 6. V_{CC} versus I_O (secondary load)

SS/OLP (Pin 5)

Through the SS/OLP pin, soft-start and overload protection is enabled by connecting a 0.47 to 3.3 µF capacitor to the pin.

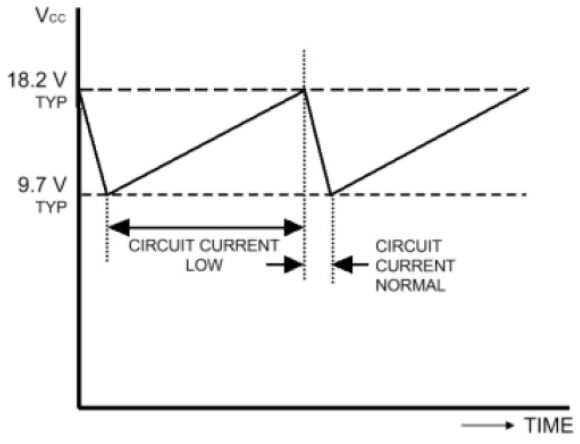


Figure 7. V_{CC} during latch mode

Soft-start operation at start-up of power supply At the power supply start-up, an external capacitor is charged up to the soft-start operation threshold voltage, $V_{SSOLP(SS)}$, by soft-start operation charging current, $I_{SSOLP(SS)}$, sourced from the SS/OLP pin. Soft-start is activated at power supply start-up by means of the SS/OLP pin voltage change from the initial 0 V level, up to 1.2 V. Timing is shown in figure 8 and the following table:

Soft-start Timing (Charging current: 550 µA)*

C_{SS} (µF)	0.47	1	2.2	3.3	4.7
Time (ms)	1.0	2.2	4.8	7.2	10.3

*A large C_{SS} value also results in a longer time from OLP operation to latched mode.

By comparing the oscillation waveforms of the SS/OLP pin and that of the internal control, soft-start widening of the on-width is activated. In addition, soft-start is operated every time in the burst oscillation of Auto-standby mode and manual standby mode.

Gradual increase of drain current suppresses audible noise from the transformer.

Overload protection (OLP) Figure 9 shows output characteristics of the secondary side when the OCP circuit is activated due to an overload at the secondary side output. When the output voltage drops in an overload mode, the bias winding voltage of the primary side drops proportionally, and the VCC pin voltage drops below the Operation-Stop voltage to deactivate the IC. Then the circuit current decreases, and the VCC pin voltage rises again by way of the start-up resistor (R2) charge current to reactivate the IC intermittently at the Operation-Start voltage. However, where the transformer has multiple output windings and coupling is not good enough, the intermittent operation might not be sensed even if the output voltage drops in an overload mode, because the primary bias winding voltage would not drop. Although the intermittent operation is not realized, protection might still be by means of the OLP activation.

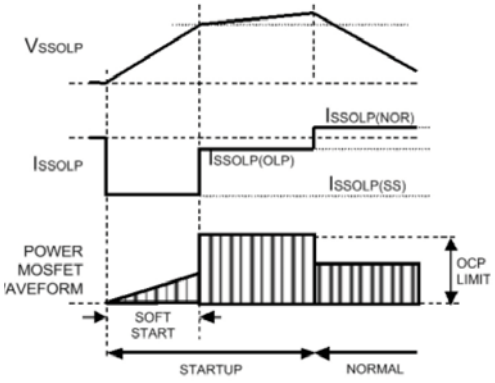


Figure 8. Soft-start operation

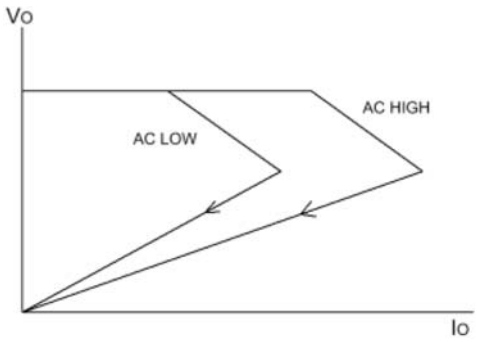


Figure 9. Current-mode control

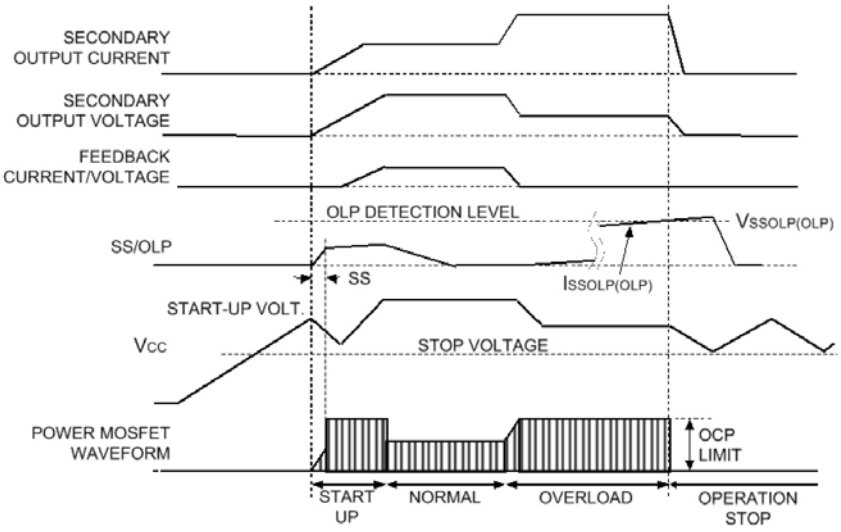


Figure 10. Timing at overload

In the overload mode, where drain current is controlled by OCP operation, the secondary-side output voltage drops. Accordingly, the error-amplifier and photocoupler on the secondary side are cut off. The STR-X6700 series regards the signal absence with continuous OCP operation as an overload status, and the SS/OLP pin voltage starts rising by $I_{SSOLP(OLP)}$ as shown in figure 10 and in the following table:

OLP timing (0 to 4.9 V, charging current: 11 µA)

C_{SS} (µF)	0.47	1.0	2.2	3.3	4.7
Time (ms)	209	445	980	1470	2094

NOTE: A large C_{SS} value also results in a longer soft-start time.

After the SS/OLP pin voltage keeps rising to the OLP-Operation Threshold Voltage ($V_{SSOLP(OLP)}$ = 4.9 V), the oscillation stops, and the IC goes into a latched mode.

The time from OLP activation to a latched mode should be obtained from the following formula, assuming $I_{SSOLP(OLP)}$ is from a constant-current circuit:

$$t = \frac{C_{SS} \times \Delta V}{I_{SSOLP(OLP)}} \quad (2)$$

where ΔV is the capacitor charging voltage of approximately 4.9 V.

However, the $I_{SSOLP(OLP)}$ is dependent on the SS/OLP pin voltage, and $I_{SSOLP(OLP)}$ drops as the SS/OLP pin voltage rises. The actual current value therefore does not exactly match the value calculated in the equation above, and the actual load conditions should be carefully considered. Also, make sure that OCP operation at power supply start-up does NOT place the IC in a latched mode. Note: During this period, if V_{CC} goes below the UVLO threshold voltage, the IC does not go into a latch mode, but goes into intermittent operation. Where the CSS voltage rises to 4.9 V and V_{CC} does not go below the UVLO threshold voltage, the IC goes into a latched mode.

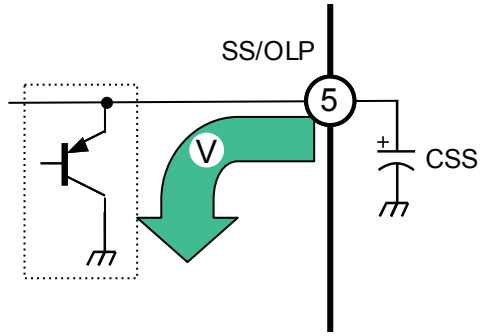


Figure 11. Reset circuit at power turn off

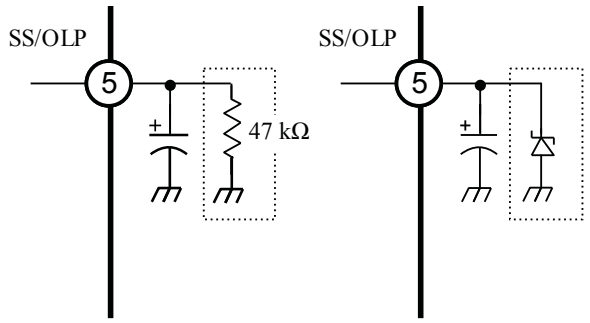


Figure 12. OLP deactivation circuit alternative configurations

Operation at power supply turn off At power supply turn off, voltage on capacitor CSS, which is externally connected to the SS/OLP pin, is discharged by way of an internal RESET circuit as shown in figure 11. The RESET circuit does not operate in normal operation while the internal regulator circuit operates.

Deactivating the OLP circuit To deactivate the OLP circuit while soft-start is active, connect either a 47 kΩ resistor or a Zener diode to the SS/OLP pin (figure 12). By doing this, OLP operation is deactivated at start-up or during an overload status.

FB (Pin 6)

The FB pin is used in either a normal mode (constant-voltage-control circuit operation) or in a standby mode. Refer to Standby Operation section for controlling in the standby mode.

Constant voltage control circuit The STR-X6700 series adopts the current-mode control circuit, which ensures stability with a heavy load. The peak value of the MOSFET drain current (at on-time) is changed by comparing the FB pin voltage with the internal V_{OCPM}. Off-time becomes quasi-resonant operation synchronized to the reset signal from a transformer. Where no reset signal is input from the transformer, it becomes fixed oscillation frequency (approximately 22 kHz) set by the internal oscillator

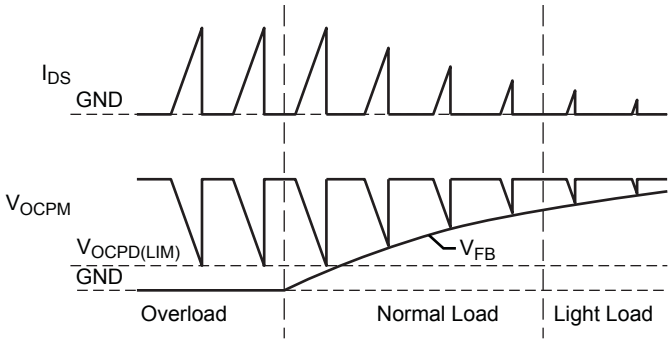


Figure 13. Constant-voltage control at fixed oscillation frequency (quasi-resonant signal not available)

circuit. The timing chart is shown in figure 13, and the internal circuit diagram of the constant voltage control circuit is shown in figure 14.

The constant-voltage-control circuit feeds a control signal (FB current) from an error amplifier into pin 6 by way of the isolating photocoupler. The input FB current is transformed into feedback voltage V_{FB} by the internal resistor (SW1 is turned on during normal status). The voltage waveform (V_{OCPM}) from the drain current waveform is input to the inverting input terminal of the FB comparator.

Figure 13 shows the FB current is decreased to nearly zero in an overload, when the drain current is restricted to below the current value set by the overcurrent protection circuit. In the period from normal load to light load in figure 13, the drain current decreases because the FB current increases and V_{FB} rises. When V_{FB} exceeds the FB pin threshold voltage ($V_{FB(OFF)}$, 1.45 V) at light load, the oscillation stops so as not to raise the secondary-side output voltage.

OCP/BD (Pin 7)

The OCP/BD pin functions in overcurrent detection, bottom-skip, and quasi-resonant-operation control. Bottom-skip and quasi-resonant features are described in the Operation Description section.

Negative-detection type OCP circuit The OCP circuit of the STR-X6700 series is a pulse-by-pulse type, which detects the peak value of the MOSFET drain current for each pulse and inverts the oscillator output. As shown in figure 15, the overcurrent sense resistor, R_{OCP}, is connected externally along with R4 and C5. R4 and C5 are to prevent malfunction caused by surges when the MOSFET switches on. When the MOSFET switches on, switching current occurs, and a voltage is developed across R_{OCP}. After that, the MOSFET turns off when the OCP/BD pin voltage reaches $V_{OCPBD(LIM)}$.

The threshold voltage of the OCP/BD pin, $V_{OCPBD(LIM)}$, is –0.94 V. The OCP circuit adopts negative-detection, which creates the detecting voltage, V_{OCPM}, in the control part by dividing the voltage ($V_1 + V_{ROCP}$) with RB1, RB2, and R4. Because RB1 and RB2 are resistors incorporated in the IC, taking the variance of RB1 and RB2 (defined as I_{OCPBD} in the specifications) into consideration, the value of R4 should be small, between 100 Ω and 330 Ω. Select capacitor C5 (100 to 680 pF target value) for good thermal behavior type. A high capacitance value results in slow response time, ending up with an increase in peak drain current during a transient and at start-up.

Operation description

Quasi-resonant operation Quasi-resonant operation matches the timing of the MOSFET turn on to the bottom point of the voltage resonant waveform, namely, ½ cycle of the resonant frequency after the transformer discharges energy.

As shown in figure 16, the voltage resonant capacitor, C4, is connected between the drain and source, and the delay circuit, C10, D3, D4, and R9 are connected between the bias winding and

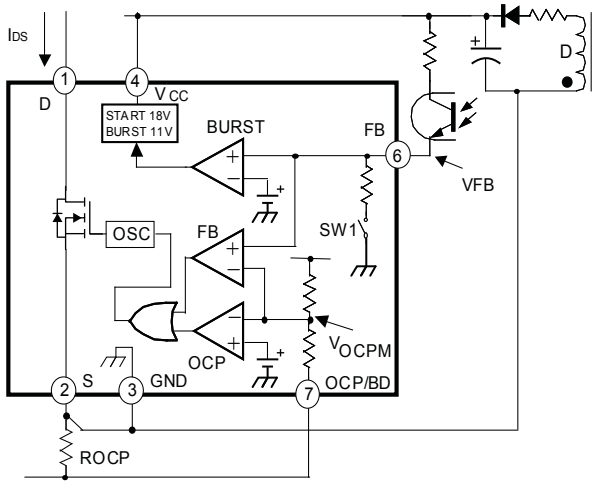


Figure 14. REG circuit functional block diagram

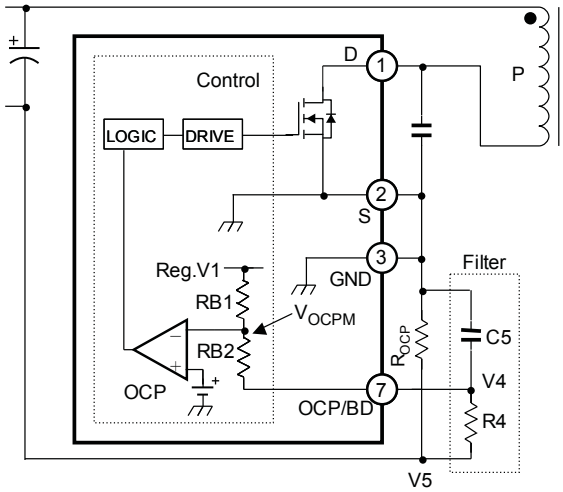


Figure 15. OCP functional block diagram

the OCP/BD pin. When the MOSFET turns off, a quasi-resonant signal is generated from the flyback voltage in the bias winding, and the BD comparator inside the IC operates, enabling quasi-resonant operation. Even after the energy of the transformer is discharged by way of the delay circuit, the quasi-resonant signal imposed on the OCP/BD pin does not drop immediately. This is because C10 is discharged by R4, and the voltage drops to the threshold voltage, $V_{OCPBD(TH1)}$, at 0.4 V after a certain period.

The delay time needs to be set by adjusting C10, monitoring the operating waveform, so that the MOSFET turns on when the V_{DS} of the MOSFET hits the lowest point.

In addition to the quasi-resonant operation, the IC incorporates a bottom-skip mode in order to suppress the increase of oscillating frequency during a light-to-medium load. It lengthens the off time in accordance with the load status. Change-over timing between the quasi-resonant and bottom-skip modes is described below.

When the quasi-resonant signal voltage imposed on the OCP/BD pin is below $V_{OCPBD(TH2)}$ at 0.8 V, the IC goes into PWM operation with a fixed oscillating frequency of 22 kHz.

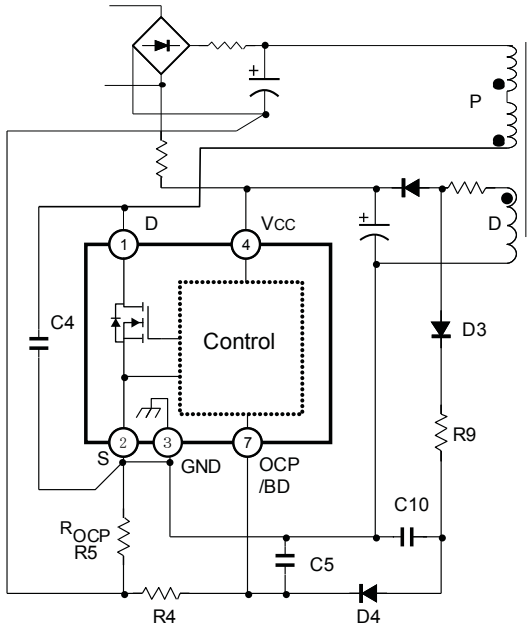


Figure 16. Quasi-resonant and delay circuit

PWM operation is also activated at power supply start-up or at low bias winding voltage due to a winding short, which lowers oscillating frequency and reduces MOSFET stress. After the quasi-resonant signal exceeds $V_{OCPBD(TH2)}$ at 0.8 V, the MOSFET remains off during $V_{OCPBD(TH1)}$ at 0.4 V and higher. A voltage difference between $V_{OCPBD(TH1)}$ and $V_{OCPBD(TH2)}$ prevents malfunction.

In setting R9 and R4, the quasi-resonant signal imposed on the OCP/BD pin needs to be 5 V or less. In a normal condition, it should be approximately 1.5 V. The value of R4 is 100 to 330 Ω and R_{OCP} is small enough to be ruled out. The bias winding output voltage is set at 18 V. To make the OCP/BD pin voltage 1.5 V or higher, R9 value is to be 1 to 3.3 kΩ. However, R9 needs to be considered together with C10 capacitance relative to setting up the delay time. R9 determines the time constant with C10 capacitance. Assuming the time constant is 2.2 µs, R4 is 220 Ω, R9 is 2.2 kΩ and C10 is 1000 pF, then proper selection should be done while looking at the quasi-resonant signal and V_{DS} waveform in the actual application.

Bottom-skip mode (shift from quasi-resonant operation) The basic bottom-skip mode is activated at light load by judging secondary load status by means of the drain current value (actually OCP/BD pin voltage). If the load status evaluates as heavy load, the IC goes into quasi-resonant operation. Judging is made by reading the OCP/BD pin voltage during the falling edge of the MOSFET gate voltage. Also, the count of falling edges (OCP/BD pin voltage is less than $V_{OCPBD(TH1)}$) of quasi-resonant signal is counted to be utilized to turn the MOSFET on in accordance with the load status described above.

- Quasi-resonant operation → bottom-skip mode
  Quasi-resonance is operated under the absolute value of V_{OCP} greater than $V_{OCPBD(BS2)}$. When the load becomes lighter and the drain current drops to make V_{OCP} less than $V_{OCPBD(BS2)}$, the operation is shifted to the bottom-skip mode, and the reference voltage is automatically changed to $V_{OCPBD(BS1)}$. Figure 17 shows shift timing from quasi-resonant operation to bottom-skip mode.
- Bottom-skip mode → quasi-resonant operation
  Bottom-skip is operated under the absolute condition of V_{OCP} less than $V_{OCPBD(BS2)}$. When the load becomes heavier and the drain current increases to make V_{OCP} greater than $V_{OCPBD(BS2)}$, operation is shifted to quasi-resonant operation mode, and the

reference voltage is automatically changed to $V_{OCPBD(BS2)}$. V_{OCP} is the OCP/BD pin voltage at the falling edge of the MOSFET gate voltage.

As described above, the reference voltages for bottom-skip mode, $V_{OCPBD(BS1)}$ and $V_{OCPBD(BS2)}$, has hysteresis to make a stable operation shift as shown in figure 18.

Standby modes The STR-X6700 series devices incorporate standby modes to reduce power consumption. Two modes are available. One is Auto-Standby mode (except the STR-X6729, STR-X6759N, and STR-X6768N) and the other is manual standby mode (external trigger).

Auto-Standby mode The Auto-Standby mode is started by internally sensing the drain current pulse. Because the minimum drain pulse width is limited to the minimum on-time pulse width of $t_{ON(MIN)}$, at light load the power supply can not lower its output power any more, and the output voltage starts increasing. When the FB pin voltage exceeds the the FB terminal threshold voltage, $V_{FB(OFF)}$, the IC stops working until V_{FB} drops and then the power supply starts working again.

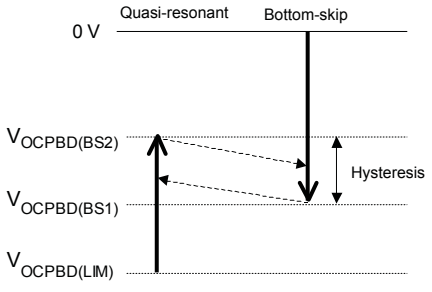


Figure 18. Operation mode shift

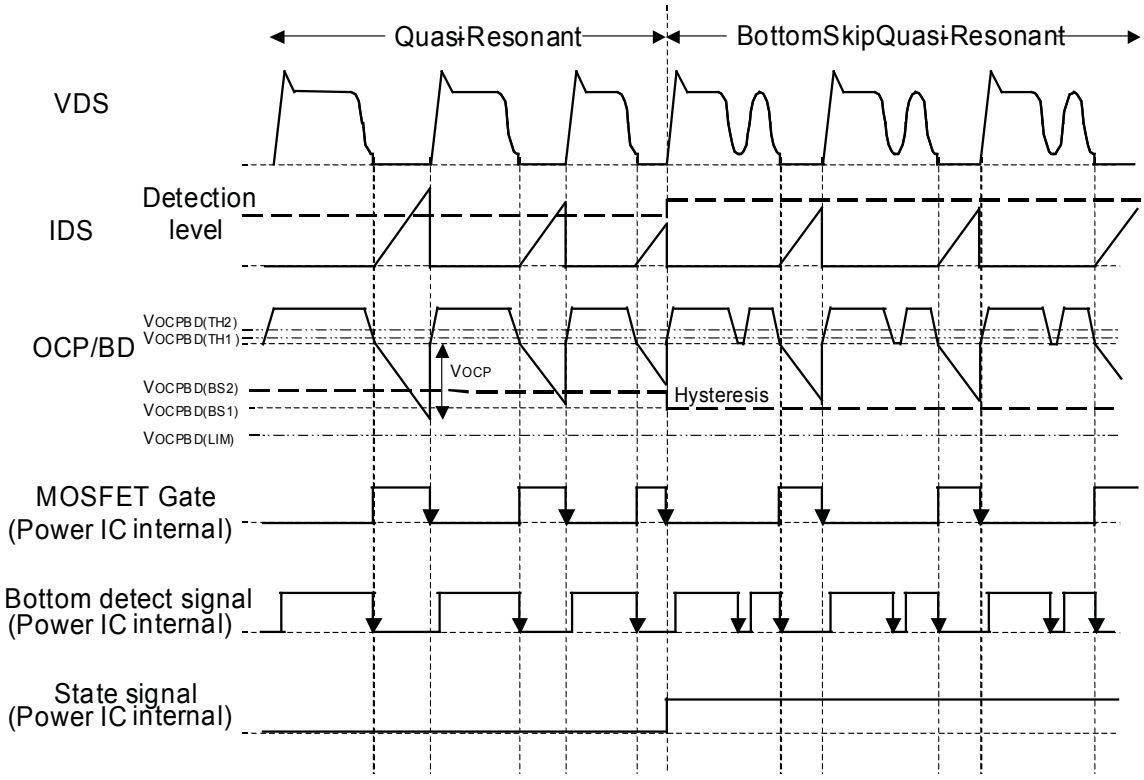


Figure 17. Quasi-resonant to bottom-skip operation timing

Manual standby mode (external trigger) The manual standby mode is remotely controlled by a clamp on the secondary side to reduce the output voltage. Then, the transformer winding voltage drops and it reduces the bias winding voltage and the VCC pin (pin 4) voltage decreases. When the VCC pin voltage reaches the Operation-Stop voltage (9.7 V), the IC stops its operation, and current consumption of the IC becomes the Standby Non-Operation Circuit Current, $I_{CC(S)}$. The IC will not restart its operation until the VCC pin voltage rises to the Standby Operation Start Voltage, $V_{CC(S)}$, by charging the start-up capacitor (C3) through the start-up resistor (R2). By repeating this cycle, the IC maintains a UVLO intermittent oscillation mode. This is illustrated in figure 19.

In order to eliminate the transformer audible noise in the UVLO intermittent oscillation mode, the voltage difference between the Standby Operation Start Voltage, $V_{CC(S)}$, and the Operation Stop Voltage, $V_{CC(OFF)}$, is designed to be small. By doing this, the operating frequency is increased without increasing the losses in the startup resistor, and the IC is in a mode where switching current is reduced to as low a level as possible.

NOTE: During transitions between the manual standby and normal operation, because the STR-X6700 series is not pumping energy, make sure that normal output load is not applied, otherwise output voltage will drop significantly and will affect the entire system operation.

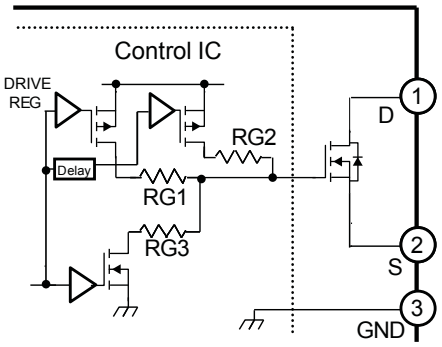


Figure 20. Step drive circuit

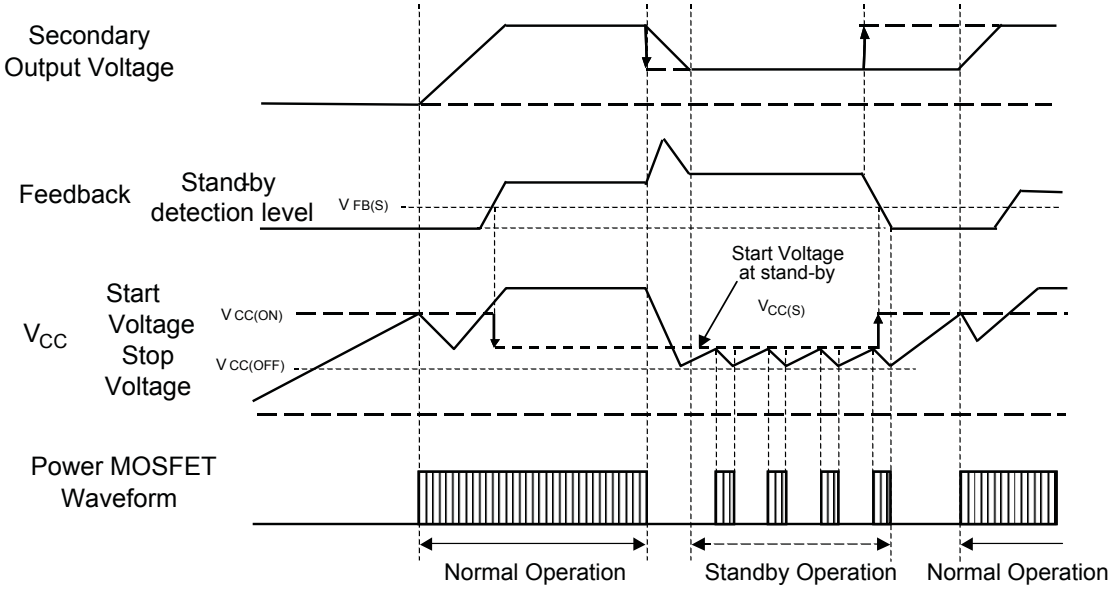


Figure 19. Quasi-resonant to bottom-skip operation timing

Gate step-drive circuit The STR-X6700 series incorporates a step-drive circuit (figure 20) for driving the MOSFET, which reduces noise when the MOSFET turns on. The drive current, when the MOSFET turns on, is at first limited only by RG1, and the gate voltage is increased gradually, and then rapidly in approximately 0.9 µs via (RG1 / RG2). Drive voltage then uses the constant-voltage drive circuit, maintained at V_{DRM} = 7.5 V, which is not affected by V_{CC}. The MOSFET gate charge is rapidly discharged through RG3 when the MOSFET turns off.

Maximum on-time control function The MOSFET on-time is limited during transients such as at low input voltage and at turn on and turn off of AC input. This is illustrated in figure 21. The maximum on-time is set at about 70% (approximately 32 µs) of the oscillation cycle ($1/f_{osc}$ = 45 µs). In designing a power supply, the MOSFET on-time at maximum load and at minimum input voltage should be considered.

Transformer parameters

Basically, the same type of transformer is recommended as that for a conventional quasi-resonant circuit. Examples are shown in figure 22. The primary inductance, Lp, is determined by the following:

$$L_P = \frac{(V_{IN} \times D)^2}{([2 \times P_O \times f_{OSC} / \eta]^{1/2} + V_{IN} \times \pi \times f_{OSC} \times D \times C_4^{1/2})^2} \quad (3)$$

where:

P_O = maximum output power,
f_{OSC} = minimum oscillating frequency,
D = On duty cycle at minimum V_{IN}(AC)
= $E_f/(V_{IN} + E_f)$, given E_f = flyback voltage,
η = transformer conversion efficiency (0.9 in the case of CRT TV, and 0.75 to 0.85 in the case of low output voltage), and
V_{IN} = rectified and smoothed DC input voltage at minimum V_{IN}(AC).

Turn-on delay results in duty cycle change in a quasi-resonant operation, therefore, duty cycle correction is necessary. From the following formulas, the number of turns, the peak switching current (I_{DP}), corrected duty cycle (D_{err}), delay time (t_d), and others can be obtained:

$$t_d = \pi \times (L_P \times C_4)^{1/2} \quad (4)$$

$$D_{err} = D \times (1 - [f_{OSC} \times t_d]) \quad (5)$$

$$I_{IN} = P_O / (\eta 2 \times V_{IN}) \quad (6)$$

$$I_{dp} = 2 \times I_{IN} / D_{err} \quad (7)$$

$$N_P = (L_P / AL)^{1/2} \quad (8)$$

$$N_S = N_P (V_O + V_f) / E_f \quad (9)$$

where:

I_{IN} = average DC input current,
I_{dp} = peak switching current,
C_4 = voltage resonance capacitance,
η2 = power supply efficiency (0.85-0.9 in case of CRT TV),
L_P = primary inductance
N_P = primary turns
N_S = secondary turns, and
V_f = forward voltage of the secondary rectifier.

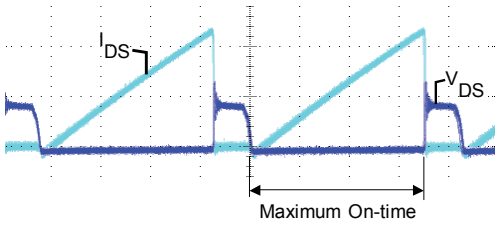


Figure 21. Maximum on-time

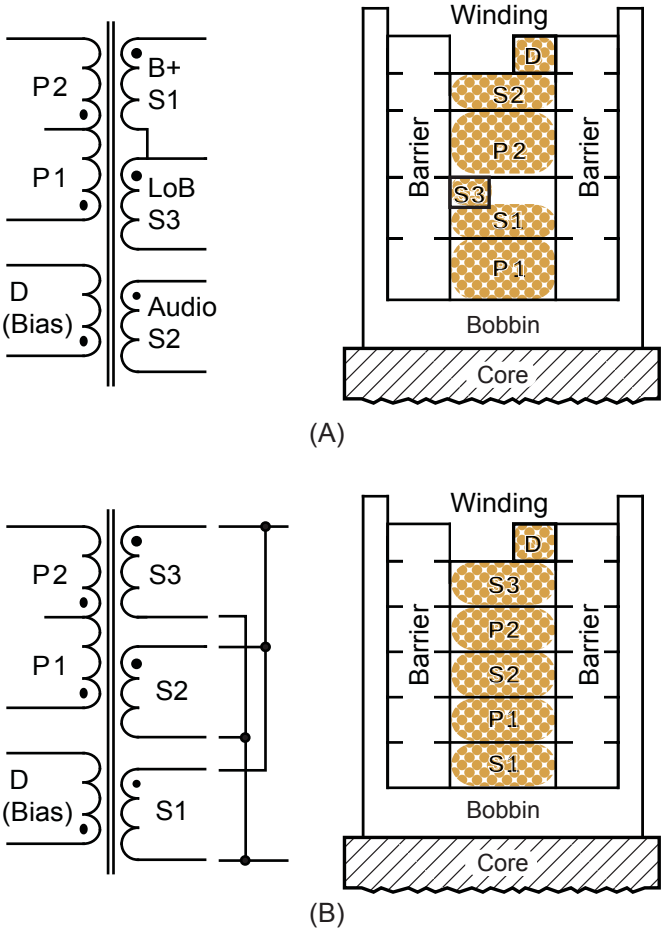


Figure 22. Example of recommended transformers: (A) CRT TV transformer, (B) low output-voltage transformer.

In addition, in the design of the transformer, using 130% of the estimated peak switching current is recommended to ensure that the transformer is not saturated, based on the plot of N × I-limit (AT) versus AL-value (nH / N^2).

Instead of performing the calculations above, software that provides a complete flyback transformer design tool is available.

CRT TV application concerns:

- Rather than winding with a single thick wire, a thin and bifilar or trifilar winding across the entire width of bobbin is recommended.
- For windings where N_P and +B are a large number of turns, divisional sandwich winding is recommended.
- For an output where a tight regulation is required, winding with good coupling with S1 (+B) is recommended.
- For the +B winding, better coupling by use of litz wire is required. In case the litz wire does not fit into a the bobbin winding width, reduce the wire size, and use 2 to 3 of them in strands.
- For improved thermal design:
  - Leakage flux of wires close to the core center becomes large. Eddy current can be reduced by the use of litz wire.
  - In case the entire winding does not fit into the available winding thickness, reduce the size of wires from outer side.
  - Wire diameter is determined based on actual current and should be less than 4 A / mm^2.

Single and/or low-voltage output concerns:

- Wind so that wires are parallel and with good coupling.
- Sandwich winding is recommended.

General considerations

Universal AC input correction in OCP

With a universal AC input application, as described in the Overload Protection (OLP) section, the load conditions for OCP activation vary according to input voltage level, 110 V or 230 V. Figure 23 illustrates a solution.

In the loop surrounded by the dashed line, the negative voltage of the bias winding, which is in proportion to the input voltage level when the MOSFET switches on, works for the input correction during OLP.

The Zener diode is set to be on with a 230 VAC input, but not to be activated with a 110 VAC input. When the bias winding output voltage is 18 V, the resistor, Zener, and diode within the dashed line are recommended.

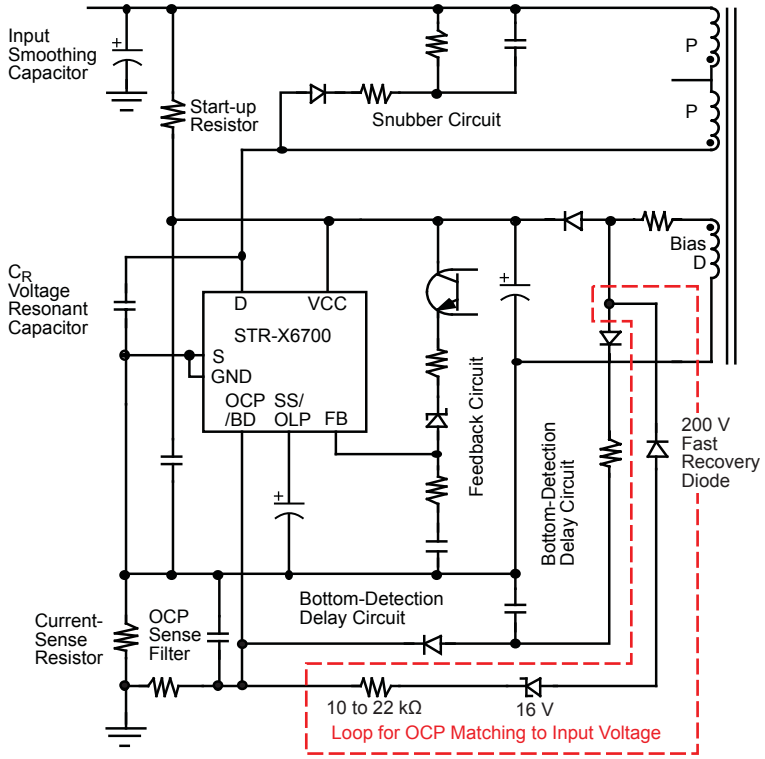


Figure 23. Reference circuit for general application considerations

OCP on the FB pin

As shown in the feedback circuit portion of figure 23, a Zener diode is connected in series with the photocoupler. This is a countermeasure against an FB-pin voltage rise over 9 V in the manual standby mode. The absolute maximum FB-pin voltage is 9 V, and a Zener diode voltage of 5.6 to 6.2 V is recommended.

Output regulation and transformer noise during standby and automatic modes

Figure 24 presents a simplified circuit of the secondary output and manual standby circuit by V_O drop.

After the output voltage is shifted over to a lower level, the IC goes into a manual standby mode on the primary side. In this mode, sufficient power is not obtained, resulting in audible noises from the transformer, and deep ripple output voltage is generated, a sharp drop of output voltage, and unsustainable regulation, although a larger output smoothing capacitor reduces this issue.

Load in an actual manual standby mode ranges between tens of milliwatts and 0.2 W.

In regard to the audible noise from the transformer, contact a transformer manufacturer as a precaution against possible varnish dissolving and ferrite core attaching.

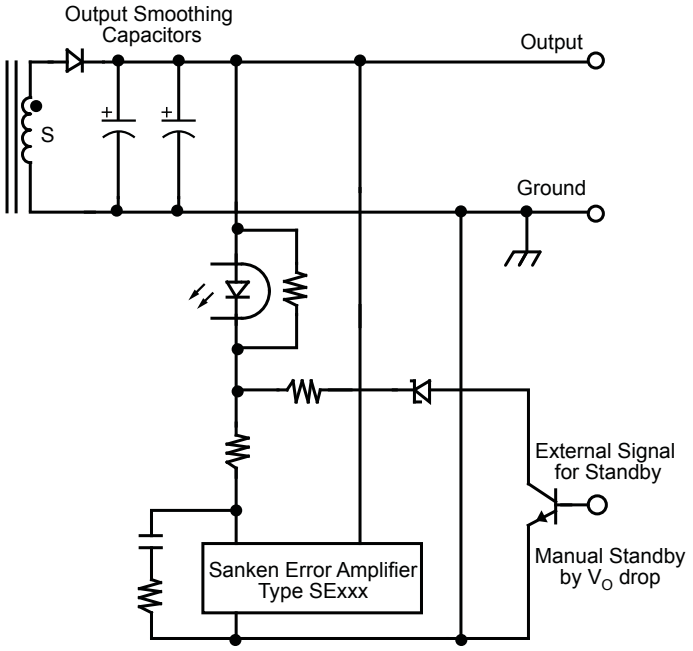


Figure 24. Output circuit

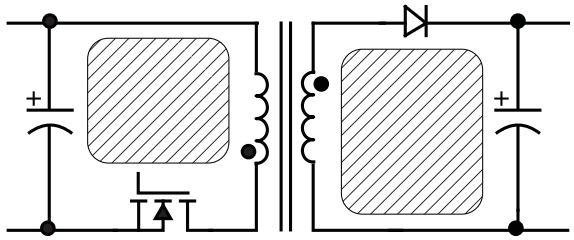


Figure 25. High frequency, high current loops

Design considerations

Component placement considerations in SMPS circuits

As pattern layout and component position may cause malfunctions of the IC, EMI noises, or power losses, the following guidelines should be followed:

- Traces where high frequencies and high current levels flow should be kept thick and short to lower line impedance.
- The hatched area illustrated in figure 25, where high frequencies and high currents create a loop, should be kept as small as possible.
- GND and earth ground lines should be kept as thick and short as possible.
- In off-line SMPS (switch-mode power supply) circuitry, because traces and paths of high voltage exist, component layout and trace length should be carefully considered, as required by safety standards.
- Take into account the positive thermal coefficiency of the MOSFET $R_{DS(on)}$ when preparing the thermal design.

Layout considerations

In order to reduce or eliminate common impedance lines, the GND pin (pin 3) and its peripheral components should be located as close together as possible, as illustrated in figure 26. The trace from the overcurrent sense resistor to the input smoothing capacitor should be kept as short and thick as possible.

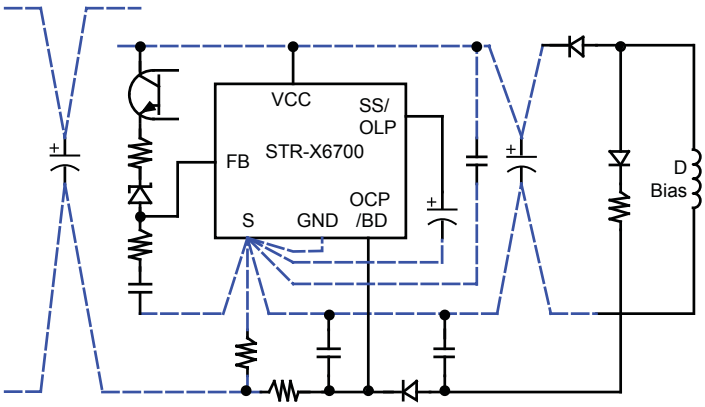


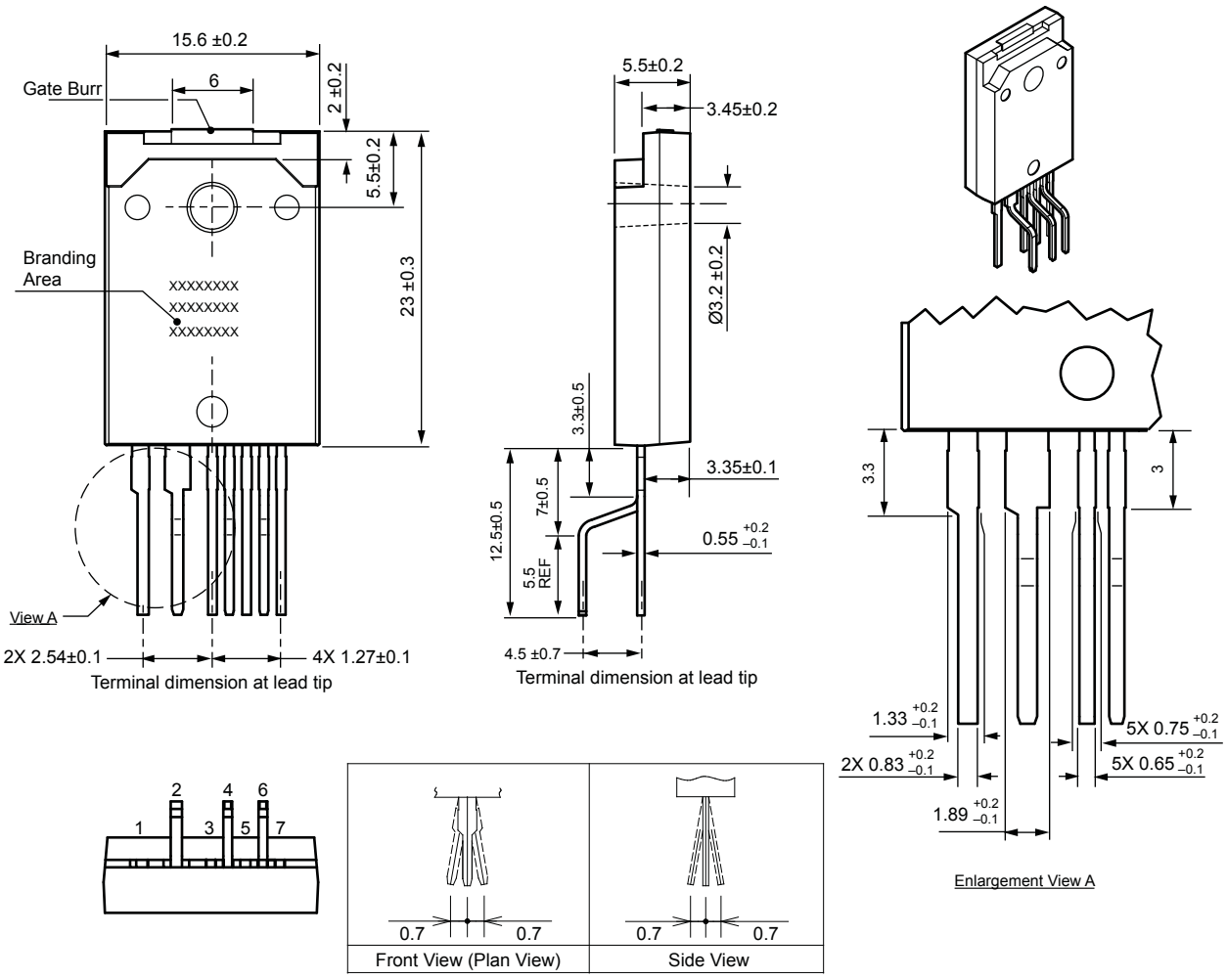
Figure 26. High frequency, high current loops

Terminal List Table

Number	Name	Description	Functions
1	D	Drain	MOSFET drain
2	S	Source	MOSFET source
3	GND	Ground terminal	Ground
4	VCC	Power supply terminal	Input of power supply for control circuit
5	SS/OLP	Soft Start/Overload Protection terminal	Input to set delay for Overload Protection and Soft Start operation
6	FB	Feedback terminal	Input for Constant Voltage Control and Burst (intermittent) Mode oscillation control signals
7	OCP/BD	Overcurrent Protection/Bottom Detection	Input for Overcurrent Detection and Bottom Detection signals

Package dimensions, TO-3P

Leadform 1901 (STR-X6737 and STR-X6769)



Gate burr: 0.3 mm (max.)
Terminal core material: Cu
Terminal treatment: Ni plating and Pb-free solder dip
Leadform: 1901

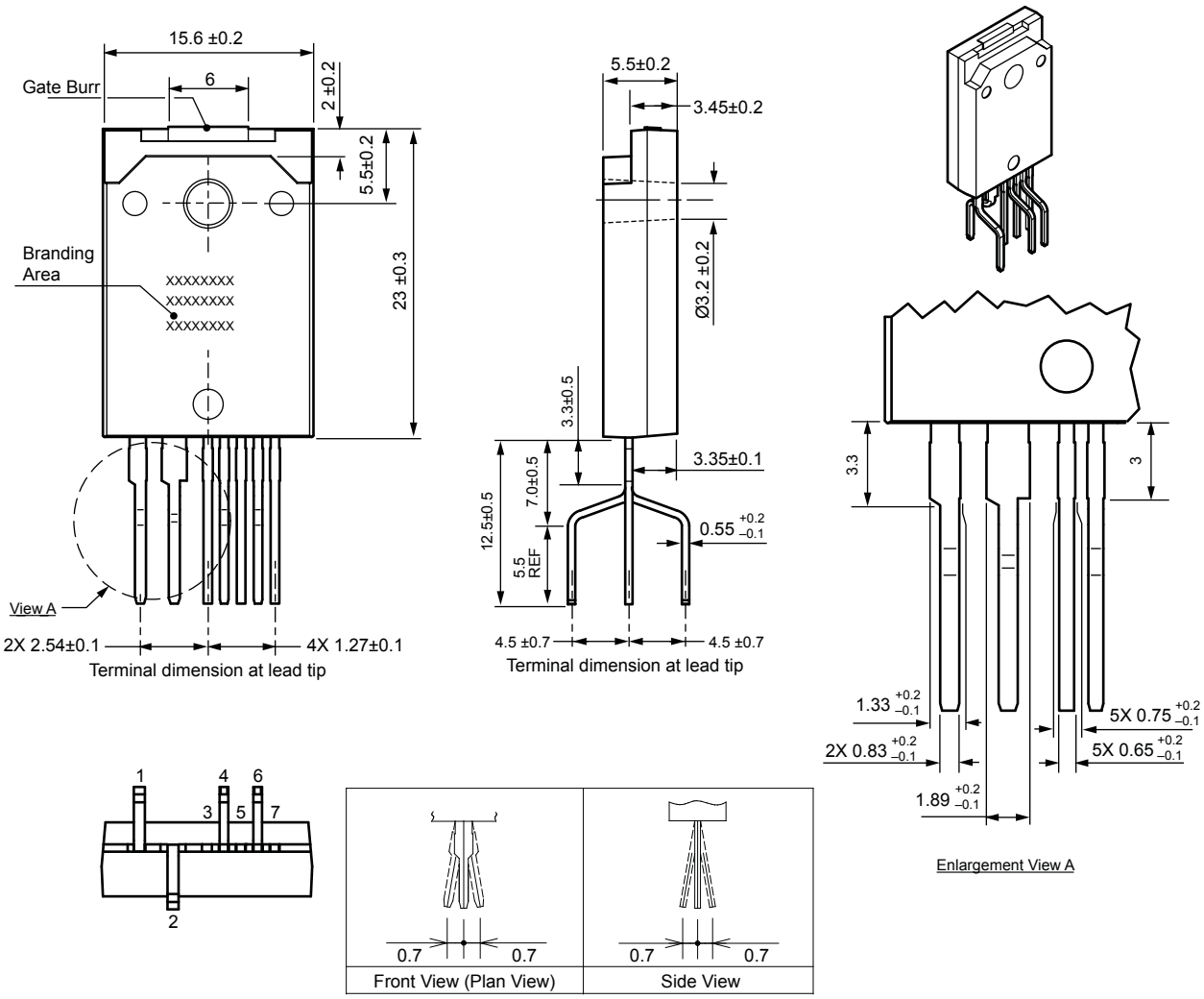
Approximate weight: 6 g

Dimensions in millimeters

Drawing for reference only
Branding codes (exact appearance at manufacturer discretion):
1st line, type: STR
2nd line, subtype: X6737 or X6769
3rd line, lot: *YM DD*
Where: Y is the last digit of the year of manufacture
M is the month (*1* to *9*, *O*, *N*, *D*)
DD is the 2-digit date

Leadframe plating Pb-free. Device composition includes high-temperature solder (Pb >85%), which is exempted from the RoHS directive.

Leadform 1902 (STR-X6729 and STR-X6768N)



Gate burr: 0.3 mm (max.)
Terminal core material: Cu
Terminal treatment: Ni plating and Pb-free solder dip
Leadform: 1902

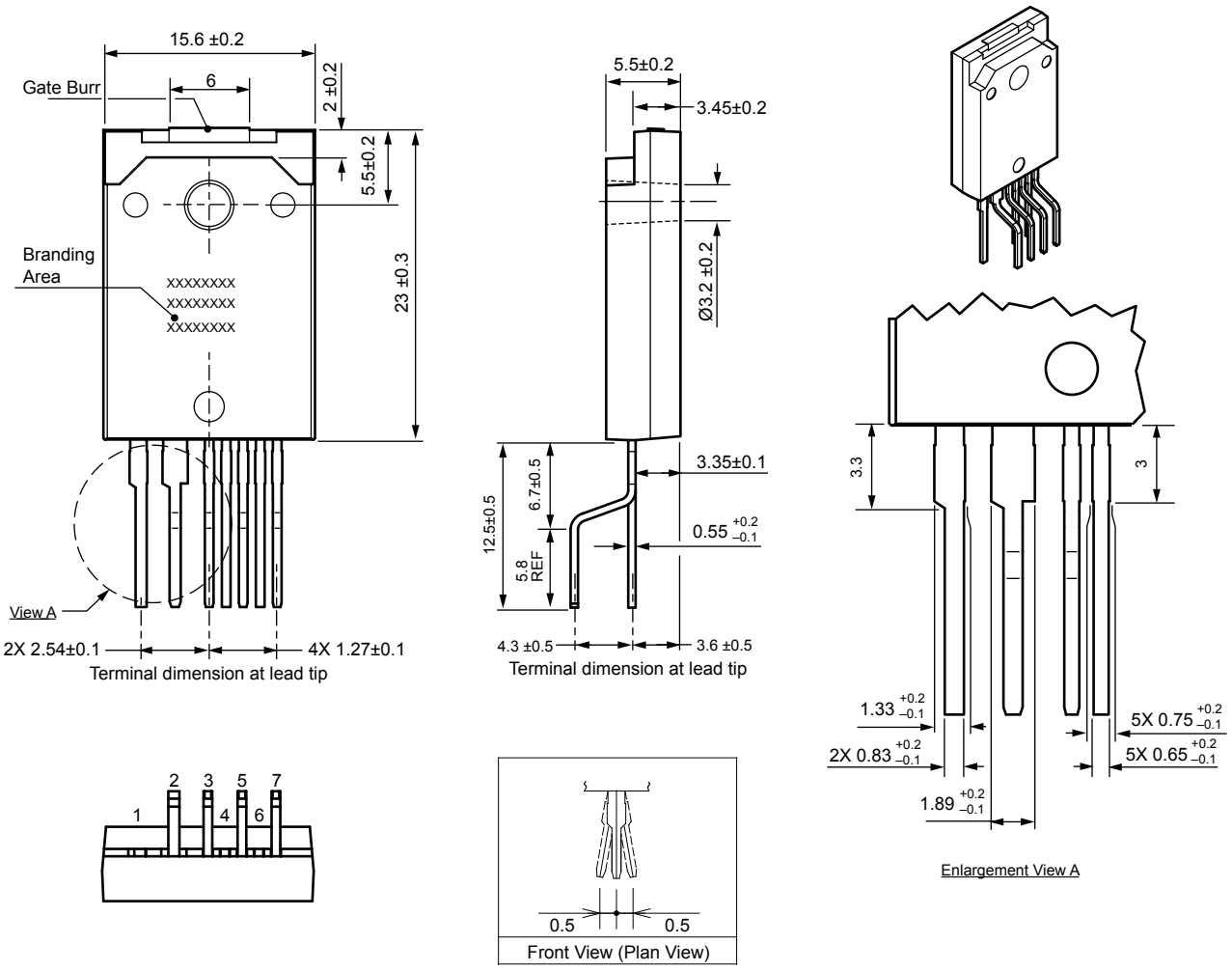
Approximate weight: 6 g

Dimensions in millimeters

Drawing for reference only
Branding codes (exact appearance at manufacturer discretion):
1st line, type: STR
2nd line, subtype: X6729 or X6768
3rd line, lot: *YM DD*
Where: Y is the last digit of the year of manufacture
M is the month (*1* to *9*, *O*, *N*, *D*)
DD is the 2-digit date

Leadframe plating Pb-free. Device composition includes high-temperature solder (Pb >85%), which is exempted from the RoHS directive.

Leadform 1905 (STR-X6757 and STR-X6759N)



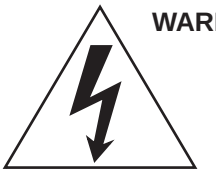
Gate burr: 0.3 mm (max.)
Terminal core material: Cu
Terminal treatment: Ni plating and Pb-free solder dip
Leadform: 1905

Approximate weight: 6 g

Dimensions in millimeters

Drawing for reference only
Branding codes (exact appearance at manufacturer discretion):
1st line, type: STR
2nd line, subtype: X6757 or X6759
3rd line, lot: *YM DD*
Where: Y is the last digit of the year of manufacture
M is the month (*1* to *9*, *O*, *N*, *D*)
DD is the 2-digit date

Leadframe plating Pb-free. Device composition includes high-temperature solder (Pb >85%), which is exempted from the RoHS directive.



WARNING — These devices are designed to be operated at lethal voltages and energy levels. Circuit designs that embody these components must conform with applicable safety requirements. Precautions must be taken to prevent accidental contact with power-line potentials.

The use of an isolation transformer is recommended during circuit development and breadboarding.

Because reliability can be affected adversely by improper storage environments and handling methods, please observe the following cautions.

Cautions for Storage

- Ensure that storage conditions comply with the standard temperature (5°C to 35°C) and the standard relative humidity (around 40 to 75%); avoid storage locations that experience extreme changes in temperature or humidity.
- Avoid locations where dust or harmful gases are present and avoid direct sunlight.
- Reinspect for rust on leads and solderability of products that have been stored for a long time.

Cautions for Testing and Handling

When tests are carried out during inspection testing and other standard test periods, protect the products from power surges from the testing device, shorts between adjacent products, and shorts to the heatsink.

Remarks About Using Silicone Grease with a Heatsink

- When silicone grease is used in mounting this product on a heatsink, it shall be applied evenly and thinly. If more silicone grease than required is applied, it may produce stress.
- Coat the back surface of the product and both surfaces of the insulating plate to improve heat transfer between the product and the heatsink.
- Volatile-type silicone greases may permeate the product and produce cracks after long periods of time, resulting in reduced heat radiation effect, and possibly shortening the lifetime of the product.
- Our recommended silicone greases for heat radiation purposes, which will not cause any adverse effect on the product life, are indicated below:

Type	Suppliers
G746	Shin-Etsu Chemical Co., Ltd.
YG6260	Momentive Performance Materials
SC102	Dow Corning Toray Silicone Co., Ltd.

Heatsink Mounting Method

- Torque When Tightening Mounting Screws. Thermal resistance increases when tightening torque is low, and radiation effects are decreased. When the torque is too high, the screw can strip, the heatsink can be deformed, and distortion can arise in the product frame. To avoid these problems, observe the recommended tightening torques for this product package type, TO-3P: 0.588 to 0.785 N•m (6 to 8 kgf•cm).
- For effective heat transfer, the contact area between the product and the heatsink should be free from burrs and metal fragments, and the heatsink should be flat and large enough to contact over the entire side of the product, including mounting flange and exposed thermal pad, and have a minimal mounting hole to prevent possible deflection and cracking of the product case when fastened to the heatsink.

Soldering

- When soldering the products, please be sure to minimize the working time, within the following limits:

  260±5°C 10 s

  350±5°C 3 s
- Soldering iron should be at a distance of at least 1.5 mm from the body of the products

Electrostatic Discharge

- When handling the products, operator must be grounded. Grounded wrist straps worn should have at least 1 MΩ of resistance to ground to prevent shock hazard.
- Workbenches where the products are handled should be grounded and be provided with conductive table and floor mats.
- When using measuring equipment such as a curve tracer, the equipment should be grounded.
- When soldering the products, the head of soldering irons or the solder bath must be grounded in other to prevent leak voltages generated by them from being applied to the products.
- The products should always be stored and transported in our shipping containers or conductive containers, or be wrapped in aluminum foil.

The products described herein are manufactured in Japan by Sanken Electric Co., Ltd. for sale by Allegro MicroSystems, Inc.

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