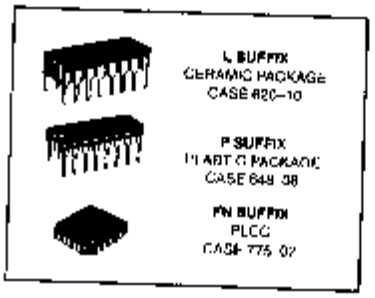
Triple Line Receiver

MC10116



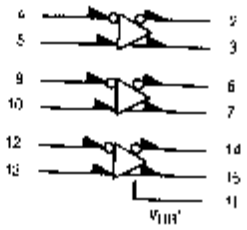
The MC10116 is a triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10116 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

P_D = 85 mW typ/pkg (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM

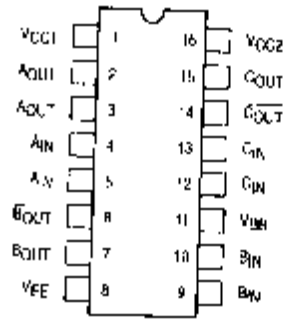


V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

*V_{BB} is to be used to supply bias to the MC10116 only and bypassed (when used) with 0.01 µF to 0.1 µF capacitor to ground. V_{BB} can source = 1.0 mA.

▲When the input pin with the bubble goes positive, the output pin with the bubble goes positive.

DIP
PIN ASSIGNMENT



Pin assignment is for Dual-In-Line Package.
For PLCC pin assignment, see the Pin Conversion tables on page 8-11.

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ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Pin Under Test	Test Limits							Unit
				−30°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current		I_E	8		23		17	21		23	mAdc
Input Current		I_{inH}	4		150			95		95	µAdc
		I_{CBO}	4		1.5			1.0		1.0	µAdc
Output Voltage	Logic 1	V_{OH}	2 3	−1.080 1.060	−0.890 0.890	−0.960 −0.960		−0.810 −0.810	−0.890 −0.890	−0.700 −0.700	Vdc
Output Voltage	Logic 0	V_{OL}	2 3	−1.890 −1.890	−1.675 1.675	−1.850 −1.850		−1.650 −1.650	−1.825 −1.825	−1.615 −1.615	Vdc
Threshold Voltage	Logic 1	V_{OHA}	2 3	−1.080 −1.080		−0.980 −0.980			−0.910 −0.910		Vdc
Threshold Voltage	Logic 0	V_{OLA}	2 3		−1.655 −1.655			−1.630 −1.630		1.595 1.595	Vdc
Reference Voltage		V_{BB}	11	−1.420	−1.280	−1.360		−1.230	−1.295	−1.150	Vdc
Switching Times (50Ω Load)											ns
Propagation Delay		t_{4-2+}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	
		t_{4-2-}	2	1.0	3.1	1.0	2.0	2.9	1.0	3.3	
		t_{4-3+}	3	1.0	3.1	1.0	2.0	2.9	1.0	3.3	
		t_{4-3-}	3	1.0	3.1	1.0	2.0	2.9	1.0	3.3	
Rise Time	(20 to 80%)	t_{2+}	2	1.1	3.6	1.1	2.0	3.3	1.1	3.7	
		t_{3-}	3	1.1	3.6	1.1	2.0	3.3	1.1	3.7	
Fall Time	(20 to 80%)	t_{2-}	2	1.1	3.6	1.1	2.0	3.3	1.1	3.7	
		t_{3+}	3	1.1	3.6	1.1	2.0	3.3	1.1	3.7	

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ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{BB}	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	From Pin 11	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475		−5.2
+85°C	−0.720	−1.825	−1.035	−1.440		−5.2

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						(V_{CC}) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{BB}	V_{EE}	
Power Supply Drain Current		I_E	8		4, 9, 12			5, 10, 13	8	1, 16
Input Current		I_{inH}	4	4	9, 12			5, 10, 13	8	1, 16
		I_{CBO}	4		9, 12			5, 10, 13	8,4	1, 16
Output Voltage	Logic 1	V_{OH}	2	4	9, 12			5, 10, 13	8	1, 16
			3	9, 12	4			5, 10, 13	8	1, 16
Output Voltage	Logic 0	V_{OL}	2	9, 12	4			5, 10, 13	8	1, 16
			3	4	9, 12			5, 10, 13	8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	2		9, 12	4		5, 10, 13	8	1, 16
			3	9, 12			4	5, 10, 13	8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	2		9, 12		4	5, 10, 13	8	1, 16
			3	9, 12		4		5, 10, 13	8	1, 16
Reference Voltage		V_{BB}	11					5, 10, 13	8	1, 16
Switching Times	(50Ω Load)					Pulse In	Pulse Out		−3.2 V	+2.0 V
Propagation Delay		t_{4+2-}	2			4	2	5, 10, 13	8	1, 16
		t_{4-2+}	2			4	2	5, 10, 13	8	1, 16
		t_{4+3-}	3			4	3	5, 10, 13	8	1, 16
		t_{4-3+}	3			4	3	5, 10, 13	8	1, 16
Rise Time	(20 to 80%)	t_{2+}	2			4	2	5, 10, 13	8	1, 16
		t_{3+}	3			4	3	5, 10, 13	8	1, 16
Fall Time	(20 to 80%)	t_{2-}	2			4	2	5, 10, 13	8	1, 16
		t_{3-}	3			4	3	5, 10, 13	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear lpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

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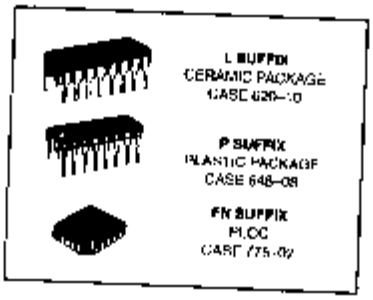
Dual 4-5-Input OR/NOR Gate

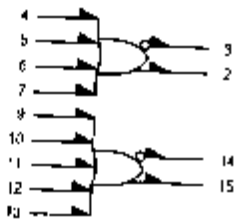
MC10109

The MC10109 is a dual 4-5 input OR/NOR gate

P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

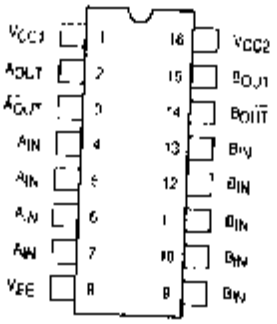


LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8

DIP
PIN ASSIGNMENT



Pin Assignment is for Dual-In-Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 8-11.

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		15		11	14		15	mAdc
Input Current	I_{inH}	4		425			265		265	µAdc
	I_{inL}	4	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	2 3	−1.060 −1.060	−0.860 −0.860	−0.980 −0.980		−0.810 −0.810	−0.890 −0.890	−0.700 −0.700	Vdc
Output Voltage Logic 0	V_{OL}	2 3	−1.890 −1.890	−1.675 −1.675	−1.850 −1.850		−1.650 −1.650	−1.825 −1.825	−1.615 −1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2 3	−1.080 −1.080		−0.980 −0.980			−0.910 −0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2 3		−1.655 −1.655			−1.630 −1.630		−1.595 −1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{4+2+}	2	1.0	3.7	1.0	2.0	2.9	1.0	3.7	
	t_{4-2-}	2	1.0	3.7	1.0	2.0	2.9	1.0	3.7	
	t_{4+3-}	3	1.0	3.7	1.0	2.0	2.9	1.0	3.7	
	t_{4-3+}	3	1.0	3.7	1.0	2.0	2.9	1.0	3.7	
Rise Time (20 to 80%)	t_{2+}	2	1.1	4.0	1.1	2.0	3.3	1.1	4.0	
	t_{3+}	3	1.1	4.0	1.1	2.0	3.3	1.1	4.0	
Fall Time (20 to 80%)	t_{2-}	2	1.1	4.0	1.1	2.0	3.3	1.1	4.0	
	t_{3-}	3	1.1	4.0	1.1	2.0	3.3	1.1	4.0	

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ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature	TEST VOLTAGE VALUES (Volts)				
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
−30°C	0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	1.850	1.105	1.475	5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic		Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(VCC) Gnd
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8						
Input Current		I_{inH}	4	4				8	1, 16
		I_{inL}	4		4			8	1, 16
Output Voltage	Logic 1	V_{OH}	2	4				8	1, 16
			3					8	1, 16
Output Voltage	Logic 0	V_{OL}	2					8	1, 16
			3	4				8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	2			4		8	1, 16
			3				4	8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	2					8	1, 16
			3			4	4	8	1, 16
Switching Times	(50Ω Load)					Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay		t_{4+2+}	2			4	2	8	1, 16
		t_{4-2-}	2			4	2	8	1, 16
		t_{4+3-}	3			4	3	8	1, 16
		t_{4-3+}	3			4	3	8	1, 16
Rise Time	(20 to 80%)	t_{21}	2			4	2	8	1, 16
		t_{3-}	3			4	3	8	1, 16
Fall Time	(20 to 80%)	t_{2}	2			4	2	8	1, 16
		t_{3-}	3			4	3	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

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