14 POWER MANAGEMENT

14.1 Power supply inputs

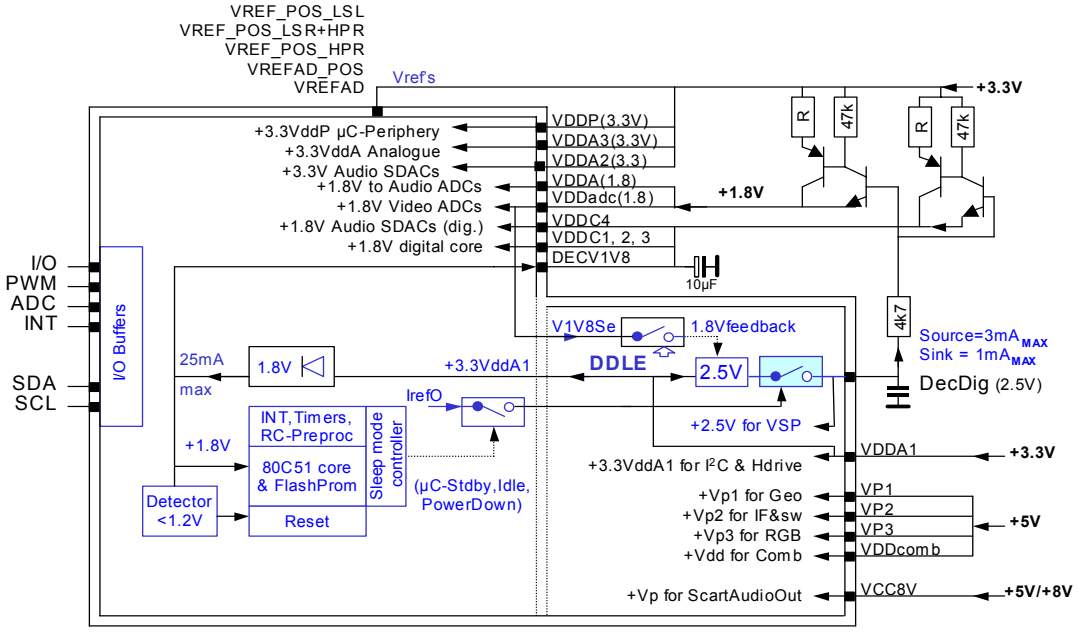

Figure 149. Supply structure

The UOCIII needs several supply voltages for several functions. The Video-Signal-Processor (VSP) needs +3.3V and +5V. The Scart audio output needs +8V in case of $2V_{RMS}$ output else it needs +5V for $1.2V_{RMS}$ output.
The digital part needs +1.8V which can be generated by the UOCIII itself using some external transistors. During SLEEP modes the +1.8V is generated inside the IC.

The +3.3V is used for I2C, H-drive and to generate 2.5V at the **DecDig** pin. With simple transistors the 1.8V supply for the digital part can be made. In case bit **DDLE**=1 this voltage is monitored internally via pin **VDDadc(1.8)** to adjust the 2.5V DecDig keeping the 1.8V within limits. If bit **DDLE**=0 the 2.5V DecDig becomes independent of the 1.8V feedback signal. This can be used control an external 1.8V supply is applied instead of the self controlled loop.

When the digital core is switched to a SLEEP mode (µC-STDBY, IDLE or POWERDOWN), the 2.5V DecDig switches off. As the external generated 1.8V drops below 80%, an internal 1.8V supply (pin **DECV1V8**, derived from 3.3V) takes over and many circuits are disconnected. Pins **VDDA(1.8)** and **VDDadc(1.8)** must be switched-off; all other 1.8V inputs are allowed to stay on: powered via pin **DECV1V8.** The external 1.8V supply should become high impedance and may NOT pull current OUT of pin **DECV1V8**.

The 1.8V for the 80C51 core is monitored by a reset circuit. When this decoupled voltage is less than 1.2V, a reset is generated.
Whenever pin **DecDig** drops below 2.0V, a **POR** is generated for the VSP and all I2C-bus registers of the VSP must be re-written (including **DDLE**). Below 2.0V bit **DDLE** is ignored, to

guarantee a proper start-up of **DecDig**. At first-power-up the **DecDig** always goes high, to assure proper start-up of the IC.

The pins **DECV1V8**, **VDDC1**, **VDDC2** and **VDDC3** should be connected to the same power rail (1.8V). Decoupling with a series coil of 10 uH and capacitor of 100 nF is needed.
The pins **VDDA2(3.3)**, **VDDA3(3.3V)** and **VDDP(3.3V)** should be connected to the same power rail (3.3V). Decoupling with a series coil of 10 uH and small capacitor F is needed.

The 1.8V supply level is monitored. In case of a voltage higher than 2.1V the **SUPR** bit is set.
The **SUP** bit reports presence of 4.1V at pins **VP1**, **VP2**, **VP3**, **VVDCOMB** and **VCC8V**. The software may check on these bits.

14.2 Power modes

The UOCIII several power modes.

When setting bit **STB=**0 the H+V deflection is switched off (e.g. VCR-mode or LCD-TV), all other functions in the VSP can be kept active, simply by maintaining +5V.
If any of the +5V supply inputs fail (or too low) a supply-guard detector will immediately stop the related functions in the VSP.

When setting the bit **ROMBK.STDBY=**1 the 8051 core remains fully functional, but the VSP is put to sleep. When setting the bit **PCON.IDLE** =1 internal ROM and RAM is switched off. It can wake up applying any interrupt from timer, RCP, Ext, UART, I2C, WatchDog.

Another power mode called µC-**POWERDOWN** can be used instead of **IDLE**, but waking-up is then more difficult. In **POWERDOWN** mode only an external INTerrupt (or via the static SADAC) can wake-up towards **STDBY** mode.

14.3 Power & protection related bits

The **SUP** bit monitors presence 4.1V at pins VP1, VP2, VP3, VDDcomb and VCC8V
Status bit **XPR** is latched and cleared after an I2C-bus read action, unless the fault condition still exists. **XPR** is triggered when the pin **EHTO** is forced above 3.9V. **XPR=**1 will cause a slow-stop of **Hout**. This protection can be disabled by setting **XDT=**1.
Pin **EHTO** can be used for switch-off via the mains switch, using an external detection circuit to monitor when the supply voltage drops.
Pulling pin **PH2LF** above 4.1V will immediately stop H_{OUT}. If pin 17 is left floating again, the line drive will automatically restart (Unless software reacts to protection bits like **SUP** before H_{OUT} is restarted) :
- with **DFL=**0 it will do a gentle soft-restart.
- with **DFL=**1 it will immediately continue with normal H_{OUT} periods. This gives fastest recovery, but make sure that your line-deflection stage can handle it.

To prevent built-in protections from reacting on glitches, pins 17 or pin 32 must be kept above trigger voltage longer than 1 µs before the protection will act.
Status bit **NDF** is NOT latched. It is cleared after the fault condition is removed. In some chassis during source- or channel-change the vertical guard pulse is missing for some frames. Therefore it is adviced to check **NDF=**1 during at least > 200ms, before reacting to it in software (e.g. switch to standby).

Status bit **POR** is cleared after an I2C-bus read action, unless the reset condition still exists. **POR** is only related to the 3.3V part of the VSP and the reset input. It has nothing to do with the 5V part. When **POR=**1, all I2C register data needs to be rewritten after **POR=**0 again.

Bits **DFL4..0** represent the status of slow-start (-stop). With **DEFL**=1 the software can read this to monitor the line-start-up (-shut-down) process.
Important: when the 5V drops below a certain level (4V), other protection bits can accidentally get triggered. If e.g. **XPR**=1, the HOUT will NOT automatically restart. Therefore all UOC- III software should continuously check **POR**, **XPR** (or disable the protection functions).
Short spikes on the 5V supply can be handled by the UOCIII itself. If software reads **SUP**=0 for more than 40ms, we advice to switch to standby (**STB**=0).

14.4 +3.3V supply protection procedures

The behaviour of the 3.3V supply is shown in Figure 151. The different stages are described below.

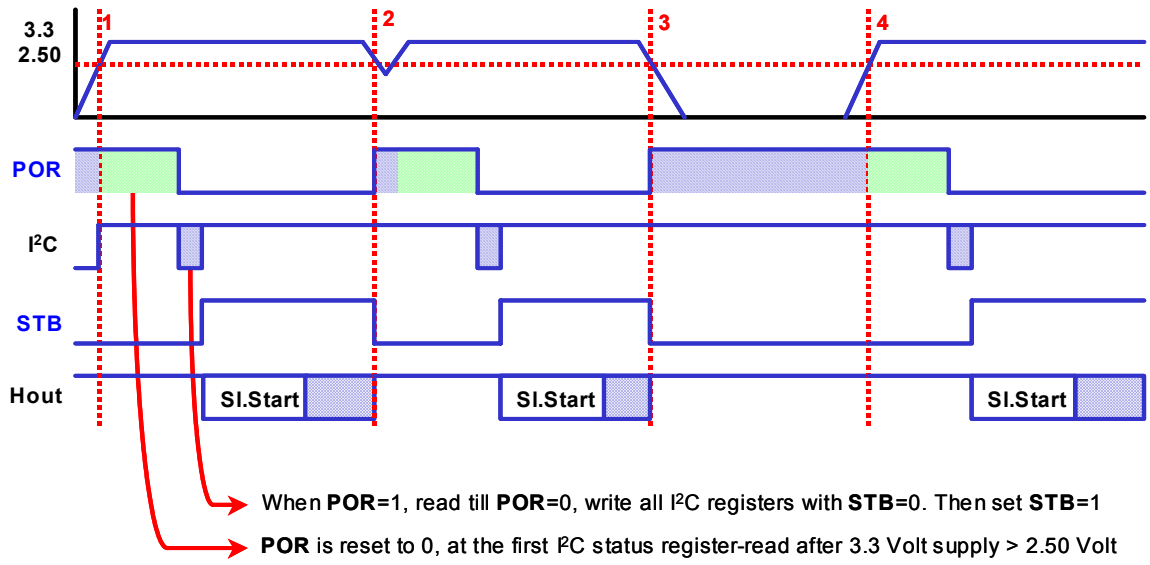

Figure 150. 3.3V supply behaviour

At **Stage 1 s**oftware must read the **POR** bit until it becomes 0. Then all I2C registers must be written with bit **STB** = 0. Bit **SUP** can be checked for 1. Then write **STB** = 1 to switch on H-out.

At **Stage 2** the power drops shortly below 2.5V. As a result the **POR** bit is set to 1 and latched. H-out is immediately switched off. When the software detects **POR** = 1, the start-up procedure as described in stage 1 must be repeated.

At **Stage 3** the power drops below 2.5V for a longer time. As a result again the Hout is immediately stopped and the device is put in reset condition.

At **Stage 4** the voltage rises above 2.50 V again. The start-up procedure as in **Stage 1** must be followed. The presence of the 3.3 Volt is basic for reliable working of the µprocessor part and the digital part (I2C registers and Hout drive circuit). Checking the 3.3 V regularly by reading **POR** and taking appropriate action when **POR** = 1 has absolute priority over all other matters.

14.5 +5V supply protection procedures (+5V from main supply)

Figure 151 represents the different stages depending on the +5V supply supplied from the main supply. Starting point is a correct working 3.3V supply.

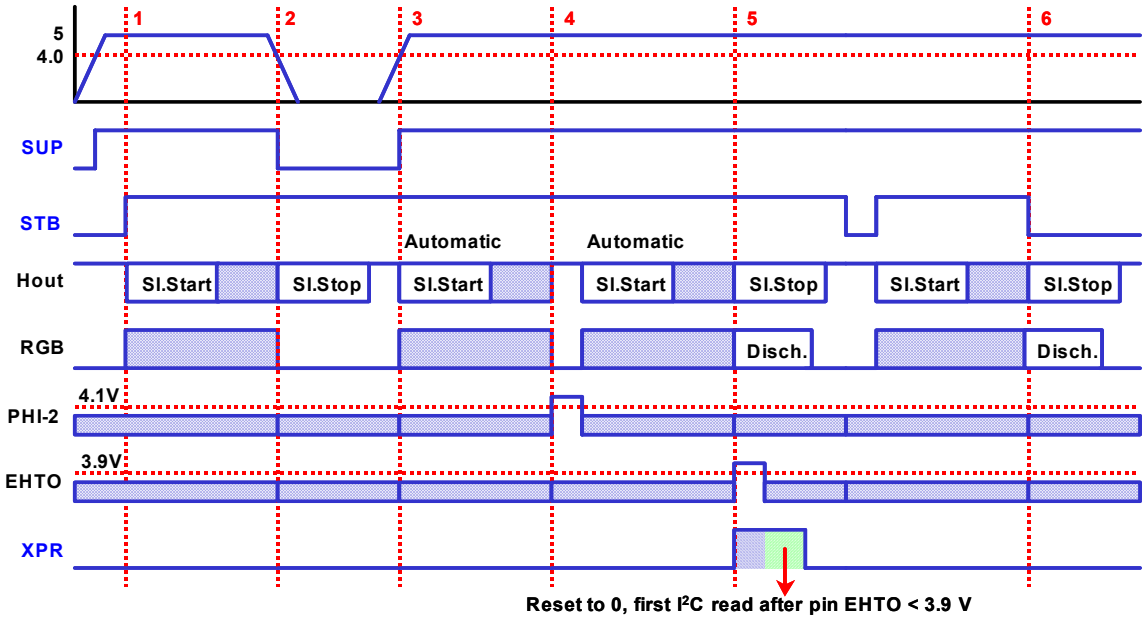

Figure 151. 5V supply behaviour (5V from main supply)

At **stage 1** bit **SUP** = 1 and bit **STB** may set to 1. This will cause Hout to start via Slow Start.

At **stage 2** when 5 V supply drops below 3.9 V, Hout will be stopped according the Slow Stop procedure. The RGB outputs are immediately blanked.

At **stage 3** the supply rises again above 4.1 V, Hout will automatically start again via Slow Start procedure.

At **stage 4** the Flash protection is activated when the voltage at pin **PHI-2** is kept above 4.1 V longer than 1 µs. Hout is immediately stopped to protect the line transistor and RGB outputs are blanked. When the voltage at pin **PHI-2** drops again below 6 Volts, Hout is automatically started via Slow Start.

At **stage 5** the Overvoltage protection is activated when the voltage at pin **EHTO** is kept above 3.9V longer than 1 µs. Bit **XPR** is set to 1 and Hout is switched off according the Slow Stop procedure. RGB outputs discharge the EHT and the IC is set in Stand-by. When **XPR** = 1, software must read till **XPR** = 0, then write **STB** = 0 followed by **STB** = 1

At **stage 6** **STB** is put to 0. As a result Hout is switched off via Slow Stop and the RGB outputs discharge the EHT.

14.6 +5V supply protection procedures (+5V from LOT)

Figure 152 represents the different stages depending on the +5V supply supplied from the LOT. Starting point is a correct working 3.3V supply.

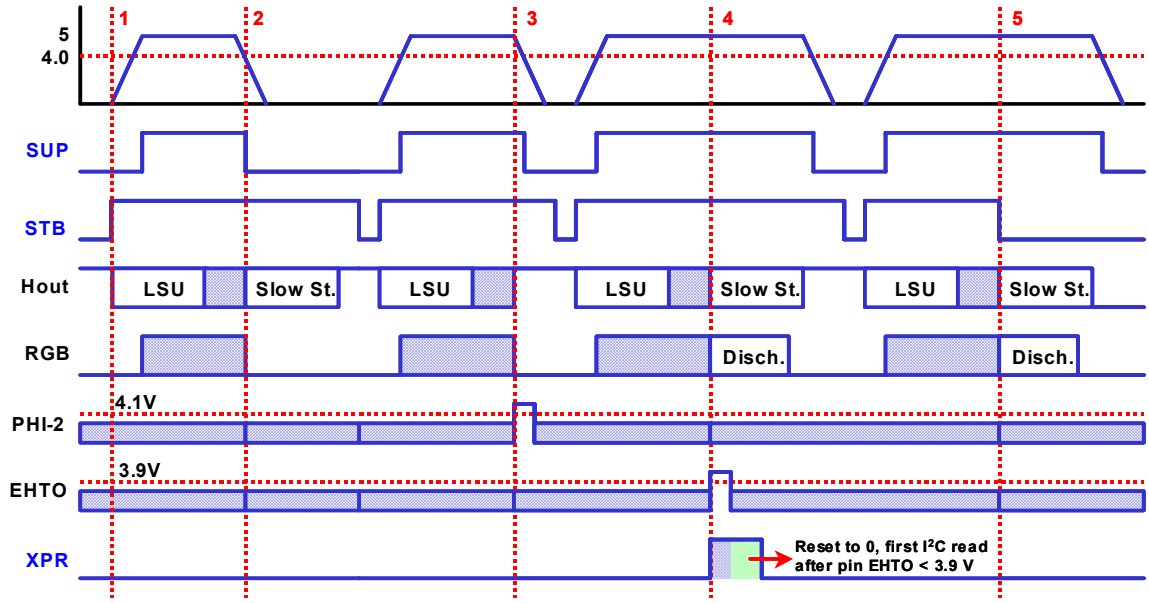

Figure 152. 5V supply behaviour (+5V from LOT)

At **stage 1** the 3.3V is ok and all I2C registers are written. Bit **STB** can be set to 1. Hout performs a Low voltage Start-up via Slow Start. The 5 Volt from FBT will rise. At 4.1 V all other video processor blocks are released.

At **stage 2** the 5 V drops below 3.9 V (e.g. due to overload). H-out will stop according the Slow Stop procedure and the RGB outputs are immediately blanked. Because the Hout is stopped, the 5 V will not return any more. The µprocessor can check this by monitoring the **SUP** bit. A new Low Voltage Start-up must be initiated by writing **STB** = 0 followed by **STB** = 1.

At **stage 3** the Flash protection stops immediately Hout and blanks the RGB outputs. Also now the 5 V doesn't return because Hout is stopped. A new Low Voltage Start-up must be initiated by toggling bit **STB.**

At **stage 4** overvoltage protection stops Hout via Slow Stop. RGB outputs discharge the EHT and the IC is set in Stand-by. The µprocessor must check **XPR** and **SUP** and when **XPR** = 0 initiate a new Low Voltage Start-up by toggling **STB**.

At **stage 5** bit **STB** = 0 switches off Hout via Slow Stop and the RGB outputs discharge the EHT.

14.7 Clock strategy

The clock structure has been shown in Figure 153.