AN1897
APPLICATION NOTE

VIPower: LOW COST UNIVERSAL INPUT DVD SUPPLY WITH VIPer22A

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INTRODUCTION

In the past few years, many consumer products have been provided to the end user, such as DVD or VCD players. Generally their power supply require multiple outputs to supply a variety of control circuits: MCU, Motor, Amplifier, VFD.

ST VIPer series of off-line switch mode power supply regulators combines an optimized, high voltage, avalanche rugged Vertical Power MOSFET with current mode control PWM circuitry. The result is truly innovative AC to DC conversion that is simpler, quicker and - with component count halved - less expensive.

The VIPer family also presents the easiest solution to comply with the "Blue Angel" and "Energy Star" Eco norms, with extremely low total power consumption at stand-by mode, thanks to the burst operation.

This document would present the application on DVD player power supply with VIPer22A satisfying the specification See table 1 below.

Table 1: Output Specification

INPUT	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	OUTPUT 6
Universal mains line	5 V +/- 5% (See note 1)	+12 V +/- 5% (See note 1)	-12 V +/- 5% (See note 1)	-26 V +/- 5% (See note 1)	3.3 V +/- 5% (See note 1)	$5V_{stb}$ +/- 5% (See note 1)
Min: 85Vac Max: 265Vac	Imin: 20mA Imax: 1.5 A	Imax: 30 mA	Imax: 30 mA	Imax: 50mA	Imax: 150mA	Imax: 100mA

Note 1: The accuracy of +/-5% is reached only for a certain range of loads combination. See paragraph 3.2 for cross regulation results.

1. APPLICATION DESCRIPTION AND DESIGN

1.1 Schematics

The overall schematic is shown in figure 2.

1.1.1 Start-up Phase

As any member of the VIPer family, VIPer22A has an integrated high voltage current source linked to Drain pin. At the startup converter, it will charge the V_{DD} capacitor until it reaches VIPer startup level (14.5V), and then the VIPer22A starts switching.

1.1.2 Auxiliary Supply

VIPer22A has a wide operating voltage range from 8V to 42V, respectively minimum and maximum values for under-voltage and over-voltage protections.

This function is very useful for achieving low stand-by total power consumption. During normal working, the feedback loop is connected to 5V output by D12 to regulate 5V output. At the mean time, +5Vstb output is blocked by Q3, so +5Vstb regulation is neglected. When the stand-by signal is present, the Vce of Q3 can not provide enough voltage to maintain D12 conducted, so the 5V output is blocked, and the +5Vstb output is connected to the feedback loop. In this condition the +5Vstb is regulated. Thanks to the transformer structure, all the other secondary outputs and the auxiliary voltages are pulled down to a very low level, also pulling down the total power consumption.

All these contents can be summarized by the following list:

- in normal full load, the V_{DD} voltage of the device must be lower than the over-voltage protection;
- in short circuit, the V_{DD} voltage must be lower than the shutdown voltage. Actually, this condition leads to the well known hiccup mode in practice;
- in no load condition, the V_{DD} voltage must be higher than the shutdown voltage.

1.1.3 Burst Mode

The Viper22A integrates a current mode PWM with a Power MOSFET and includes the leading edge blanking function. The burst mode is a feature which allows VIPer22A to skip some switching cycles when the energy drained by the output load goes below $E=(T_b*V_{in})^2 * f_{sw}/2L_p$ (T_b=blanking time, V_{in}=DC input voltage, f_{sw}=Switching frequency, L_p=Primary Inductance).

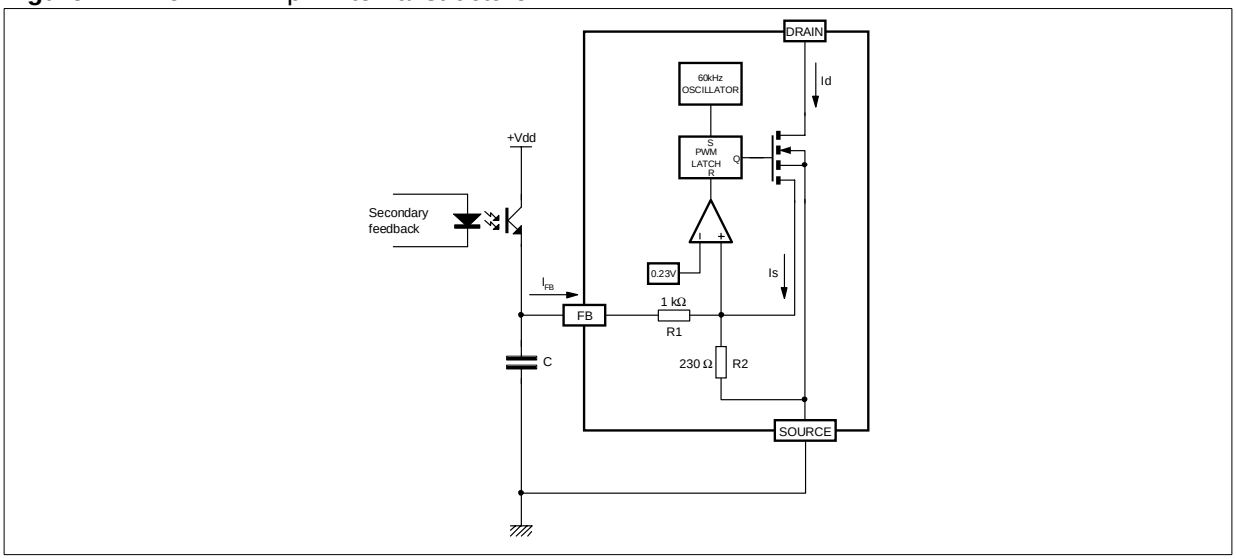
It has the consequence to reduce the switching losses when working in low load condition by reducing the switching frequency.

1.1.4 Feedback Loop

The 5V output voltage is regulated with a TL-431 (U3) via an optocoupler (U2) to the feedback pin. If the output voltage is high, the TL-431 will draw more current through its cathode to the anode and the current increases in the optocoupler diode. The current in optocoupler NPN increases accordingly and the current into the VIPer22A FB pin increases. When the FB current increases, the VIPer22A will skip some cycles to decrease turn on time and lower the output voltage to the proper level (see figure 1).

The 5V output voltage is regulated thanks to the reference voltage of TL-431 and the resistive divider R8 and R9.

Figure 1: VIPer22A FB pin internal structure



1.1.5 Primary Driver

In a fly-back power supply, the transformer is used as an energy tank fuelled during the ON time of the MOSFET. When the MOSFET turns off, its drain voltage rises from a low value to the input voltage plus the reflected voltage while the secondary diode conducts, transferring on the secondary side the magnetic energy stored in the transformer. Because primary and secondary windings are not perfectly magnetically coupled, there is a serial leakage inductance that behaves like an open inductor charged at I_{pk} that causes the voltage spikes on the MOSFET drain. These voltage spikes must be clamped to keep the VIPer22A Drain voltage below the BVdss (730Vmin) rating. If the peak voltage is higher than this value, the device will be destroyed. The most used solution is the RCD clamp (see figure 3). This is a very simple and cheap solution, but it impacts on the efficiency and even on the power dissipation in stand-by condition. Also the clamping voltage varies with load current. RCD clamp circuits may allow the drain voltage to exceed the data sheet breakdown rating of VIPer22A during overload operation or during turn on with high line AC input voltage. So, a zener clamp is recommended (see figure 4). However such a solution gives higher power dissipation at full load, even if the clamp voltage is exactly defined.

1.2 Transformer Consideration

On the electrical specification of a multiple output transformer (cross regulation, leakage inductance), the main efforts focused on the proper coupling between the windings. A lower leakage inductance transformer will allow a lower power clamp to reduce the input power. It will lead to lower power dissipation on the primary side.

Auxiliary and secondary windings are swapped in order to decrease the coupling to the primary one. The secondary windings act as a shielding layer to reduce the capacitive coupling. Fewer spikes are generated on the auxiliary windings, the primary and secondary windings have better coupling.

Designing transformers for low leakage inductance involves several considerations:

- Minimize number of turns
- Keep winding build (ratio of winding height to width) small
- Increase width of windings
- Minimize insulation between windings
- Increase coupling between windings

Figure 2: Application schematic

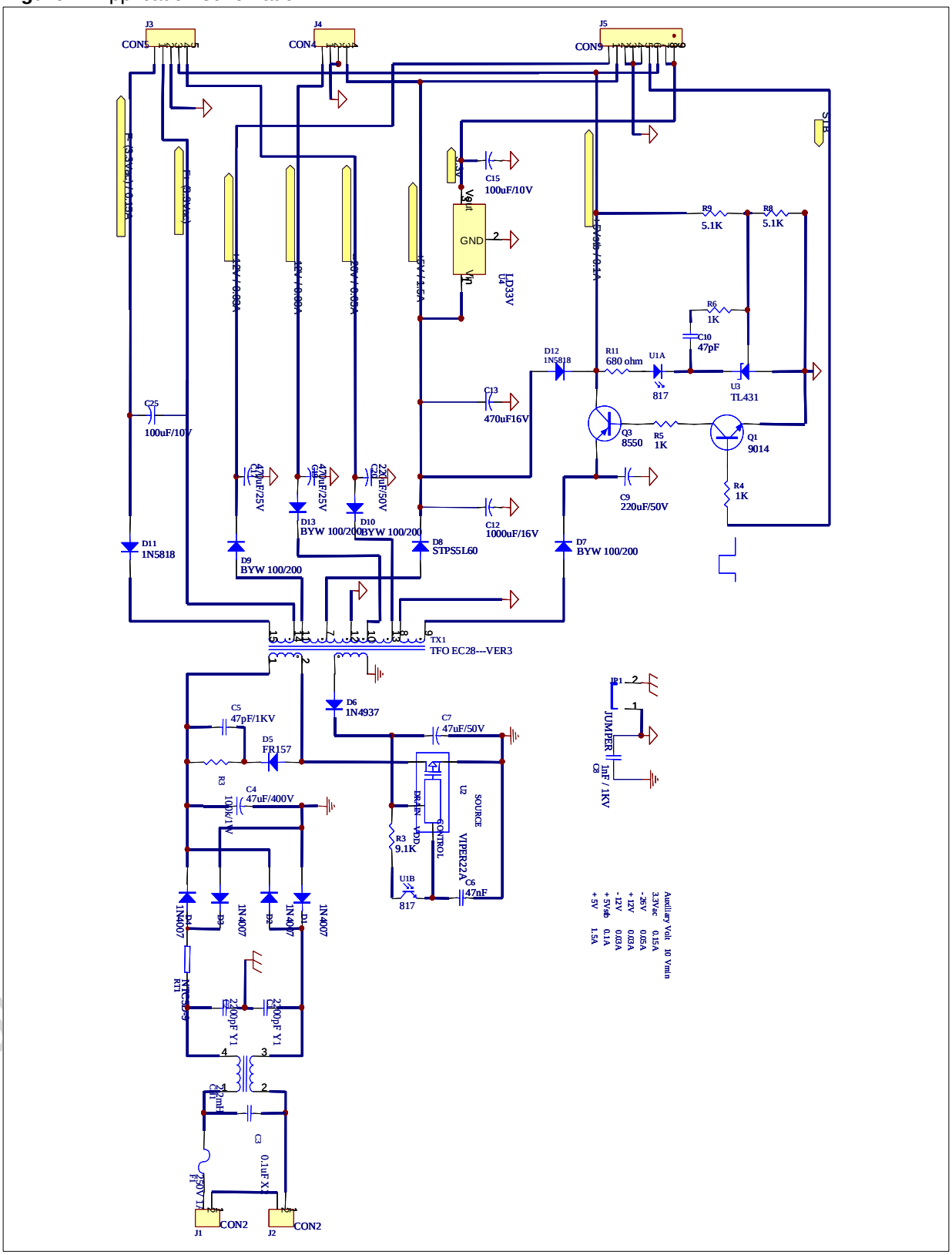


Figure 3: RCD clamp topology

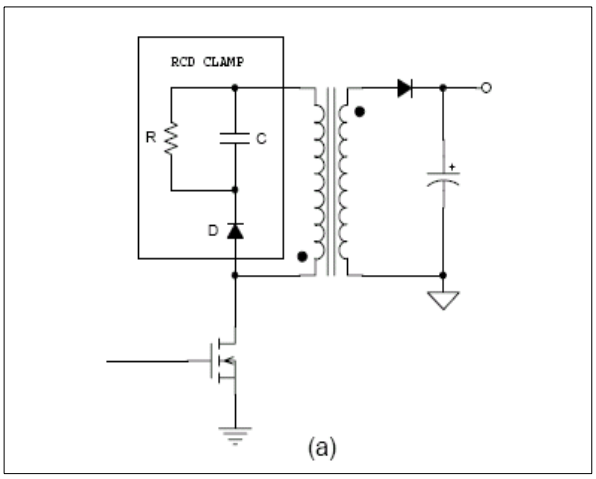
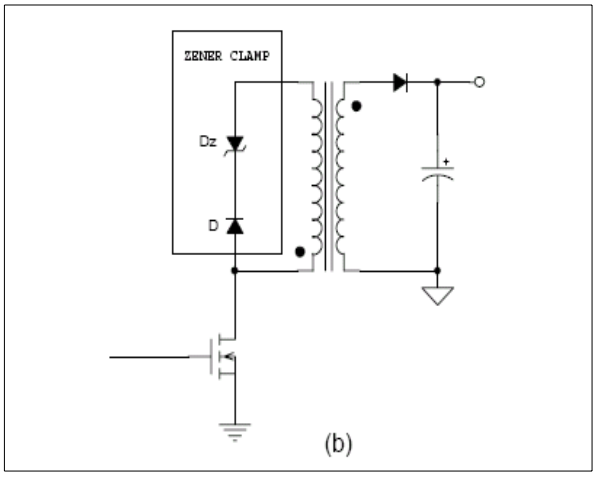


Figure 4: Zener clamp topology



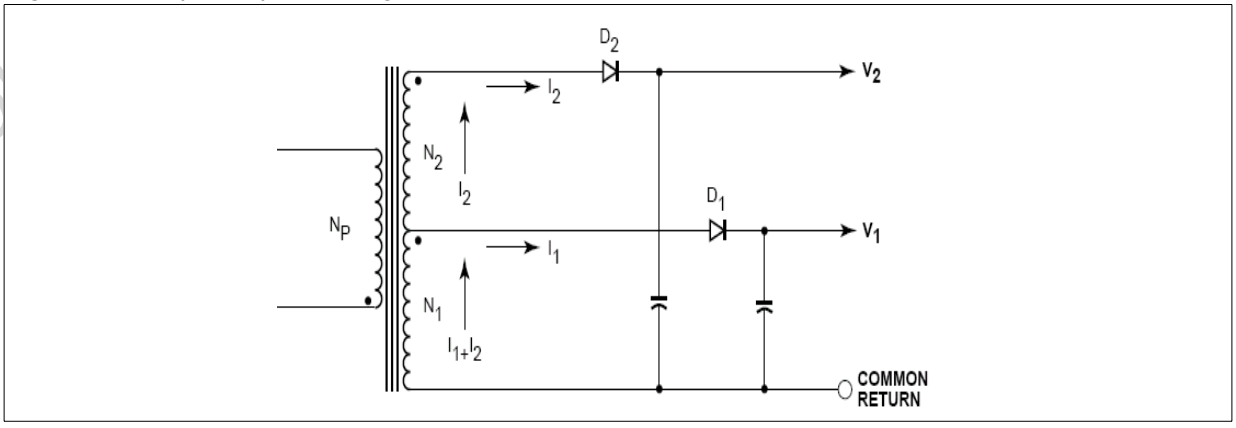
For a transformer meeting international insulation and safety requirements, a practical value for leakage inductance is about 1-3% of the open circuit primary inductance.

A high efficiency transformer should have low inter-winding capacitance to decrease the switching losses. Energy stored in the parasitic capacitance of the transformer is absorbed by VIPer cycle by cycle during the turn-on transition. Excess capacitance will also ring with stray inductance during switch transitions, causing noise problems. Capacitance effects are usually the most important in the primary winding, where the operating voltage (and consequent energy storage) is high. The primary winding should be the first winding on the transformer. This allows the primary winding to have a low mean length per turn, reducing the internal capacitance. The driven end of the primary winding (the end connected to the Drain pin) should be the beginning of the winding rather than the end.

This takes advantage of the shielding effect of the second half of the primary winding and reduces capacitive coupling to adjacent windings. A layer of insulation between adjacent primary windings can cut the internal capacitance of the primary winding by as much as a factor of four, with consequent reduction of losses. A common technique for winding multiple secondaries with the same polarity sharing a common return, is to stack the secondaries (see figure 5). This arrangement will improve the load regulation, and reduce the total number of secondary turns.

Commonly a clamper based on an RCD network or a diode with a zener to clamp the rise of the drain voltage is used.

Figure 5: Multiple output winding



2. LAYOUT RECOMMENDATION

Since EMI issues are strongly related to layout, a basic rule has to be taken into account in high current path routing, i.e. the current loop area has to be minimized. If a heat-sink is used it has to be connected to ground too, in order to reduce common mode emissions, since it is close to the floating drain tab.

One more consideration has to be made regarding the control ground connection: in fact in order to avoid any noise interference on VIPer logic pin the control ground has to be separated from power ground.

3. EXPERIMENTAL RESULT

3.1 Efficiency

Figure 6: Efficiency at 230Vac (Load on 5V)

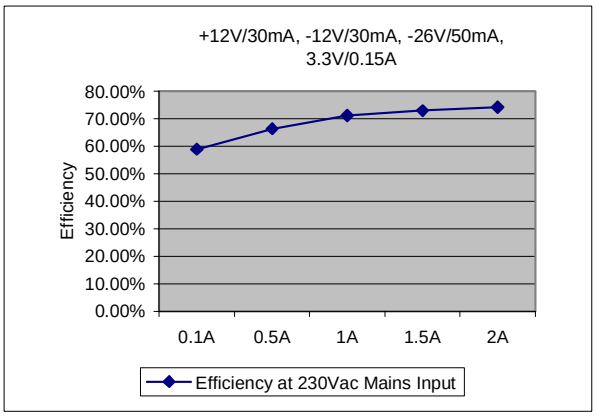


Figure 7: Efficiency at 260Vac (Load on 5V)

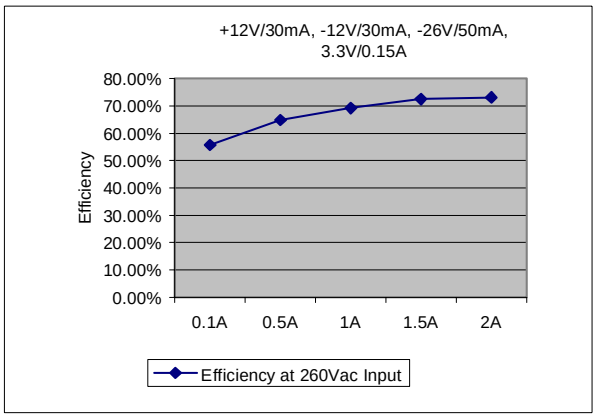


Figure 8: Efficiency at 85Vac (Load on 5V)

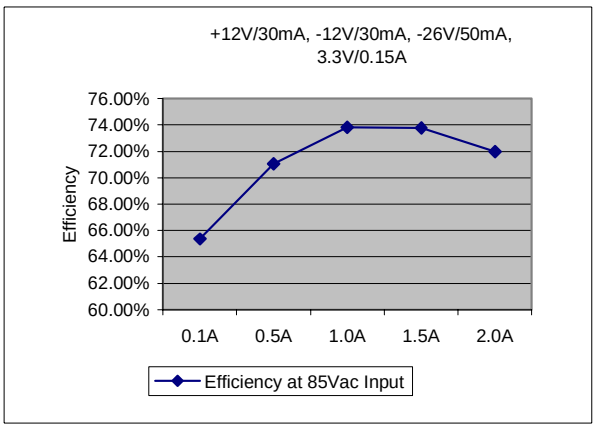
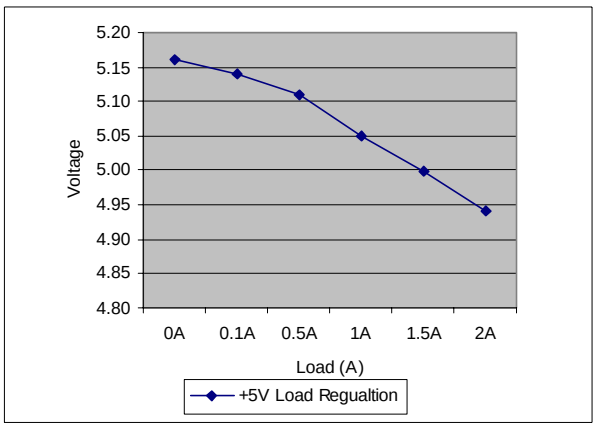


Figure 9: Load Regulation (load on +5V)



3.2 Regulation

Table 2: Line regulation

Output	85Vac	230Vac	260Vac
5V/ 0.1A	5.15V	5.15V	5.15V
5Vstb/ 0A	5.15V	5.15V	5.15V
12V/ 0A	12.08V	12.11V	12.12V
-12V/ 0A	-11.98V	-11.99V	-12.00V
-26V/ 0A	-25.82V	-25.85V	-25.86V
3.3V/ 0A	3.87V	3.87V	3.88V

Figure 10: Cross regulation

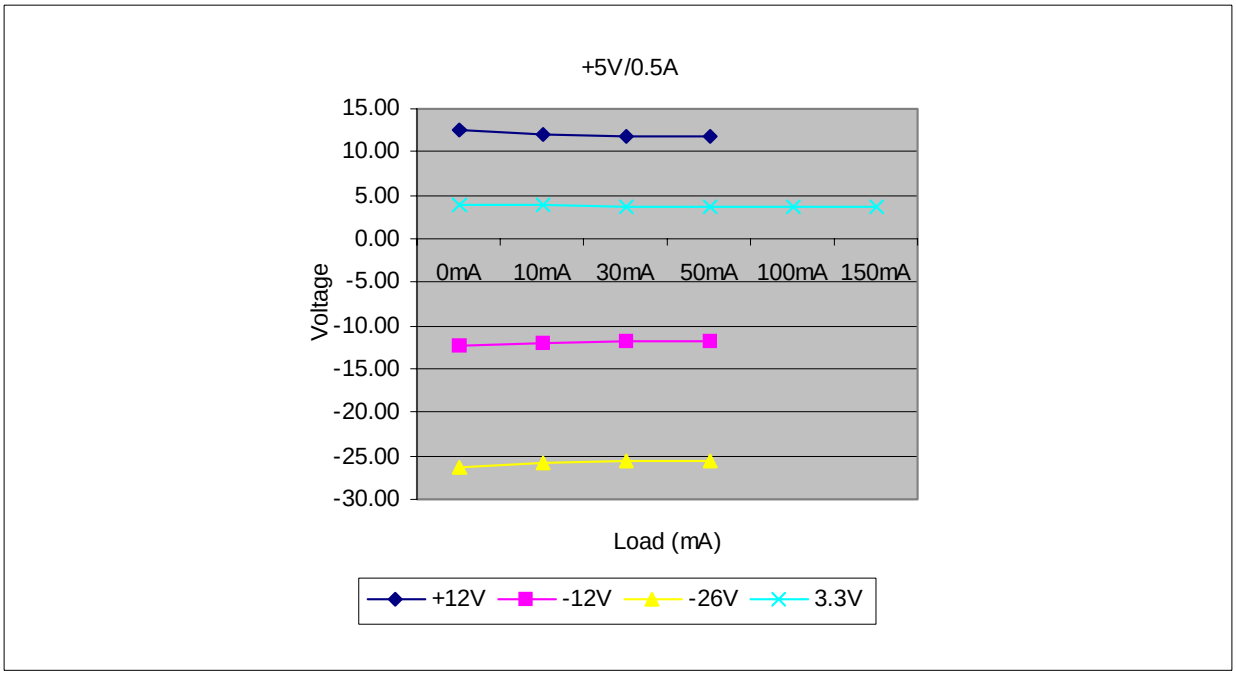


Table 3: Stand by model

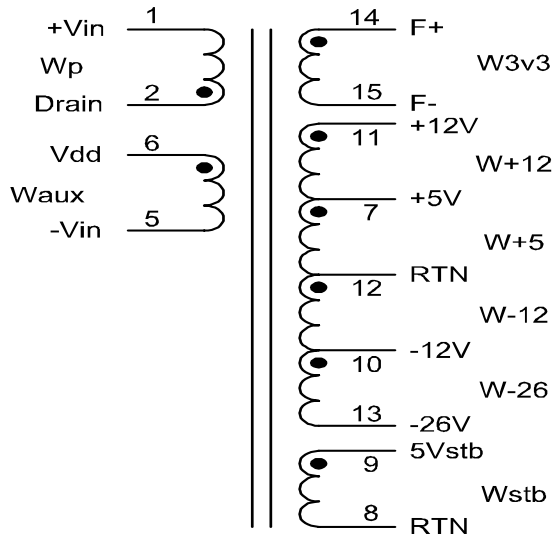
Output	85Vac	230Vac	260Vac
5V	2.05V	2.05V	2.07V
5Vstb (100mA)	5.08V	5.11V	5.14V
12V	4.00V	3.99V	3.98V
-12V	3.99V	3.99V	3.98V
-26V	9.12V	9.10V	9.08V
3.3V	1.70V	1.50V	1.51V
Pdis	0.8W	1W	1.1W

Table 4: Full Load Regulation

Output	85Vac	230Vac	260Vac
5V/ 1.5A	5.02V	5.09V	5.08V
5Vstb/ 0A	5.02V	5.09V	5.08V
12V/30mA	12.03V	12.06V	12.05V
-12V/30mA	-12.01V	-12.05V	-12.05V
-26V/50mA	-26.06V	-26.16V	-26.15V
3.3V/0.15A	3.77V	3.80V	3.78V
VIPer Temp	53°C	47°C	45°C

4. TRANSFORMER SPECIFICATION

Figure 11: Transformer Structure



Primary inductance: Lp = 2.8 mH 1KHz, 0.3V
Leakage inductance: Lk < 28uH at Secondary and auxiliary winding short (1KHz, 0.3V)
Core: EER28L
Bobbin: ER28 (6 + 9 Pin)
Vendor: YuanDongDa electronics Co., Ltd

Table 5: Winding Parameters

Layers description	Symbol	Start Pin	End Pin	Number of Layer	Turns	Wire Size (mm)
Primary	Wp	Pin2	Pin1	2	65	0.3
Out1 (5V/1.5A)	W5	Pin7	Pin12	1	4	2*0.6
Out2 (12V/0.03A)	W12	Pin11	Pin7	1	5	0.3
Out3 (-12V/0.03A)	W-12	Pin12	Pin10	1	9	0.45
Out4 (-26V/0.05A)	W-26	Pin10	Pin13	1	10	0.3
Out5 (5Vstb/0.1A)	Wstb	Pin9	Pin8	1	12	0.3
Out6 (3.3V/0.15A)	W3v3	Pin14	Pin15	1	3	0.3
Auxiliary	Waux	Pin6	Pin5	1	24	0.3

BOBBIN								
	Barrier (3mm)							
	Wp	W5	W12	W-12	W-26	W3v3	Wstb	Waux
	2 1	7	11	12	10	14	9	6
	Barrier (3mm)							

5. PCB LAYOUT

Figure 12: Bottom view of the demo board (not in scale)

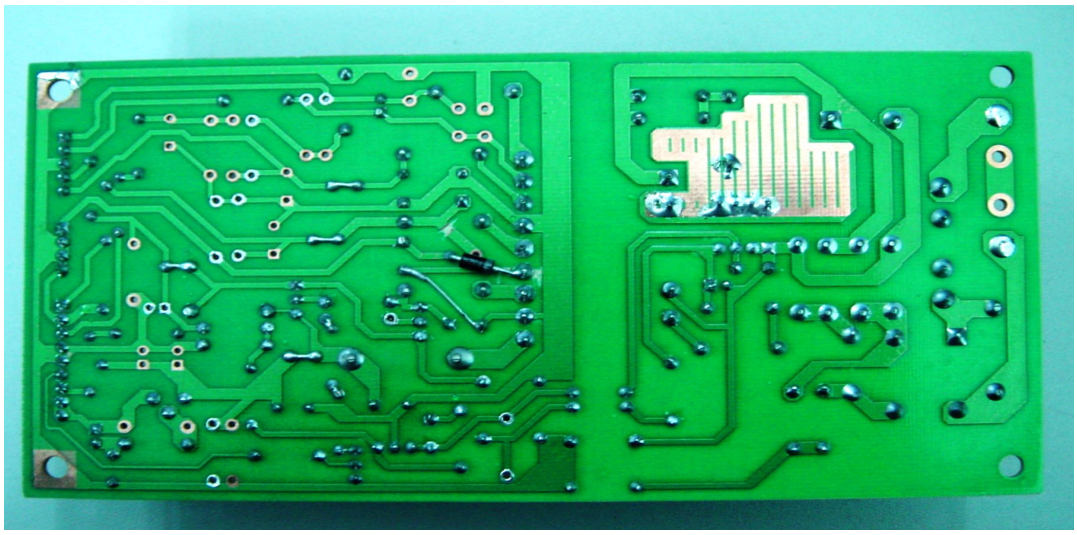
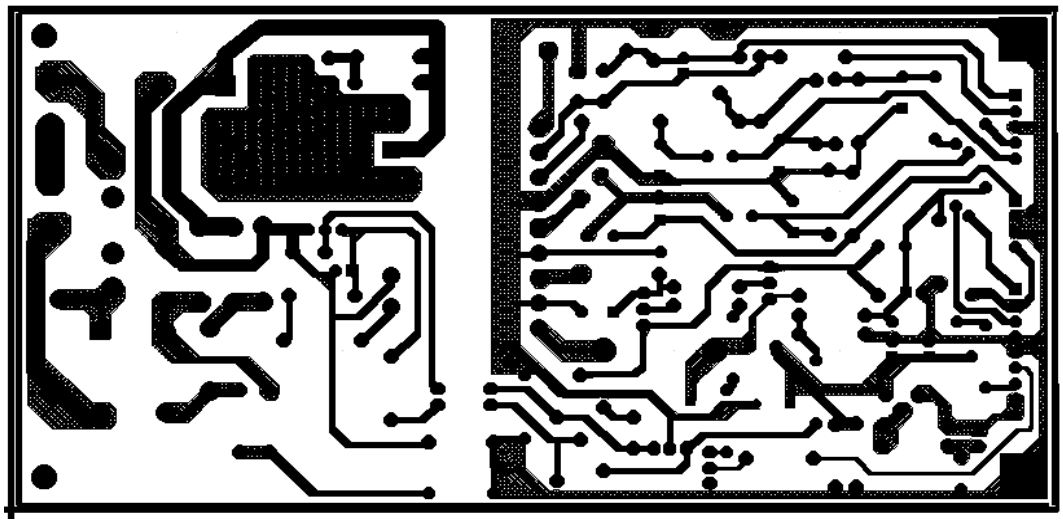


Figure 13: PCB Art Work (not in scale)



5. BILL OF MATERIALS

Ref.	Description	Note
U1	Photocoupler PC817	SHARP
U2	VIPer22A DIP	**STMicroelectronics**
U3	TL431 ACZ	**STMicroelectronics**
U4	L4931 ABV33	**STMicroelectronics**
Q1	SS9014	
Q3	SS8550	
D1, D2, D3, D4	1N4007	
D5	FR157	
D6, D7, D9, D10, D13	STTH102	**STMicroelectronics**
D8	STPS5L60	**STMicroelectronics**
D11, D12	1N5818	**STMicroelectronics**
C1, C2	Y1 Capacitor 2200pF	
C3	X2 Capacitor 0.1uF	
C4	Electrolytic Capacitor 100uF/400V	
C5, C8	1nF/1KV	
C6	Ceramic Capacitor 47nF/50V	
C7	Electrolytic Capacitor 47uF/50V	
C9	Electrolytic Capacitor 220uF/50V	
C10	Ceramic Capacitor 47pF/50V	
C12	Electrolytic Capacitor 1000uF/16V	
C13	Electrolytic Capacitor 470uF/16V	
C15	Electrolytic Capacitor 100uF/10V	
C17	Electrolytic Capacitor 470uF/25V	
C19	Electrolytic Capacitor 470uF/25V	
C20	Electrolytic Capacitor 220uF/50V	
C25	Electrolytic Capacitor 220uF/16V	
RT1	Not fit	
R2	9.1KΩ ¼ W	
R3	100KΩ 1W	
R4, R5, R6	1KΩ ¼ W	
R8, R9	5.1KΩ ¼ W	
R11	680Ω ¼ W	
CH1	2.2mH Common choke	
TX1	EER28 transformer	
F1	Fuse 1A	
J1, J2	2pin connector	
J3	5pin connector	
J4	4pin connector	
J5	9pin connector	