Layout Guidelines (Cont.)

Next, looking at the switcher power section, the schematic in Figure 10 below shows the power section for VDDQ:

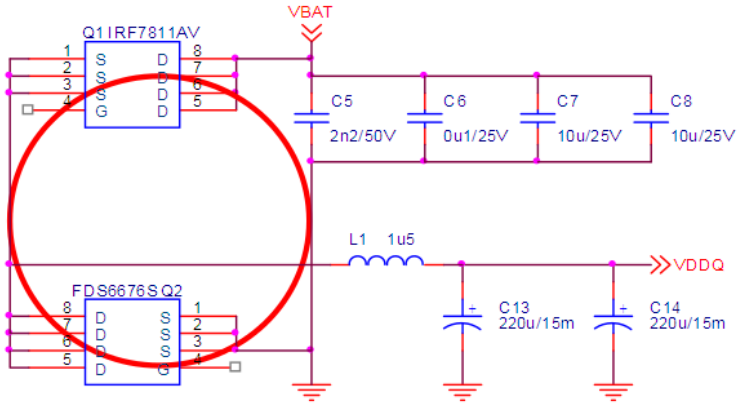

Figure 10: VDDQ Power Section and Input Loop

The highest di/dts occur in the input loop (highlighted in red) and thus this should be kept as small as possible. The input capacitors should be placed with the highest frequency capacitors closest to the loop to reduce EMI. Use large copper pours to minimize losses and parasitics. See Figure 11 below for an example.

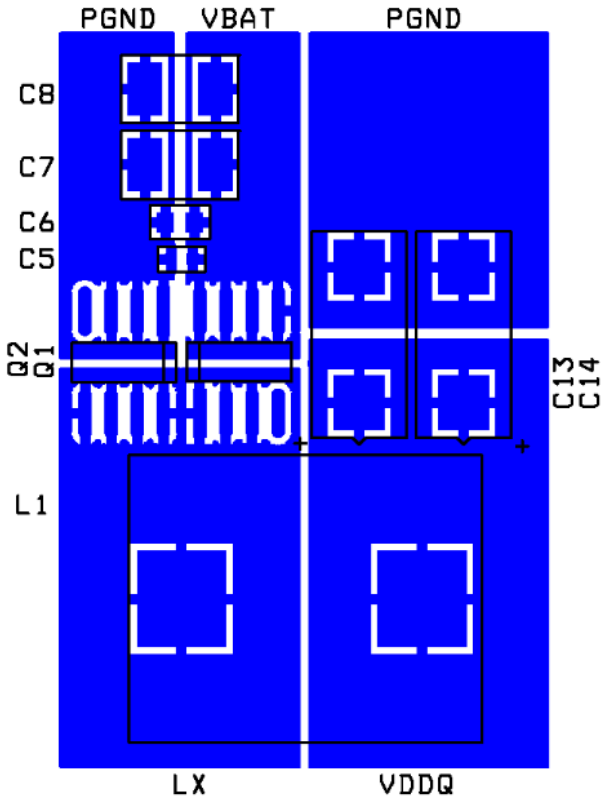

Figure 11: Example VDDQ Power Section Layout