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Renesas Electronics website: http://www.renesas.com

April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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M62429P/FP

Serial Data Control Dual Electronic Volume

REJ03F0209-0300 Rev.3.00 Jun 15, 2007

Description

The M62429 is a dual channel electronic volume controlled with 2-wire serial data.

The built-in reference circuit can compose of an electronic volume with less external parts.

Features

• Built-in reference circuit

• Control with serial data Volume 0 to −83 dB (1 dB/step), −∞ (Independent control is allowed in each channel)

• Low noise and low distortion

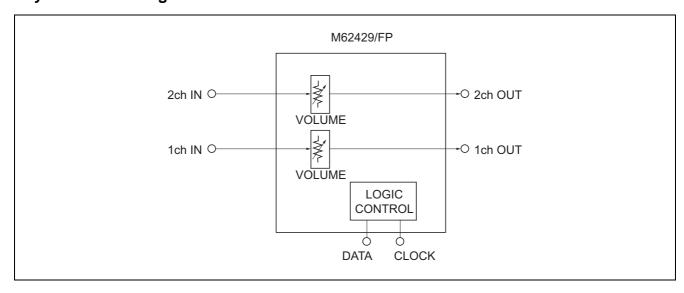
VNO = 5 μ Vrms (ATT = $-\infty$, JIS-A) THD = 0.01 % Typ. (V0 = 0.5 Vrms, DIN-AUDIO)

Recommended Operating Conditions

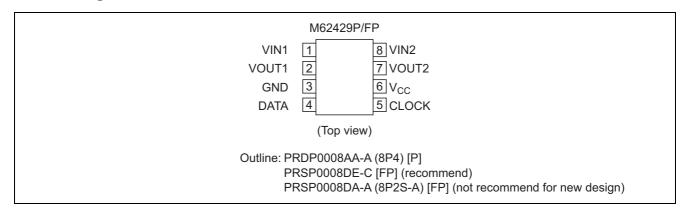
Supply voltage range: $V_{CC} = 4.5$ to 5.5 V

Rated supply voltage: $V_{CC} = 5 \text{ V}$

System Block Diagram



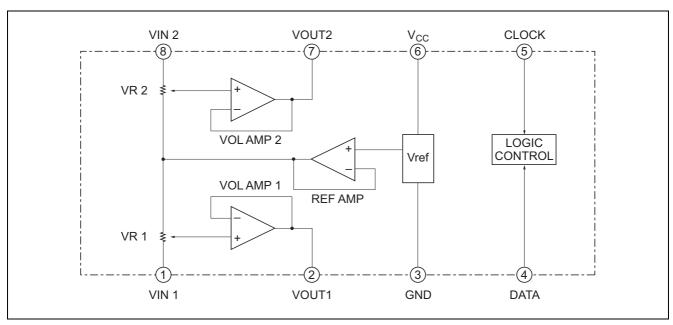
Pin Arrangement



Pin Description

Pin No.	Symbol	Function
1	VIN1	1-ch input pin
2	VOUT1	1-ch output pin
3	GND	Ground pin
4	DATA	Control data input pin. Inputs data in synchronization with clock.
5	CLOCK	Clock input pin for transferring serial data.
6	V _{CC}	Power supply pin. Stabilize the pin with decoupling capacitor.
7	VOUT2	2-ch output pin
8	VIN2	2-ch input pin

IC Internal Block Diagram



Absolute Maximum Ratings

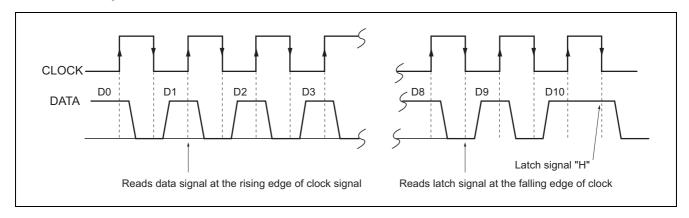
Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}, V_{DD}	6.0	V
Power dissipation	Pd	625 (P), 440 (FP)	mW
Operating temperature	Topr	−20 to +75	°C
Storage temperature	Tstg	-55 to +125	°C

Electrical Characteristics

 $(V_{CC} = 5 \text{ V}, \text{ Ta} = 25 \text{ }^{\circ}\text{C}, \text{ unless otherwise noted})$

		Limits				
Item	Symbol	Min	Тур	Max	Unit	Conditions
Circuit current	Icc	_	8	16	mA	
Maximum attenuation	A _{TT}	_	-90	-80	dB	$A_{TT} = -\infty$
Attenuation error	ΔA_{TT}	-2.0	0	2.0	dB	$A_{TT} = 0$
Maximum input voltage	V_{IM}	1.5	1.7	_	Vrms	THD = 1 %, A _{TT} = -6 dB
Maximum output voltage	V _{OM}	0.8	1.3	_	Vrms	THD = 1 %
Output noise voltage	V _{NO} 1	_	4	10	μVrms	$A_{TT} = 0$, $Rg = 0$, JIS-A
	V _{NO} 2	_	5	10		$A_{TT} = -\infty$, $Rg = 0$, JIS-A
Total harmonic distortion	THD	_	0.01	0.05	%	f = 1 kHz, Vo = 0.5 Vrms, A _{TT} = 0
Channel separation	CS	_	-80	-70	dB	f = 1 kHz, JIS-A

Relationship between Data and Clock



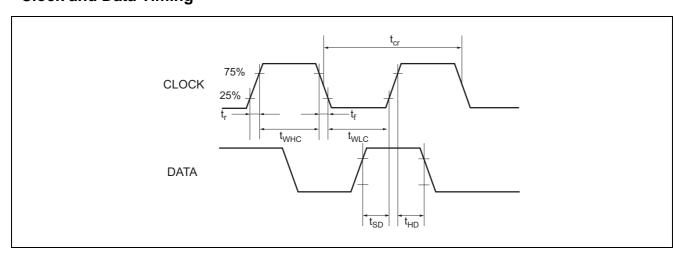
DC Characteristics of Digital Block

		Limits					
Item	Symbol	Min	Тур	Max	Unit	Tes	t Conditions
"L" level input voltage	V _{IL}	0	~	0.2 V _{CC}	V	Data, clock	pin
"H" level input voltage	V _{IH}	0.8 V _{CC}	~	V _{CC}	V		
"L" level input current	I _{IL}	-10	_	10	μΑ	$V_I = 0$	Data, clock pin
"H" level input current	I _{IH}	_	_	10	μА	$V_I = 5 V$	

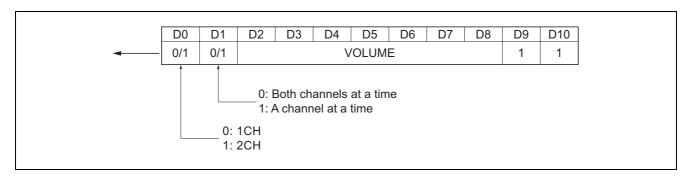
AC Characteristics of Digital Block

	Limits				
Item	Symbol	Min	Тур	Max	Unit
Cycle time of clock	t _{cr}	4	_	_	μS
Pulse width of clock ("H" level)	twnc	1.6	_	_	μS
Pulse width of clock ("L" level)	t _{WLC}	1.6	_	_	μS
Clock rising time	t _r	_	_	0.4	μS
Clock falling time	t _f	_	_	0.4	μS
Data setup time	t _{SD}	0.8	_	_	μS
Data hold time	t _{HD}	0.8	_	_	μS

Clock and Data Timing



Data Input Format

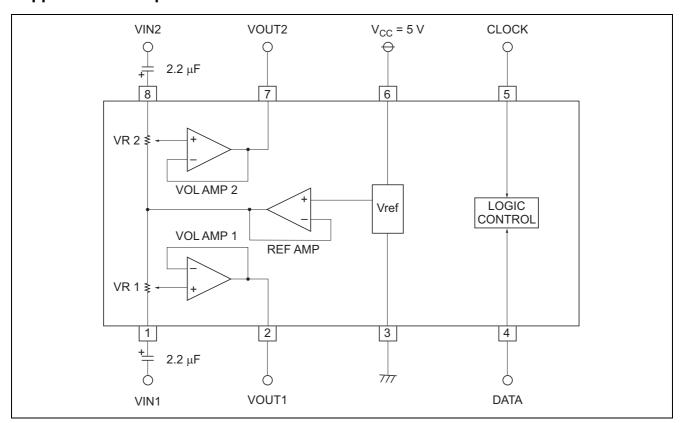


Volume Code

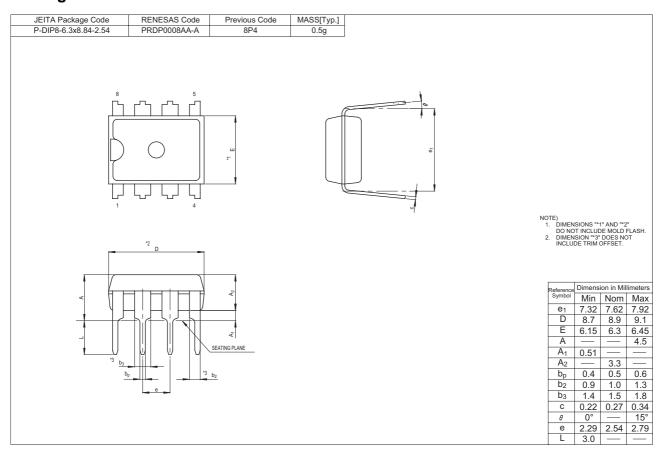
ATT1	D2	D3	D4	D5	D6
0 dB	Н	L	Н	L	Н
–4 dB	L	L	Н	L	Η
–8 dB	Н	Н	L	L	Η
–12 dB	L	Н	L	L	Н
–16 dB	Н	L	L	L	Н
–20 dB	L	L	L	L	Н
–24 dB	Н	Н	Н	Н	L
–28 dB	L	Н	Н	Н	L
–32 dB	Н	L	Н	Н	L
–36 dB	L	L	Н	Η	L
–40 dB	Н	Н	L	Η	L
–44 dB	L	Н	L	Η	L
–48 dB	Н	L	L	Н	L
–52 dB	L	L	L	Н	L
–56 dB	Н	Н	Н	L	L
–60 dB	L	Н	Н	L	L
–64 dB	Н	L	Н	L	L
–68 dB	L	L	Н	L	L
–72 dB	Н	Н	L	L	L
–76 dB	L	Н	L	L	L
–80 dB	Н	L	L	L	L
-∞	L	L	L	L	L

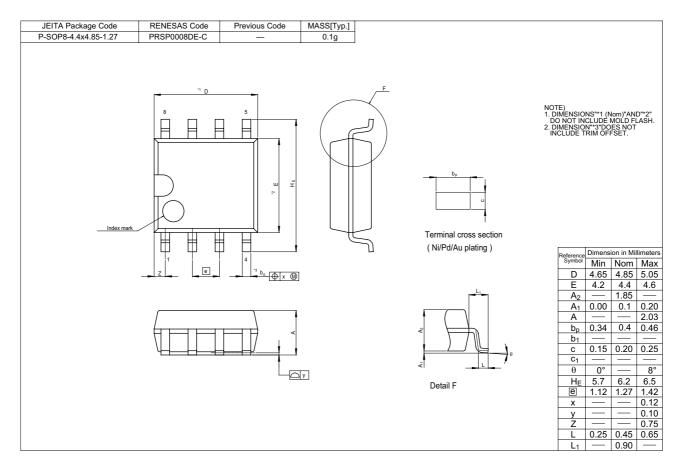
ATT2	D7	D8
0 dB	Н	Н
–1 dB	L	Н
−2 dB	Н	L
−3 dB	L	L

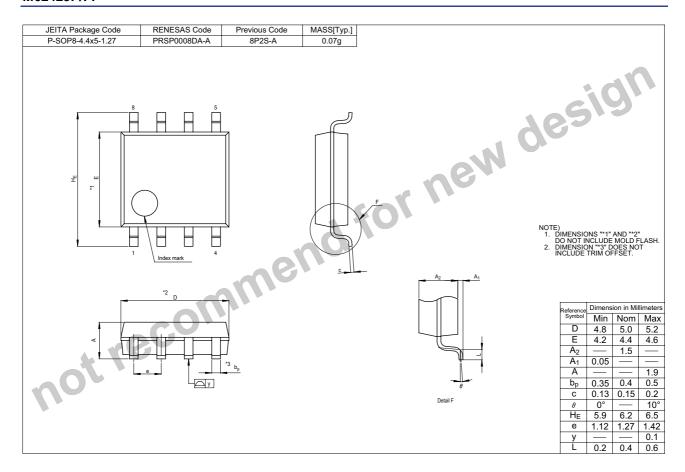
Application Example



Package Dimensions







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