16 MULTI-FUNCTION LED DRIVER AND GPIO CONTROLLER WITH I²C INTERFACE

FEATURES

- **16 multi-function I/O, each for LED drive (current-source dimming) or GPIO mode**
- **256 steps linear dimming in LED drive mode**
- **Any GPIO can be configured as an input or an output independently**
- **Support interrupt, 8us deglitch, low-level active**
- **Standard I²C interface, AD1/AD0 select I²C device address**
- SDA, SCL, SHDN, and all GPIO can accept in 1.8V logic input
- ESD protection: ±4000V HBM (MIL-STD-883H Method 3015.8 standard）
- Latch-up：±450mA（JEDEC STANDARD NO.78C SEPTEMBER 2010 standard）
- Supply shutdown function, low-level active
- 2.5V~5.5V power supply

APPLICATION RANGE

- Cell Phone
- PDA/MP3/MP4/CD/Minidiskplay

INTRODUCTION

AW9523B is a 16 multi-function LED driver and GPIO controller. Any of the 16 I/O ports can be configured as LED drive mode or GPIO mode. Furthermore, any GPIO can be configured as an input or an output independently.

After power on, all the 16 I/O ports are configured as GPIO output as default, which default states are set according to the I²C device address selection inputs, AD0 and AD1. All I/O ports configured as inputs are continuously monitored for state changes. State changes are indicated by the INTN output. When AW9523B reads GPIO state through the I²C interface, the interrupt is cleared. Interrupt has 8us deglitch.

When the I/O ports are configured as LED drive mode, AW9523B can set the current of LED drive between 0~IMAX by I²C interface, which is divided by 256 steps linear dimming. The default maximum current (IMAX) is 37mA, and IMAX can be changed in GCR register.

AW9523B is available in TQFN4X4-24L package, and 2.5V~5.5V power supply.

PIN CONFIGURATION AND MARKING

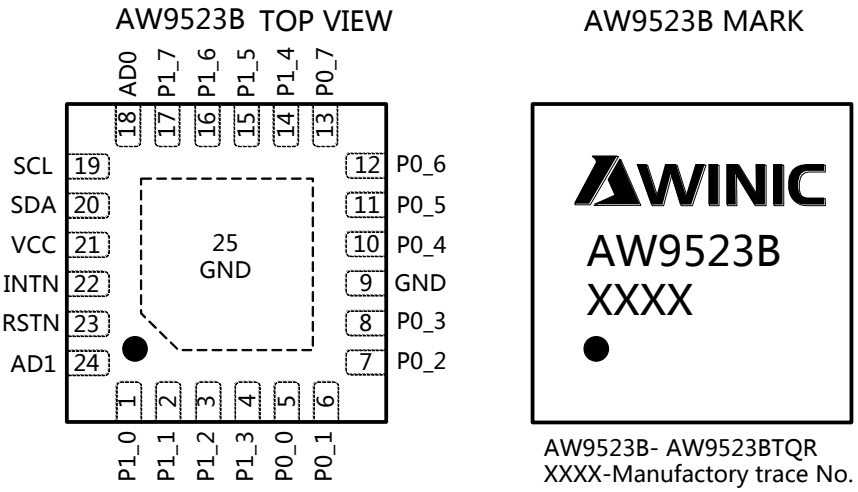
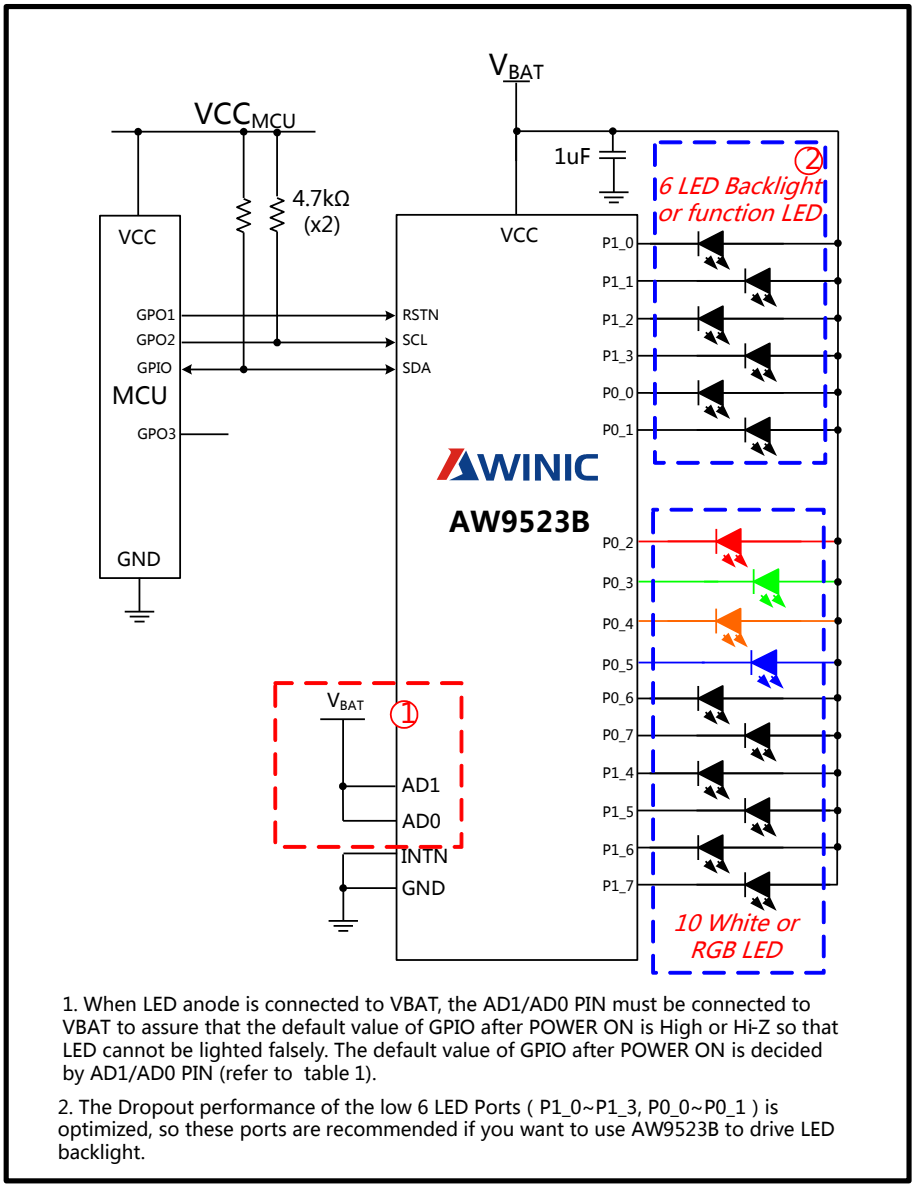


Figure 1 AW9523B PIN CONFIGURATION AND MARKING

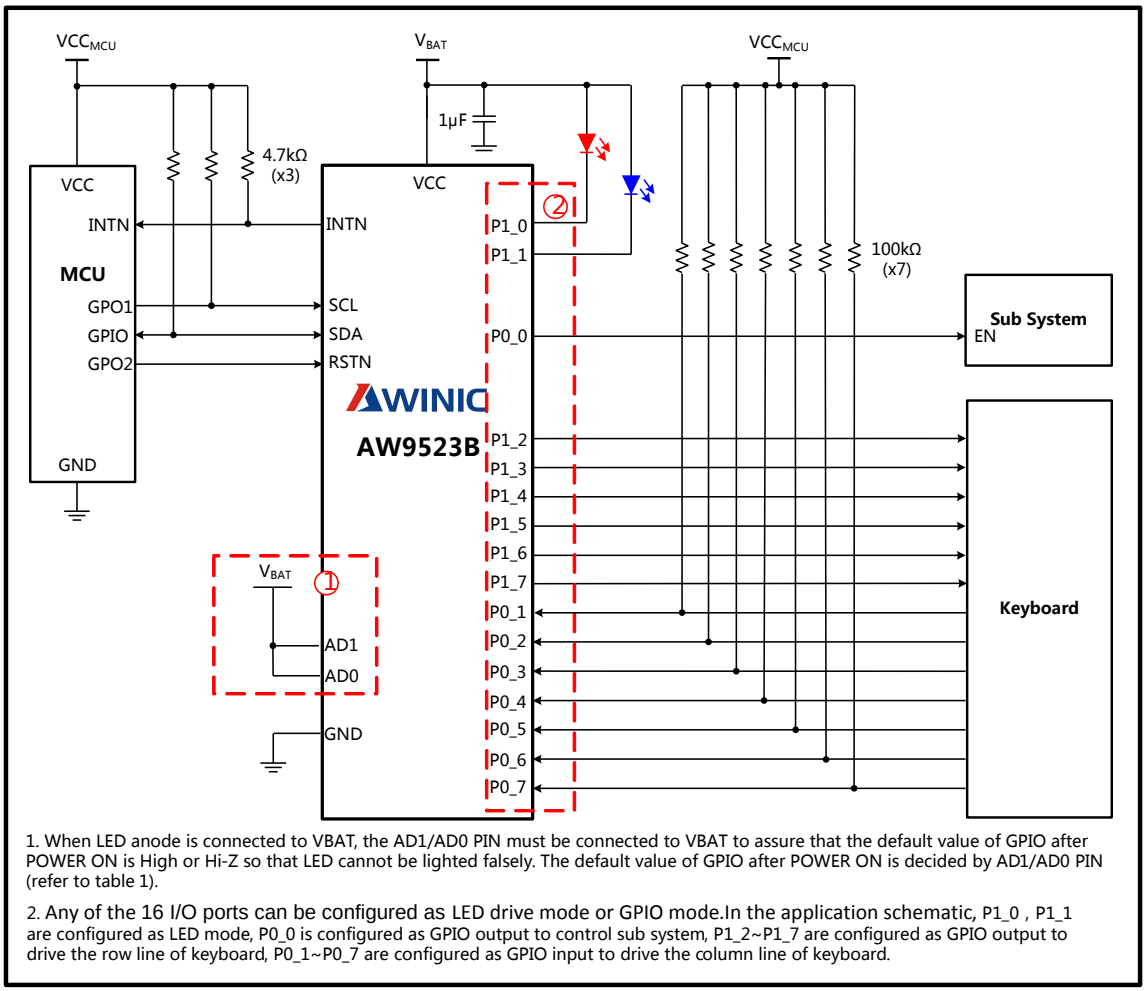
Typical Application 1: Drive 16 function LED, including 6 ports feasible for LED backlight



1. When LED anode is connected to VBAT, the AD1/AD0 PIN must be connected to VBAT to assure that the default value of GPIO after POWER ON is High or Hi-Z so that LED cannot be lighted falsely. The default value of GPIO after POWER ON is decided by AD1/AD0 PIN (refer to table 1).

2. The Dropout performance of the low 6 LED Ports (P1_0~P1_3, P0_0~P0_1) is optimized, so these ports are recommended if you want to use AW9523B to drive LED backlight.

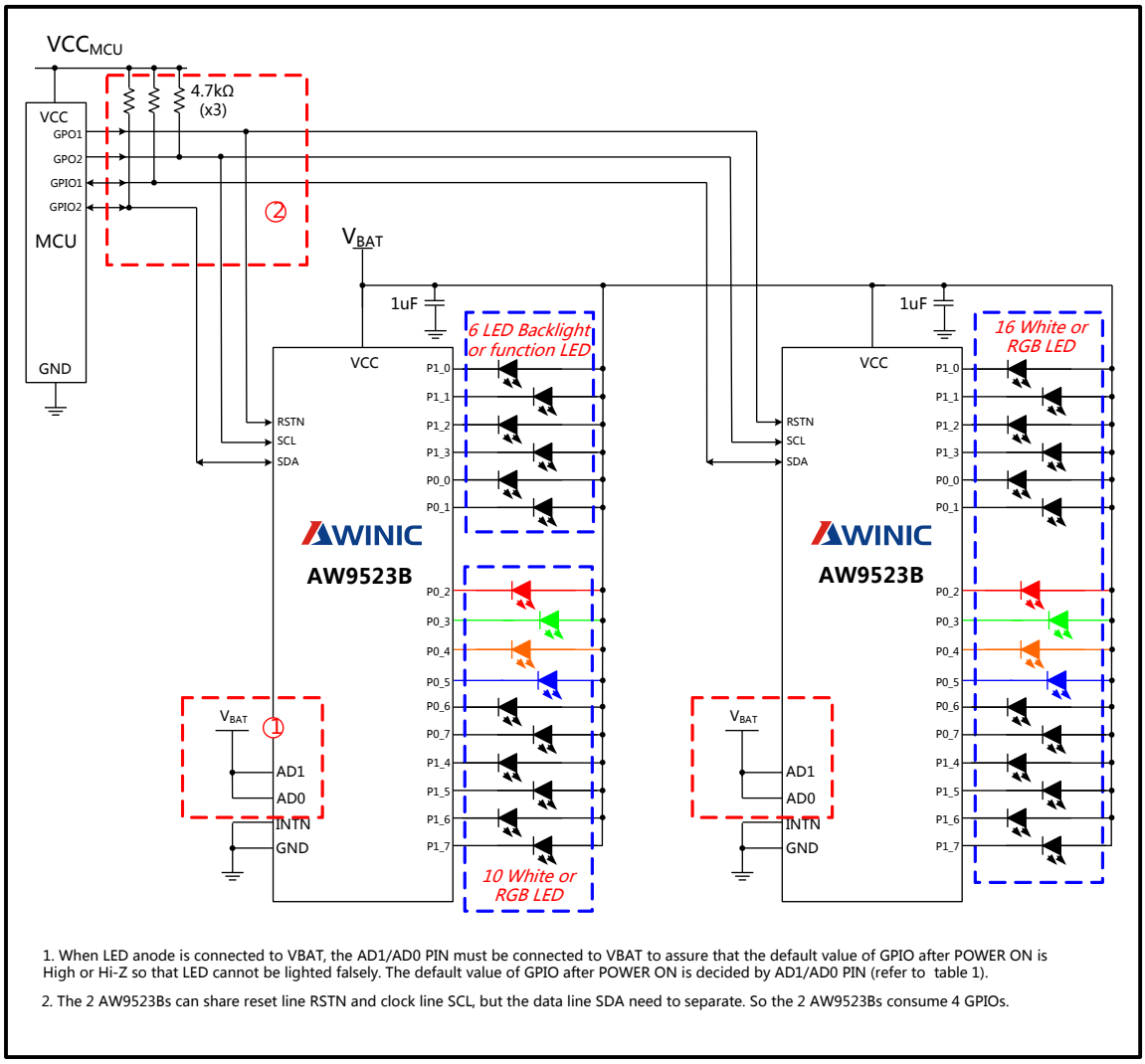
Typical Application 2: function LED + keyboard/IO Extended



1. When LED anode is connected to VBAT, the AD1/AD0 PIN must be connected to VBAT to assure that the default value of GPIO after POWER ON is High or Hi-Z so that LED cannot be lighted falsely. The default value of GPIO after POWER ON is decided by AD1/AD0 PIN (refer to table 1).

2. Any of the 16 I/O ports can be configured as LED drive mode or GPIO mode.In the application schematic, P1_0 , P1_1 are configured as LED mode, P0_0 is configured as GPIO output to control sub system, P1_2~P1_7 are configured as GPIO output to drive the row line of keyboard, P0_1~P0_7 are configured as GPIO input to drive the column line of keyboard.

Typical Application 3: 2 AW9523Bs drive 32 LEDs

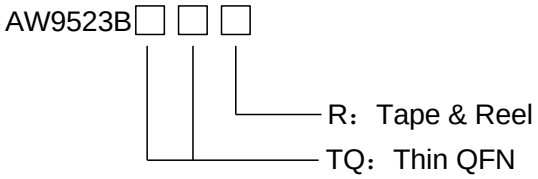


1. When LED anode is connected to VBAT, the AD1/AD0 PIN must be connected to VBAT to assure that the default value of GPIO after POWER ON is High or Hi-Z so that LED cannot be lighted falsely. The default value of GPIO after POWER ON is decided by AD1/AD0 PIN (refer to table 1).

2. The 2 AW9523Bs can share reset line RSTN and clock line SCL, but the data line SDA need to separate. So the 2 AW9523Bs consume 4 GPIOs.

ORDER INFORMATION

Part Number	Temperature	Package	Mark	SPQ
AW9523BTQR	-40℃～85℃	TQFN4X4-24L	AW9523B	Tape and Reel 6000/Tape



ABSOLUTE MAXIMUM RATINGS (Note1)

Parameter	Range
Supply voltage, VCC	-0.3V to 6 V
SCL，SDA，AD0，AD1，INTN，RSTN，P0_0~P0_7，P1_0~P1_7	-0.3V to VCC
Max power（PDmax，package@ TA=25℃）	3.2 W
Package thermal impedance, θ_{JA}	31℃/W
Max junction temperature, T_{Jmax}	125℃
Storage temperature range	-65℃ to 150℃
Solder temperature (10s)	260℃
ESD range (Note2)	
HBM	±4000V
Latch-up	
Standard ： JEDEC STANDARD NO.78C SEPTEMBER 2010	+IT：＋450mA -IT：-450mA

Note1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Note2: HBM standard: MIL-STD-883H Method 3015.8.

ELECTRICAL CHARACTERISTICS

T_A=25℃，VCC=3.8V (unless otherwise noted)

Parameter		Test Condition	Min.	Typ.	Max.	Unit
Supply voltage and current						
VCC	Supply voltage		2.5		5.5	V
$I_{shutdown}$	Shutdown current	SHDN=GND		0.1		μA
LED Drive						
I_{MAX}	Max current of LED drive	Configure DIMx Reg. as FFH		37		mA
V_{drop1}	Dropout voltage on low 6 ports（P1-0~P1_3，P0_0~P0_1）	I_{OUT}=20mA		60		mV
V_{drop2}	Dropout voltage on high 10 ports（P0-2~P0_7，P1_4~P1_7）	I_{OUT}=20mA		80		mV
Digital pin output						
V_{OH}	High-level output voltage（P0_7~P0_0，P1_7~P1_0）	VCC=2.5V，I_{SOURCE}=10mA		VCC-170		mV
		VCC=3.6V，I_{SOURCE}=20mA		VCC-250		mV
		VCC=5V，I_{SOURCE}=20mA		VCC-200		mV
V_{OL}	Low-level output voltage（P0_7~P0_0，P1_7~P1_0）	VCC=2.5V，I_{SINK}=20mA		90		mV
		VCC=3.6V，I_{SINK}=20mA		70		mV
		VCC=5V，I_{SINK}=20mA		60		mV
V_{OL}	Low-level output voltage（SDA,INTN）	VCC=2.5V，I_{SINK}=6mA		150		mV
		VCC=3.6V，I_{SINK}=6mA		100		mV
		VCC=5V，I_{SINK}=6mA		75		mV
Digital pin input						
V_{IH}	High-level input voltage（SCL，SDA，RSTN，AD0，AD1，P0_7~P0_0，P1_7~P1_0）		1.4			V
V_{IL}	Low-level input voltage（SCL，SDA，RSTN，AD0，AD1，P0_7~P0_0，P1_7~P1_0）				0.4	V
I_{IH}，I_{IL}	Input current（SCL，SDA，AD0，AD1，P0_7~P0_0，P1_7~P1_0）	V_I=VCC or GND	-0.2		+0.2	μA
$R_{\_RSTN}$	internal pull-low resistor in RSTN PIN			100k		Ω
C_I	Input capacitance（SCL，SDA，RSTN，AD0，AD1，P0_7~P0_0，P1_7~P1_0）	V_I=VCC or GND		3		pF
t_{SP_RSTN}	Pulse width that RSTN PIN can filter	RSTN=VCC		10		μs

I²C INTERFACE TIMING REQUIREMENTS

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL I²C clock frequency	f_{SCL}			400	kHz
I²C Start or repeated Start condition hold time	$t_{HD:STA}$	0.6			μS
SCL I²C clock low time	t_{LOW}	1.3			μS
SCL I²C clock high time	t_{HIGH}	0.6			μS
I²C Start or repeated Start condition setup time	$t_{SU:STA}$	0.6			μS
I²C serial-data hold time	$t_{HD:DAT}$	0			μS
I²C serial-data setup time	$t_{SU:DAT}$	0.1			μS
I²C rise time	t_R			0.3	μS
I²C fall time	t_F			0.3	μS
I²C Stop condition setup time	$t_{SU:STO}$	0.6			μS
I²C spike time	t_{BUF}	1.3			
Valid-data time	t_{SP}	0	140	240	nS
I²C bus capacitive load	C_b			400	pF

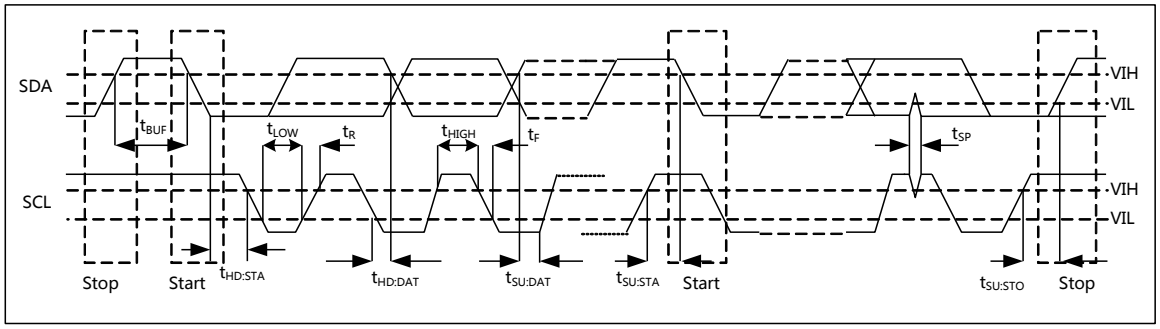


Figure 2 I²C Interface Timing

TYPICAL CHARACTERISTIC CURVES

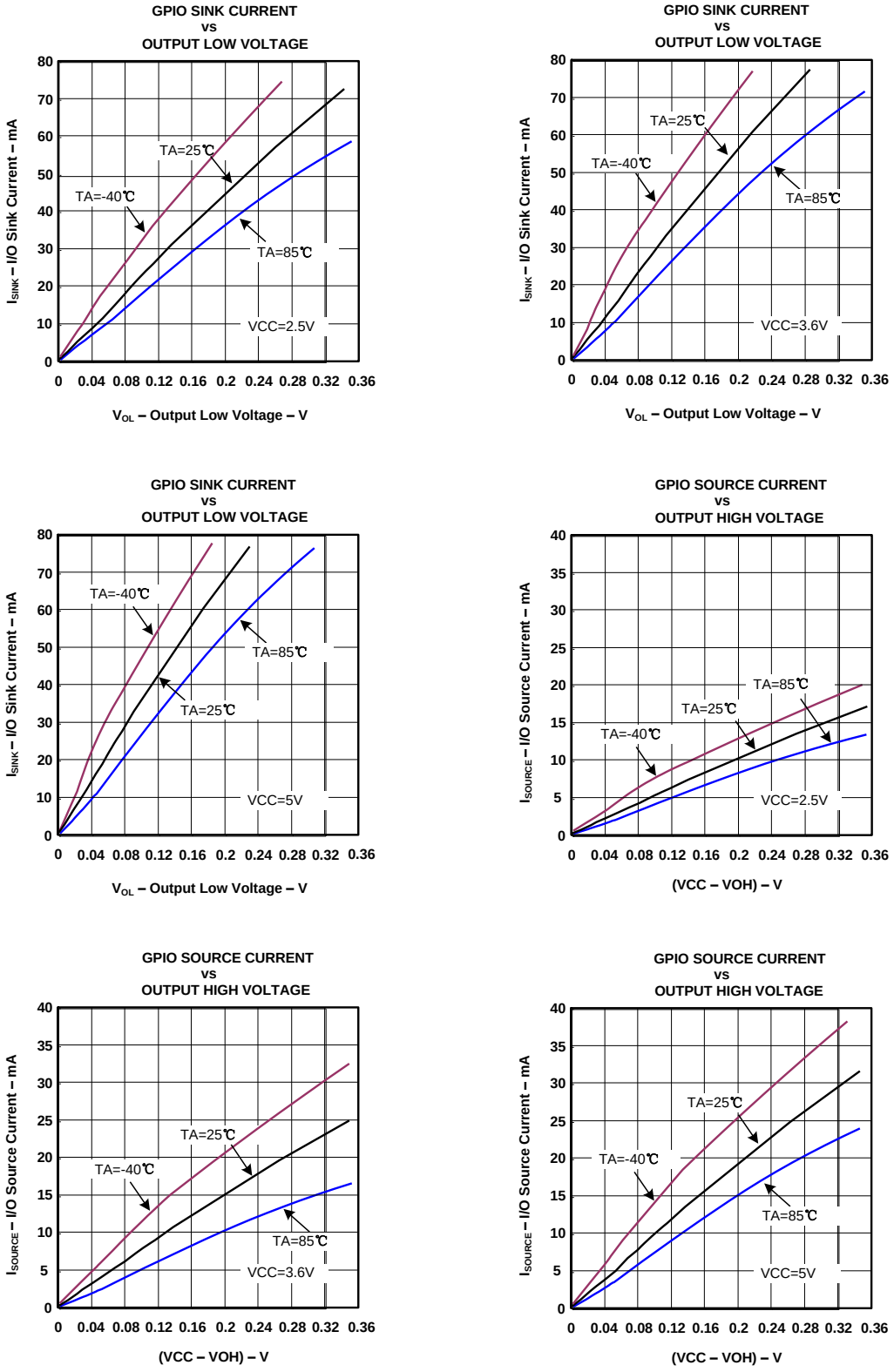


Figure 3 TYPICAL CHARACTERISTIC CURVES

PIN DEFINATION

Pin No.	Name	Description
1	P1_0	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
2	P1_1	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
3	P1_2	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
4	P1_3	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
5	P0_0	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
6	P0_1	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
7	P0_2	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
8	P0_3	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
9	GND	Ground supply
10	P0_4	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
11	P0_5	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
12	P0_6	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
13	P0_7	GPIO mode default, input or output, open-drain (default) or push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
14	P1_4	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
15	P1_5	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
16	P1_6	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
17	P1_7	GPIO mode default, input or output, push-pull mode. Can be configured as LED drive mode. The default state after power on is related to AD1/AD0 PIN.
18	AD0	I^2C interface device address，connect to VBAT or GND，and control the default state of output pin (refer to table 1).
19	SCL	I^2C interface clock bus
20	SDA	I^2C interface data bus
21	VCC	Power supply
22	INTN	Interrupt output pin, open-drain mode, need external pull-up resistor; interrupt low active.
23	RSTN	Hardware reset pin, low reset; it has an internal 100 kΩ(typical) pull-low resistor.
24	AD1	I^2C interface device address，connect to VBAT or GND，and control the default state of output pin (refer to table 1).
25	GND	Ground supply

SYSTEM BLOCK

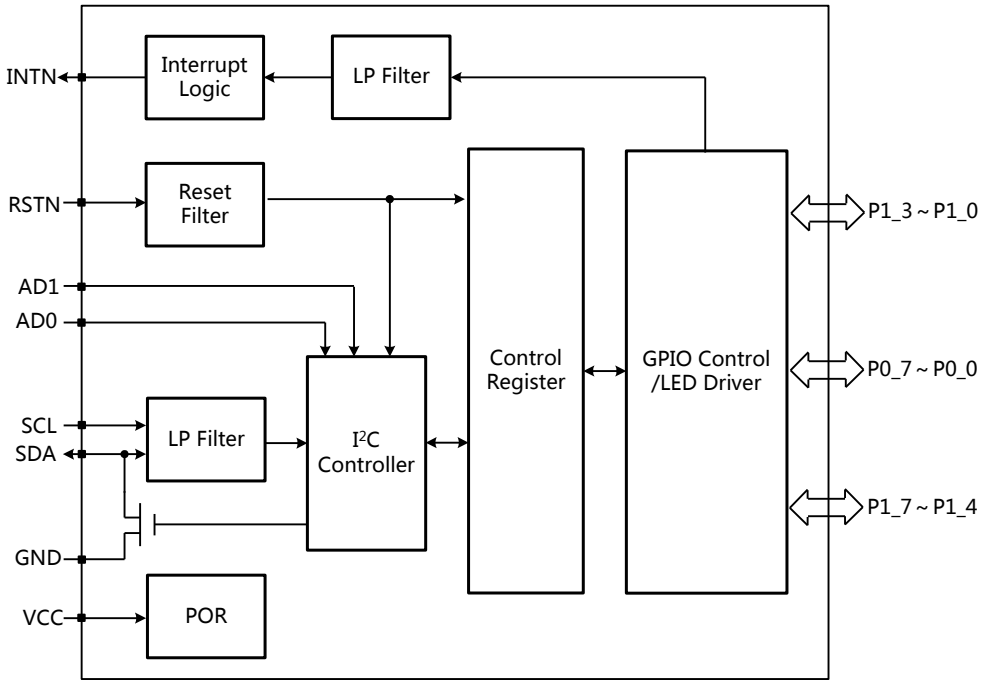


Figure 4 AW9523B system block

FUNCTION DESCRIPTION

AW9523B is a 16 multi-function IO controller, which is applied for LED drive or GPIO. Any of the 16 I/O ports can be configured as LED drive mode or GPIO mode. Furthermore, any GPIO can be configured as an input or an output independently.

When configured as GPIO mode, all I/O ports configured as inputs are continuously monitored for state changes. State changes are indicated by the INTN output. When AW9523B read GPIO state through the I^2C interface, the interrupt is cleared.

When configured as LED drive, drive current range is 0 ~IMAX, which 256 steps is divided. Default IMAX is 37mA, and it can be changed in GCR register.

GPIO OUTPUT

After power on, all the 16 I/O ports are configured as GPIO output as default, which default states are set according to the I^2C slave address selection inputs, AD0 and AD1, refer to table 1 for detail. The P1 port is Push-Pull mode; P0 port is Open-Drain mode (default) and can be configured as Push-Pull mode. When P0 port is Open-Drain mode, it need pull-up resistor.

Table 1. Default state of IO ports , AD1/AD0 and P0_x/P1_x

AD1	AD0	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0
GND	GND	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GND	VBAT	0	0	0	0	1	1	1	1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
VBAT	GND	1	1	1	1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	0	0	0	0
VBAT	VBAT	1	1	1	1	1	1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

GPIO INPUT/OUTPUT DIRECTION SELECT

The register Config_Port0 and Config_Port1 can configure a port as input or output. Each bit of the register is corresponding to each port, the bit set '1' as input, '0' as output. The default value is '0' as output.

GPIO INPUT

User can get the current state of GPIO through reading the register Input_Port0 and Input_Port1 by I^2C Interface. AW9523B GPIO support 1.8V logic input.

INTERRUPUT

AW9523B can monitor IO state to generate interrupt when configure port as GPI and GPIO interrupt enabled. External MCU is required acknowledge by INTN pin. INTN is open-drain output, low-level active, and need external pull-up resistor.

When AW9523B detect port change, any input state from high-level to low-level or from low-level to high-level will generate interrupt after 8us internal deglitch. External MCU read GPIO_INPUT_A/B register to clear interrupt. P1 port state change must clear interrupt by read GPIO_INPUT_B register; P0 port state change must clear interrupt by read GPIO_INPUT_A register.

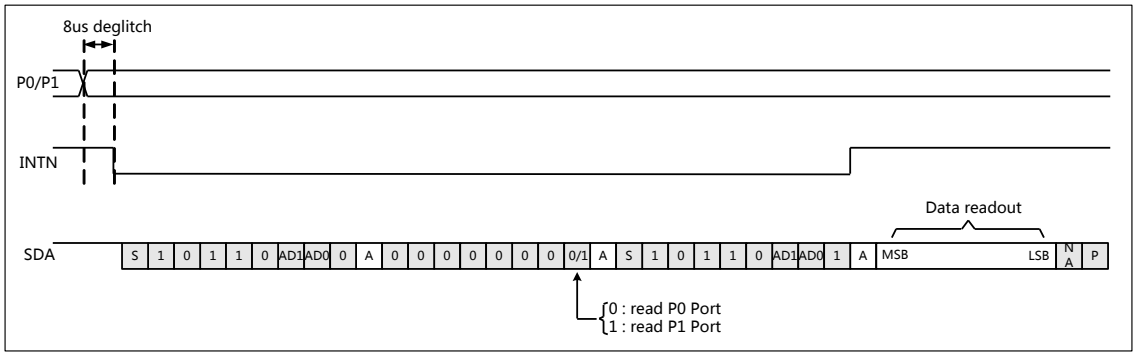


Figure 5 Interrupt generation and clear

LED DRIVE

AW9523B is co-anode current source LED drive. LED drive IMAX is configured by GCR (ISEL) register, to select 4 grades. The default IMAX is 37mA.

In LED drive mode, LED dim step can be manually controlled by external MCU. Drive current is from 0~IMAX divided by 256 steps.

Table-2. 256 step dimming

DIMx bit								D
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	$1/255 \times I_{MAX}$
0	0	0	0	0	0	1	0	$2/255 \times I_{MAX}$

.....								.....
1	1	1	1	1	1	0	1	253/255×I_{MAX}
1	1	1	1	1	1	1	0	254/255×I_{MAX}
1	1	1	1	1	1	1	1	255/255×I_{MAX}

I²C INTERFACE

AW9523B support I²C interface. The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high. After the Start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address.

After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (AD1/AD0) of the slave device must not be changed between the Start and Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master.

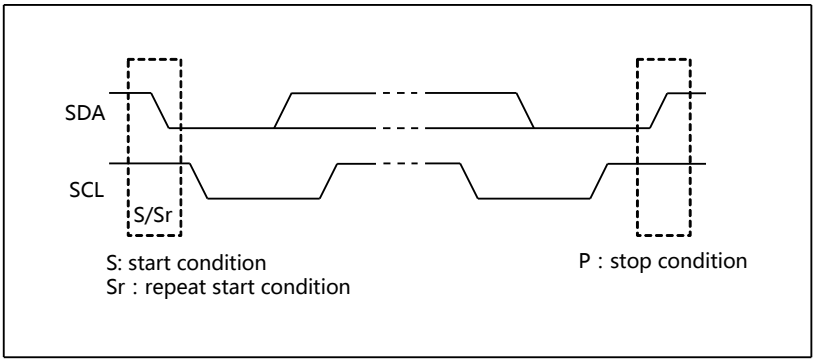


Figure 6 Start and stop condition

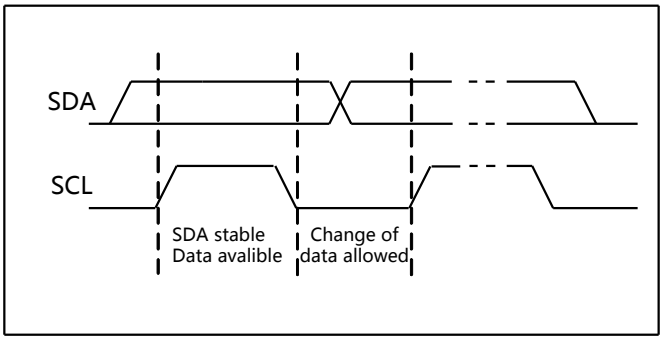


Figure 7 Bit Transfer

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

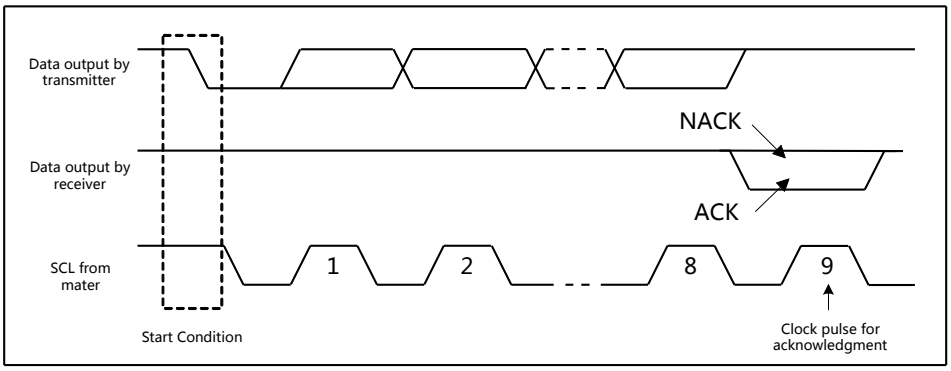


Figure 8 Acknowledgment On I^2C Bus

DEVICE ADDRESS

Below is the device address of AW9523B. AD1/AD0 bit in device address match with AD1/AD0 pin respectively.

1	0	1	1	0	AD1	AD0	R/$\overline{W}$

AD1/AD0 value match with AW9523B pin AD1/AD0 respectively

Figure 9 AW9523B Device Address

WRITE

Data is transmitted to the AW9523B by sending the device address and setting the least-significant bit to a logic 0. The register address byte is sent after the device address and determines which register receives the data that follows the command byte.

After sending data to one register, the next data byte is sent to the other register. There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

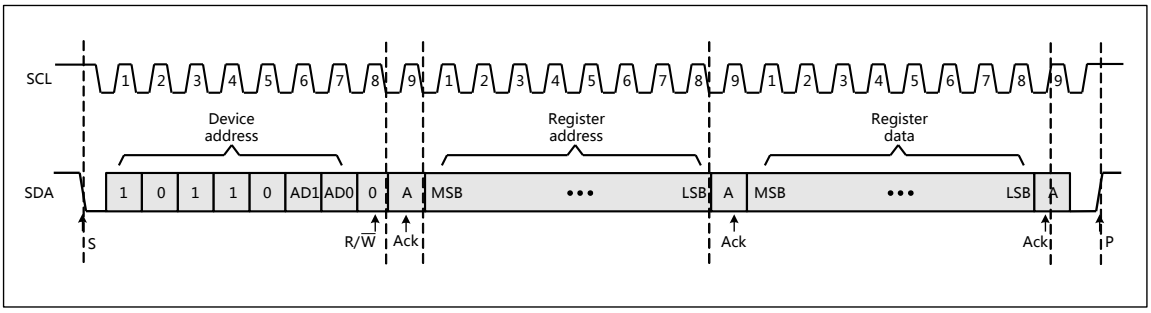


Figure 10 AW9523B Write Operation

READ

The bus master first must send the AW9523B address with the least-significant bit set to a logic 0. The register address byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again, but this time, the least-significant bit is set to a logic 1. Data from the register defined by the register address byte then is sent by the AW9523B.

After a restart, the value of the register defined by the register address byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

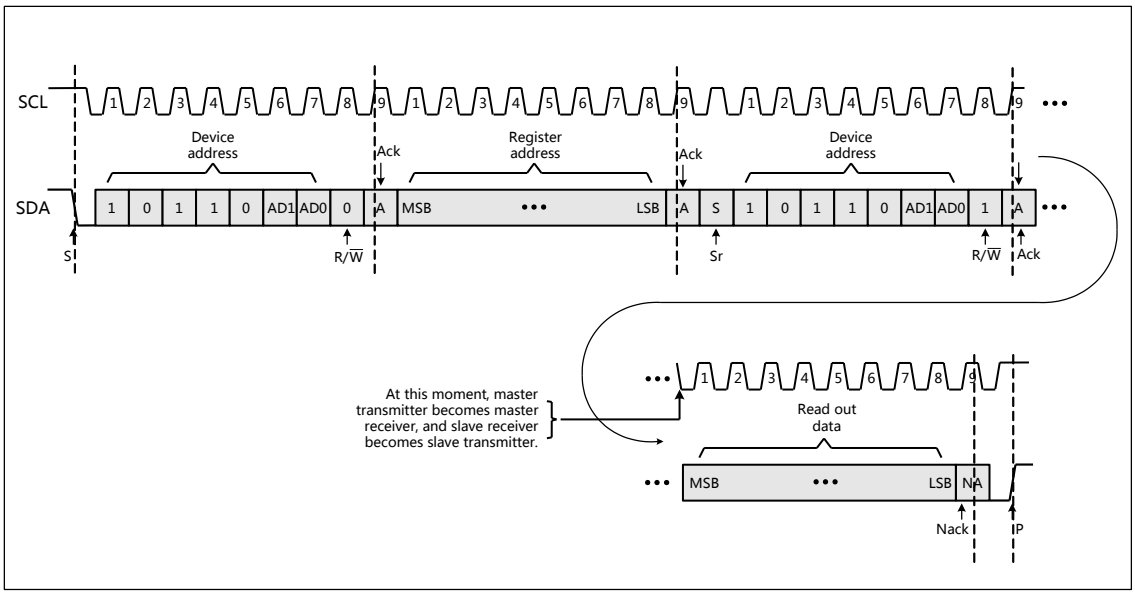


Figure 11 AW9523B Read Operation

RESET FUNCTION

AW9523B support 3 reset mode: power on reset, hardware reset, software reset. Each reset mode can reset registers to default value.

Hardware Reset

Hardware reset timing is as the following figure.

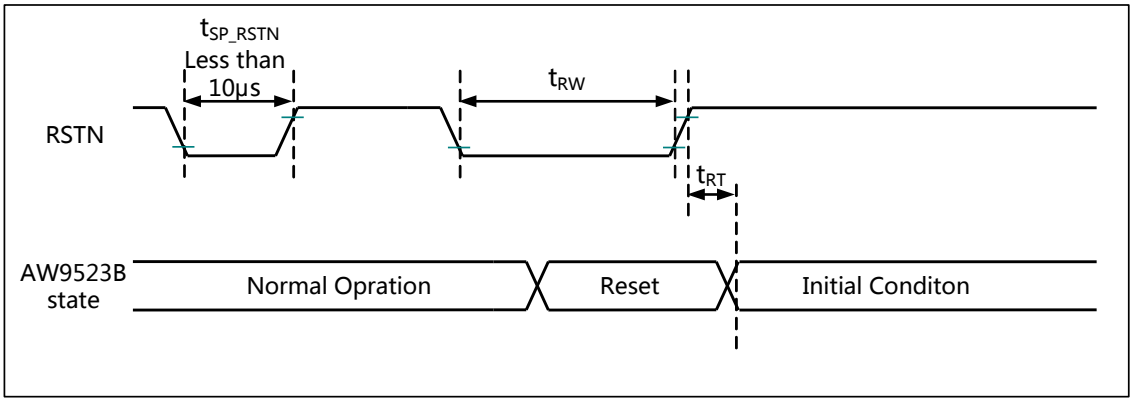


Figure 12 Hardware Reset Timing

Table 3. Hardware Reset Parameter

Parameter		**Condition**	**min**	**typ**	**max**	**unit**
t_{RW}	Reset pulse low level width	VSS=0V，VCC=2.4V~5.5V，T=-40℃~85℃	20			μs
t_{RT}	Reset recovery time		1			μs

Note:

1. The hardware reset PIN（RSTN）has a built-in deglitch block。Spike due to an electrostatic discharge on RSTN line does not cause irregular system reset according to the table below：

Reset pulse（RSTN）	AW9523B action
Shorter than 10μs（typical）	Reset Rejected
Longer than 20μs	Reset

2. After reset, AW9523B is in default state. All GPIO are configured as output, which value is decided by 2 device address (AD1/AD0) (refer to table 1). The interrupt (INTN) is cleared and pulled up by external pull-up resistor.
3. Spike Rejection also applies during a valid reset pulse as shown below:

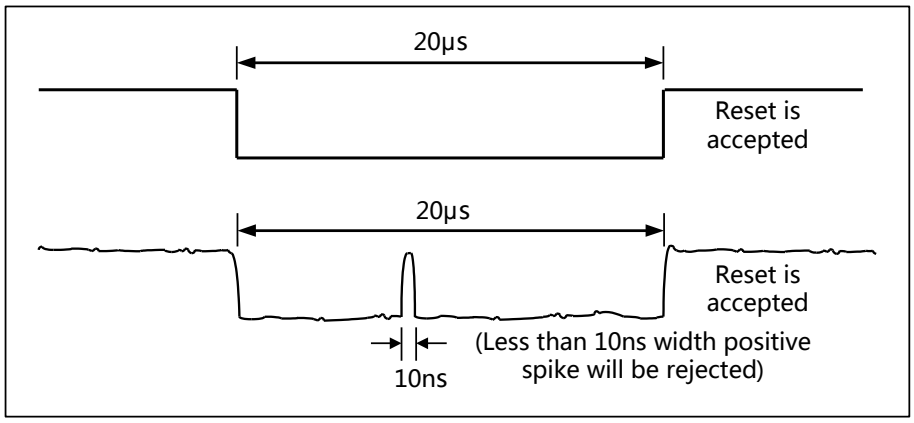


Figure 13 Operation When RSTN SLOW

Software Reset

AW9523B support software reset mode. Writing 00H to the software register(7FH) will generate a reset pulse. After software reset, AW9523B is in default state, which is the same as hardware reset. The software reset timing is as below.

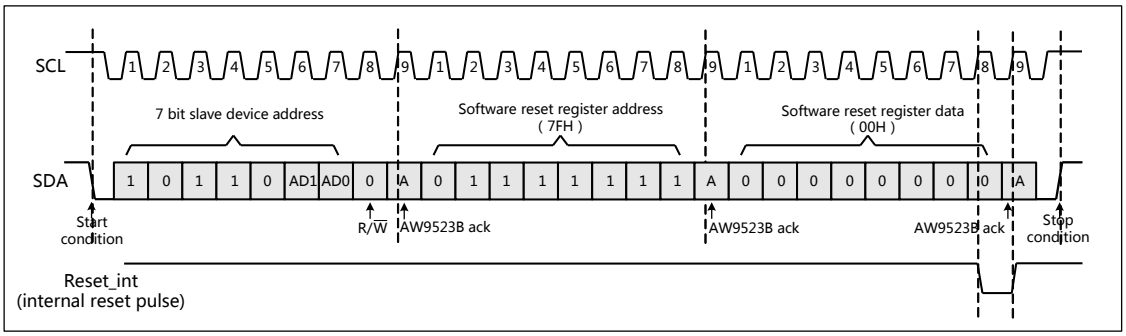


Figure 14 Software Reset Timing

REGISTERS

Table-4. AW9523B register list

Address	W/R	Default Value	Function	Description
00H	R	Equal to P0	Input_Port0	P0 port input state
01H	R	Equal to P1	Input_Port1	P1 port input state
02H	W/R	Refer to table 1	Output_Port0	P0 port output state
03H	W/R	Refer to table 1	Output_Port1	P1 port output state
04H	W/R	00H	Config_Port0	P0 port direction configure
05H	W/R	00H	Config_Port1	P1 port direction configure
06H	W/R	00H	Int_Port0	P0 port interrupt enable
07H	W/R	00H	Int_Port1	P1 port interrupt enable
10H	R	23H	ID	ID register (read only)
11H	W/R	00H	CTL	Global control register
12H	W/R	FFH	LED Mode Switch	P0 port mode configure
13H	W/R	FFH	LED Mode Switch	P1 port mode configure
20H	W	00H	DIM0	P1_0 LED current control
21H	W	00H	DIM1	P1_1 LED current control
22H	W	00H	DIM2	P1_2 LED current control
23H	W	00H	DIM3	P1_3 LED current control
24H	W	00H	DIM4	P0_0 LED current control
25H	W	00H	DIM5	P0_1 LED current control
26H	W	00H	DIM6	P0_2 LED current control
27H	W	00H	DIM7	P0_3 LED current control
28H	W	00H	DIM8	P0_4 LED current control
29H	W	00H	DIM9	P0_5 LED current control
2AH	W	00H	DIM10	P0_6 LED current control
2BH	W	00H	DIM11	P0_7 LED current control
2CH	W	00H	DIM12	P1_4 LED current control
2DH	W	00H	DIM13	P1_5 LED current control
2EH	W	00H	DIM14	P1_6 LED current control
2FH	W	00H	DIM15	P1_7 LED current control
7FH	W	00H	SW_RSTN	Soft reset
Other	-	-	-	Reserved

REGISTER DETAIL DESCRIPTION

Table 5. Input state register（00H，01H）

Address	Name	Description	Default
00H	Input_Port0	P0 port current logic state, 0-low level；1-high level	X
01H	Input_Port1	P1 port current logic state, 0-low level；1-high level	X

The Input state registers (00H,01H) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration Register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to let the I^2C device know that the Input Port registers will be accessed next.

Table 6. Output state register（02H，03H）

Address	Name	Description	Default
02H	Output_Port0	Set P0 port output value. 0-low level; 1-high level	Refer to table1
03H	Output_Port1	Set P1 port output value. 0-low level; 1-high level	Refer to table1

The Output state register（02H，03H）show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 7. Configuration register（04H，05H）

Address	Name	Description	Default
04H	Config_Port0	P0 port input/output mode select. 0-output; 1-input	00H
05H	Config_Port1	P1 port input/output mode select. 0-output; 1-input	00H

The Configuration registers (04H，05H) configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 8. Interrupt enable register（06H，07H）

Address	Name	Description	Default
06H	Int_Port0	P0 port interrupt enable. 0-enable; 1-disable	00H
07H	Int_Port1	P1 port interrupt enable. 0-enable; 1-disable	00H

The Interrupt enable register (06H，07H) are used to configure the interrupt enable or disable of GPIO. If a bit in this register is set to 1, the interrupt function of the corresponding port pin is disabled. If a bit in this register is cleared to 0, the interrupt function of corresponding port pin is enabled.

Table 9. ID register（10H）

Address	Name	Description	Default
10H	ID	ID register, read only, the readout value is 23H	23H

ID register（10H）is a read only register which stores the device ID。The ID read value of AW9523B is 23H.

Table 10. GCR ,Global control register（11H）

Address	Name	Description	Default
D[7:5]	reserved	-	-
D[4]	GPOMD	Set P0 port GPIO output drive mode。if D[4]=0, P0 port is Open-Drain mode; if D[4]=1, P0 port is Push-Pull mode.	0
D[3:2]	reserved	-	-
D[1:0]	ISEL	256 step dimming range select 00：0~I_{MAX} 01：0~(I_{MAX}×3/4) 10：0~(I_{MAX}×2/4) 11：0~(I_{MAX}×1/4)	00

D[4] is used to configure P0 port output drive as Open-Drain or Push-Pull mode。When P0 port use as output with Open-Drain mode, it needs pull-up resistor. If in Push-pull mode, it needs no pull-up resistor.

D[1:0] is used to configure the max drive current of LED。AW9523B set max current I_{MAX} to 37mA(typical) default, and through register ISEL[1:0] can set to I_{MAX}×1/4,I_{MAX}×2/4, I_{MAX}×3/4,I_{MAX},so the 256 step dimming range changes.

Except D4, D[1:0], other bits (D[7:5]\D[3:2]) are used for test purpose and the default value is 0. If user needs to configure register 11H, then the bits D[7:5]\D[3:2] must configure to 0, or system function error may occur.

Table 11. LED mode switch register（12H）

Address	Name	Description	Default
12H	LED Mode Switch	Configure P0_7~P0_0 as LED or GPIO mode。 1：GPIO mode 0：LED mode	FFH

LED mode switch register（12H）can configure P0 port as LED or GPIO mode. After reset, it is GPIO mode as default. Set a bit of 12H[7:0] to 0 so the corresponding port is LED mode, and set to 1 so the corresponding port is GPIO mode.

Table 12. LED mode switch register（13H）

Address	Name	Description	Default
13H	LED Mode Switch	Configure P1_7~P1_0 as LED or GPIO mode。 1：GPIO mode 0：LED mode	FFH

LED mode switch register（13H）can configure P1 port as LED or GPIO mode. After reset, it is GPIO mode as default. Set a bit of 13H[7:0] to 0 so the corresponding port is LED mode, and set to 1 so the corresponding port is GPIO mode.

Table 13. 256 step dimming control register (20H~2FH)

Address	Name	Description	Default
20H	DIM0	P1_0 port LED current control	00H
21H	DIM1	P1_1 port LED current control	00H
22H	DIM2	P1_2 port LED current control	00H
23H	DIM3	P1_3 port LED current control	00H
24H	DIM4	P0_0 port LED current control	00H
25H	DIM5	P0_1 port LED current control	00H
26H	DIM6	P0_2 port LED current control	00H
27H	DIM7	P0_3 port LED current control	00H
28H	DIM8	P0_4 port LED current control	00H
29H	DIM9	P0_5 port LED current control	00H
2AH	DIM10	P0_6 port LED current control	00H
2BH	DIM11	P0_7 port LED current control	00H
2CH	DIM12	P1_4 port LED current control	00H
2DH	DIM13	P1_5 port LED current control	00H
2EH	DIM14	P1_6 port LED current control	00H
2FH	DIM15	P1_7 port LED current control	00H

The dimming control register (20H~2FH) are used to configure P0 port and P1 port LED current. Each port supports 256 step dimming. For the detailed configuration, refer to table 2.

Table 13.Soft reset register（7FH）

Address	Name	Description	Default
7FH	Software Reset	Write 00H to generate a reset pulse	X

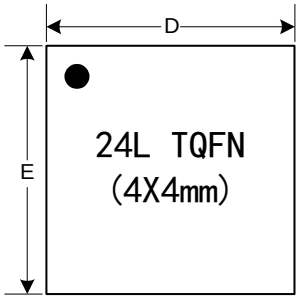
The soft reset register (7FH) support software reset function, which brings convenience to software engineer. Every time write 00H to this register, it generate a reset pulse. The software reset timing, please refer to figure 14.

Table 14. Reserve register

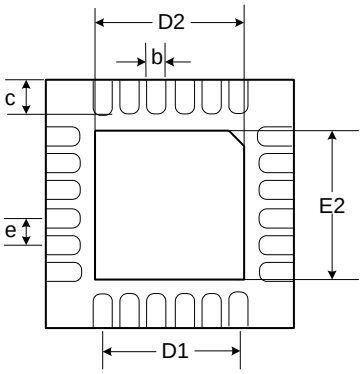
Address	Name	Descrip-tion
08H~0FH 14H~1FH 30H~7EH 80H~FFH	Reserve register, for test purpose or not defined.	X

Reserve register（08H~10H，14H~1FH，30H~7EH，80H~FFH）are for test purpose or not defined, user should not write these registers, or may cause function error.

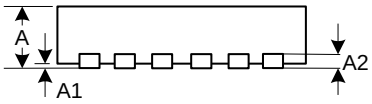
PACKAGE DESCRIPTION



Top View



Bottom View



Side View

Unit:mm	TQFN-24L		
Symbol	Min	Typ	Max
A	0.700	0.750	0.800
A1	0.000		0.050
A2	0.203 (Ref.)		
b	0.200	0.250	0.300
c	0.350	0.400	0.450
D	3.950	4.000	4.050
D1	2.500(Ref.)		
D2	2.650	2.700	2.750
e	0.500(BSC)		
E	3.950	4.000	4.050
E2	2.650	2.700	2.750