

# LV23000M



## Single-Chip Tuner IC for Radio/Cassette Players



### Overview

The LV23000M is a single-chip tuner IC for radio/cassette players that provides FM, AM, MPX, and PLL circuits. It allows the tuner PCB to be simplified significantly.

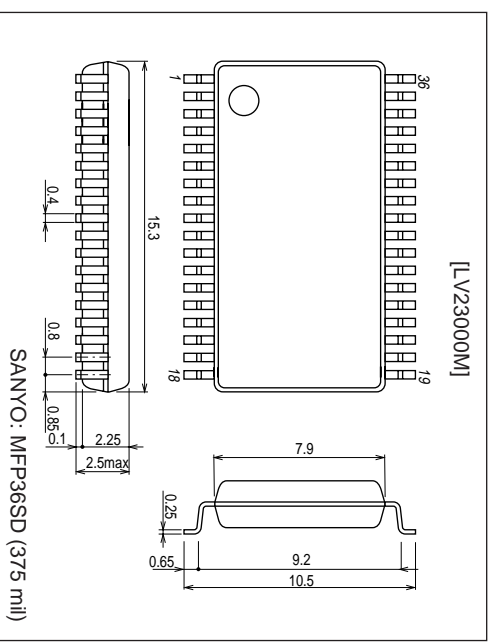
### Package Dimensions

unit: mm

**3129-MFP36SD**

- ### Functions
- AM tuner
  - FM tuner
  - Multiplex stereo decoder
  - PLL frequency synthesizer

- ### Features
- Tuner circuit includes built-in PLL for easy end product design.
  - Supports FCC standards
  - Built-in adjustment-free multiplex VCO
  - AM low-cut control
  - Provides the transistor required to implement an active low-pass filter.



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## LV23000M

### Specifications

#### Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings		Unit
			min	typ	
Maximum supply voltage	V <sub>CC</sub> max	V <sub>CC</sub>			7.0
	V <sub>DD</sub> max	V <sub>DD</sub>			7.0
Maximum input voltage	V <sub>I/N1</sub> max	CE, DI, CL			7.0
	V <sub>I/N2</sub> max	XIN			V <sub>DD</sub> + 0.3
Allowable power dissipation	P <sub>DMAX</sub>	Ta ≤ 70°C*			400
	V <sub>O1</sub> max	DO			7.0
Maximum output voltage	V <sub>O2</sub> max	XOUT, PD			V <sub>DD</sub> + 0.3
	V <sub>O3</sub> max	BO1, BO2, AOUT			12.0
					-20 to +70
Operating temperature	T <sub>opr</sub>				-20 to +70
Storage temperature	T <sub>stg</sub>				-40 to +125

Note: \* When mounted on a 114.3 × 76.1 × 1.6 mm glass epoxy printed circuit board.

#### Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings		Unit
			min	typ	
Recommended supply voltage	V <sub>CC</sub>				5.0
	V <sub>DD</sub>				3.0
Operating supply voltage range	V <sub>CC</sub> op				4.0 to 6.0
	V <sub>DD</sub> op				2.5 to 3.6

#### PLL Block Allowable Operating Ranges at Ta = -20 to +70°C, V<sub>SS</sub> = 0 V

Parameter	Symbol	Conditions	Ratings			Unit	
			min	typ	max		
Supply voltage	V <sub>DD</sub>	CE, CL, DI	2.5		3.6	V	
High-level input voltage	V <sub>IH</sub>	CE, CL, DI	0.7V <sub>DD</sub>		6.0	V	
Low-level input voltage	V <sub>IL</sub>	CE, CL, DI	0		0.3V <sub>DD</sub>	V	
		DO	0		6.0	V	
Output voltage	V <sub>O2</sub>	BO1, BO2, AOUT	0		10	V	
		XIN: V <sub>I/N1</sub>		75		KHz	
		FMIN: V <sub>I/N2</sub>		10		160	MHz
		AMIN (SNS = 1): V <sub>I/N3</sub>		2		40	MHz
Operating frequency	f <sub>N4</sub>	AMIN (SNS = 0): V <sub>I/N4</sub>	0.5		10	MHz	

Note: The XIN pin has an extremely high input impedance, which may result in current leakage problems.

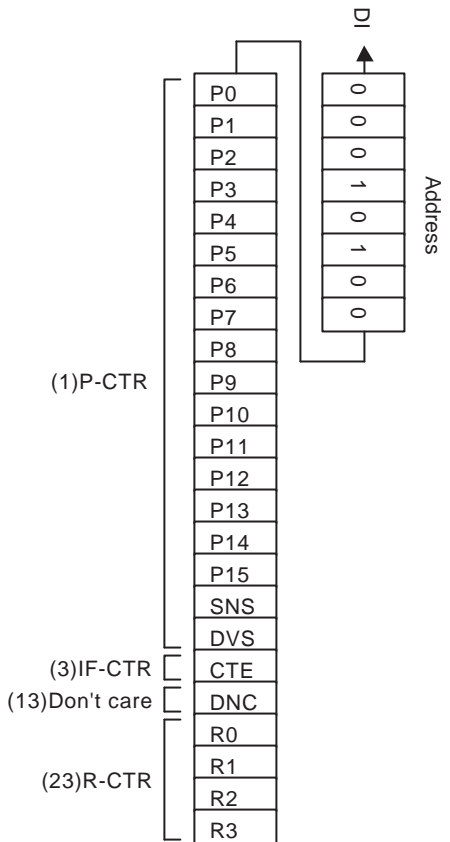
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**Operating Characteristics at Ta = 25°C, VCC = 5.0 V, VDD = 3.0 V,  
in the specified test circuit, using Yamaiichi Electronics socket IC51-0362-736**

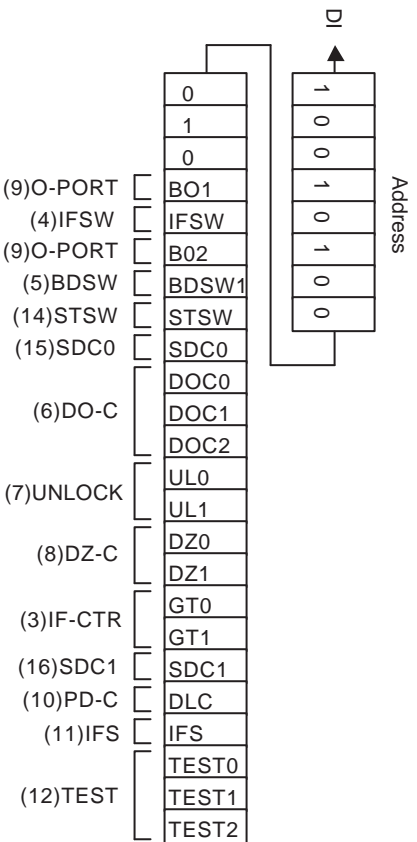
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[FM Front End Characteristics] : fc = 98 MHz, fm = 1 kHz, 22.5 kHzdev.						
3 dB sensitivity	3 dB LS	60 dBμV EMF, referenced to a 22.5 kHz dev. output, -3 dB input		12		dBμV EMF
Practical sensitivity	QS	For a 30 dB signal-to-noise ratio input		12		dBμV EMF
[FM IF Monaural Characteristics] : fc = 10.7 MHz, fm = 1 kHz, 75 kHzdev.						
Demodulator output	Vo	100 dBμ V, the pin 12 output	210	330	420	mVrms
Signal-to-noise ratio	S/N	100 dBμ V, the pin 12 output	68	75		dB
Total harmonic distortion (mono)	THD	100 dBμ V, the pin 12 output		0.3	1.5	%
3 dB sensitivity	3 dB LS	100 dBμ V, referenced to a 75 kHz dev. output, -3 dB input		38	44	dBμV
IF counter sensitivity	IF-C3	SDC0 = 1, SDC1 = 0, the pin 18 (DO) output		41	51	dBμV
Muting attenuation	Mute-Att	100 dBμ V, the pin 12 output		68		dB
[FM IF Stereo Characteristics] : fc = 10.7 MHz, fm = 1 kHz, L+R = 90%, Pilot = 10%						
Separation	SEP	100 dBμ V, L-mod, Pin 12 output/pin 13 output		28	40	dB
Total harmonic distortion (main)	THD	100 dBμ V, main modulation, the pin 12 output		0.5	1.5	%
[AM Characteristics] : fc = 1000 kHz, fm = 1 kHz, 30% mod						
Detector output 1	Vo1	23 dBμ V, the pin 12 output	20	40	80	mVrms
Detector output 2	Vo2	80 dBμ V, the pin 12 output	60	110	160	mVrms
Signal-to-noise ratio 1	S/N1	23 dBμ V, the pin 12 output		1.5	20	dB
Signal-to-noise ratio 2	S/N2	80 dBμ V, the pin 12 output		47	54	dB
Total harmonic distortion	THD	80 dBμ V, the pin 12 output		1.2	3.0	%
IF counter sensitivity	IF-C	The pin 18 (DO) output		16	26	dBμV
AM low cut	LOW-CUT	80 dBμ V, referenced to fm = 1 kHz, the pin 12 output when fm = 100 Hz.		5	8	dB
[Current Drain]						
FM tuner block	IcCFM	In FM mode with no input		20	30	mA
AM tuner block	IcCAM	In AM mode with no input		10	20	mA
PLL block	Ipd	fr = 83 MHz, X'ial = 75 kHz, With no input to the tuner block		1	2	mA
[PLL Characteristics]						
Built-in feedback resistor	Rf	XIN		8		MΩ
Built-in output resistor	Rd	XOUT		250		kΩ
Hysteresis	Vhis	CE, CL, DI		0.1VDD		V
High-level output voltage	VoH	PD: Io = -1 mA	VDD - 1.0			V
	Vo1	PD: Io = 1 mA			1.0	V
	Vo2	BO1, BO2: Io = 1 mA			0.25	V
	Vo2	BO1, BO2: Io = 5 mA			1.25	V
	Vo3	DO: Io = 1 mA			0.25	V
	Vo4	AOUT: Io = 1 mA, AIN = 2.0 V			0.5	V
High-level input current	Ih1	CE, CL, DI: Vi = 6.0 V			5.0	μA
	Ih2	XIN: Vi = VDD		0.16	0.9	μA
	Ih3	AIN: Vi = 6.0 V			200	nA
	Ih1	CE, CL, DI: Vi = 0 V			5.0	μA
Low-level input current	Ih2	XIN: Vi = 0 V		0.16	0.9	μA
	Ih3	AIN: Vi = 0 V			200	nA
Output leakage current	IoFF1	AOUT, BO1, BO2: Vo = 10 V			5.0	μA
	IoFF2	DO: Vo = 6.0 V			5.0	μA
High-level 3-state off leakage current	IoFHH	PD: Vo = 6.0 V		0.01	200	nA
Low-level 3-state off leakage current	IoFFL	PD: Vo = 0 V		0.01	200	nA

**Structure of the DI Control Data (Serial Input Data)**

(1) IN1 mode



(2) IN2 mode



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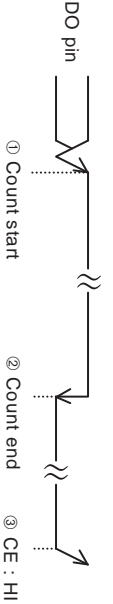
Description of the DI Control Data

No.	Control block/data	Description	Related data																																																																																					
(1)	P0 to P15 DVS, SNS Programmable divider data	<ul style="list-style-type: none"> <li>Specifies the divisor used by the programmable dividers. This is a binary value with P15 as the MSB. The LSB depends on DVS and SNS.</li> </ul> <table border="1" data-bbox="1736 494 1870 1252"> <thead> <tr> <th>DVS</th> <th>SNS</th> <th>LSB</th> <th>Divisor setting (N)</th> <th>Actual divisor</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>*</td> <td>P0</td> <td>272 to 65535</td> <td>The actual setting times 2</td> </tr> <tr> <td>0</td> <td>1</td> <td>P0</td> <td>272 to 65535</td> <td>The actual setting</td> </tr> <tr> <td>0</td> <td>0</td> <td>P4</td> <td>4 to 4095</td> <td>The actual setting</td> </tr> </tbody> </table> <p>Note: When P4 is the LSB, bits P0 to P3 are ignored.</p> <ul style="list-style-type: none"> <li>Selects the input signal (FMIN or AMIN) to the programmable divider and switches the input frequency range.</li> </ul> <table border="1" data-bbox="1496 494 1624 1252"> <thead> <tr> <th>DVS</th> <th>SNS</th> <th>Input</th> <th>Operating frequency range</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>*</td> <td>FMIN</td> <td>10 to 160 MHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>AMIN</td> <td>2 to 40 MHz</td> </tr> <tr> <td>0</td> <td>0</td> <td>AMIN</td> <td>0.5 to 10 MHz</td> </tr> </tbody> </table> <p>(* : don't care)</p>	DVS	SNS	LSB	Divisor setting (N)	Actual divisor	1	*	P0	272 to 65535	The actual setting times 2	0	1	P0	272 to 65535	The actual setting	0	0	P4	4 to 4095	The actual setting	DVS	SNS	Input	Operating frequency range	1	*	FMIN	10 to 160 MHz	0	1	AMIN	2 to 40 MHz	0	0	AMIN	0.5 to 10 MHz																																																		
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(2)	Reference divider data R0 to R3	<ul style="list-style-type: none"> <li>Data that selects the reference frequency (fref)</li> </ul> <table border="1" data-bbox="869 494 1411 1252"> <thead> <tr> <th>R3</th> <th>R2</th> <th>R1</th> <th>R0</th> <th>Reference frequency</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>25 kHz</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>25 kHz</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>25 kHz</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>25 kHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>12.5 kHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>6.25 kHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>3.125 kHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>3.125 kHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>5 kHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>5 kHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>5 kHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>1 kHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>3 kHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>15 kHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>PLL INHIBIT + X'ral OSC STOP</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>PLL INHIBIT</td> </tr> </tbody> </table> <p>Note: PLL INHIBIT</p> <ul style="list-style-type: none"> <li>In this state, the programmable divider block and the IF counter block are stopped, FMIN, AMIN, and IFIN are pulled down (to ground), and the charge pump goes to the high-impedance state.</li> </ul>	R3	R2	R1	R0	Reference frequency	0	0	0	0	25 kHz	0	0	0	1	25 kHz	0	0	1	0	25 kHz	0	0	1	1	25 kHz	0	1	0	0	12.5 kHz	0	1	0	1	6.25 kHz	0	1	1	0	3.125 kHz	0	1	1	1	3.125 kHz	1	0	0	0	5 kHz	1	0	0	1	5 kHz	1	0	1	0	5 kHz	1	0	1	1	1 kHz	1	1	0	0	3 kHz	1	1	0	1	15 kHz	1	1	1	0	PLL INHIBIT + X'ral OSC STOP	1	1	1	1	PLL INHIBIT	
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(3)	IF counter control data CTE GT0, GT1	<ul style="list-style-type: none"> <li>Measurement start data for the IF counter                      CTE = 1: Start the count.                      = 0: Reset the counter.</li> <li>Determines the measurement time for the general-purpose counter.</li> </ul> <table border="1" data-bbox="403 494 571 1252"> <thead> <tr> <th>GT0</th> <th>GT1</th> <th>Measurement time</th> <th>Wait time</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>4 ms</td> <td>3 to 4 ms</td> </tr> <tr> <td>0</td> <td>1</td> <td>8 ms</td> <td>3 to 4 ms</td> </tr> <tr> <td>1</td> <td>0</td> <td>16 ms</td> <td>3 to 4 ms</td> </tr> <tr> <td>1</td> <td>1</td> <td>32 ms</td> <td>3 to 4 ms</td> </tr> </tbody> </table>	GT0	GT1	Measurement time	Wait time	0	0	4 ms	3 to 4 ms	0	1	8 ms	3 to 4 ms	1	0	16 ms	3 to 4 ms	1	1	32 ms	3 to 4 ms	IFS																																																																	
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No.	Control block/data	Description	Related data																																				
(4)	Mute control data  IFSW	<ul style="list-style-type: none"> <li>Determines the output of the IFSW output port and controls the muting function. Data = 0: Receive mode = 1: Muted</li> </ul>																																					
(5)	FM/AM band switching control data  BDSW	<ul style="list-style-type: none"> <li>Determines the output of the BDSW output port and switches the reception band. Data = 0: AM = 1: FM</li> </ul>																																					
(6)	DO pin control data  DOCC0 DOCC1 DOCC2	<ul style="list-style-type: none"> <li>Determines the output of the DO pin.</li> </ul> <table border="1" data-bbox="1317 938 1608 1252"> <thead> <tr> <th>DOCC2</th> <th>DOCC1</th> <th>DOCC0</th> <th>DO pin state</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Open</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Low when the unlocked state is detected</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>end-UC (See the section indicated with the asterisk (*) below)</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Open</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Open</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Open</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Low when stereo detected</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Open</td> </tr> </tbody> </table> <ul style="list-style-type: none"> <li>The open state is selected after the power on reset.</li> <li>Note: end-UC: The IF counter measurement complete check.</li> </ul>  <p data-bbox="1064 550 1176 1157">DO pin</p> <p data-bbox="1064 694 1086 813">① Count start</p> <p data-bbox="1064 901 1086 1021">② Count end</p> <p data-bbox="1064 1061 1086 1157">③ CE : HI</p> <p data-bbox="1153 1340 1198 1428">UL0, UL1 CTE</p> <p data-bbox="739 486 1030 1268">           (1) If the end-UC setting is used, the DO pin will automatically go to the open state when an IF count operation starts (CTE transitions from 0 to 1).            (2) When the IF counter measurement completes, the DO pin goes low and it becomes possible to check for the count completed state.            (3) The DO pin goes to the open state when serial data I/O is performed (when the CE pin is high).            Note: The DO pin goes to the open state during the data input period (IN1 and IN2 modes when CE is high), regardless of the values of the DO pin control data (DOCC0.2). During the data output period (OUT mode when CE is high), the DO pin outputs the content of the internal DO serial data in synchronization with the CL signal, regardless of the values of the DO pin control data (DOCC0.2).         </p>	DOCC2	DOCC1	DOCC0	DO pin state	0	0	0	Open	0	0	1	Low when the unlocked state is detected	0	1	0	end-UC (See the section indicated with the asterisk (*) below)	0	1	1	Open	1	0	0	Open	1	0	1	Open	1	1	0	Low when stereo detected	1	1	1	Open	UL0, UL1 CTE
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(7)	Unlock detection data  UL0, UL1	<ul style="list-style-type: none"> <li>Phase error (<math>\phi E</math>) detection width selection data used for PLL lock state discrimination. The unlocked state is recognized when a phase error in excess of the specified detection width occurs.</li> </ul> <table border="1" data-bbox="436 494 571 1252"> <thead> <tr> <th>UL1</th> <th>UL0</th> <th><math>\phi E</math> detection width</th> <th>Detection output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Stopped</td> <td>Open</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Directly outputs <math>\phi E</math></td> </tr> <tr> <td>1</td> <td>*</td> <td><math>\pm 6.67 \mu</math></td> <td>Extends <math>\phi E</math> by 1 to 2 ms</td> </tr> </tbody> </table> <p data-bbox="369 486 414 1268">Note: When the unlocked state is detected, the DO pin goes low and UL in the serial data output will be 0.</p>	UL1	UL0	$\phi E$ detection width	Detection output	0	0	Stopped	Open	0	1	0	Directly outputs $\phi E$	1	*	$\pm 6.67 \mu$	Extends $\phi E$ by 1 to 2 ms	DOCC0 DOCC1 DOCC2																				
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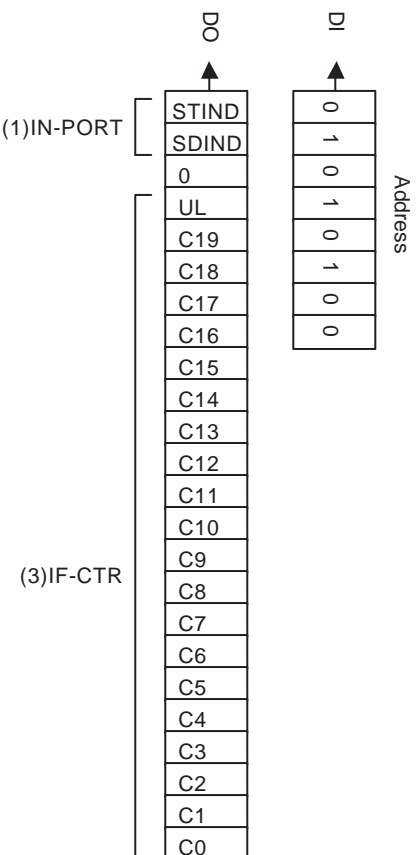
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No.	Control block/data	Description	Related data															
(8)	Phase comparator control data  DZ0, DZ1	<ul style="list-style-type: none"> <li>Controls the phase comparator dead band.</li> </ul> <table border="1" data-bbox="1706 496 1872 874"> <thead> <tr> <th>DZ1</th> <th>DZ0</th> <th>Dead band mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>DZA</td> </tr> <tr> <td>0</td> <td>1</td> <td>DZB</td> </tr> <tr> <td>1</td> <td>0</td> <td>DZC</td> </tr> <tr> <td>1</td> <td>1</td> <td>DZD</td> </tr> </tbody> </table> <p>Dead band widths: DZA &lt; DZB &lt; DZC &lt; DZD</p>	DZ1	DZ0	Dead band mode	0	0	DZA	0	1	DZB	1	0	DZC	1	1	DZD	
DZ1	DZ0	Dead band mode																
0	0	DZA																
0	1	DZB																
1	0	DZC																
1	1	DZD																
(9)	Output port data  <u>BO1</u> , <u>BO2</u>	<ul style="list-style-type: none"> <li>Sets the outputs from the <u>BO1</u> and <u>BO2</u> output ports. Data = 0: Open = 1: Low</li> </ul>																
(10)	Charge pump control data  DLC	<ul style="list-style-type: none"> <li>Forcibly controls the state of the charge pump output.</li> </ul> <table border="1" data-bbox="1364 496 1464 874"> <thead> <tr> <th>DLC</th> <th>Charge pump output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Normal operation</td> </tr> <tr> <td>1</td> <td>Forced to the low level.</td> </tr> </tbody> </table> <p>If deadlock occurs due to VCO oscillation when the VCO control voltage (V<sub>tune</sub>) is 0 V, the deadlock can be released by setting the charge pump output low and setting V<sub>tune</sub> to V<sub>CC</sub>. (This is referred to as a deadlock clear circuit.)</p>	DLC	Charge pump output	0	Normal operation	1	Forced to the low level.										
DLC	Charge pump output																	
0	Normal operation																	
1	Forced to the low level.																	
(11)	IFS	<ul style="list-style-type: none"> <li>This bit should normally be set to 1. However, setting this bit to 0 sets the device to degraded input sensitivity mode, and the input sensitivity is reduced by about 10 to 30 mV/rms.</li> </ul>																
(12)	IC test data  TEST0 to TEST2	<ul style="list-style-type: none"> <li>IC test data TEST0 TEST1 TEST2 All bits must be set to 0.</li> </ul> <p>All these bits are set to 0 after the power on reset.</p>																
(13)	DNC	<ul style="list-style-type: none"> <li>This bit must be set to 0.</li> </ul>																
(14)	Forced mono control data  STSW	<ul style="list-style-type: none"> <li>Determines the output of the STSW output port and controls the forced stereo function. Data = 0: Mono = 1: Stereo</li> </ul>																
(15) (16)	SD sensitivity adjustment data  SDC0 SDC1	<ul style="list-style-type: none"> <li>Determines the outputs of the SDC0 and SDC1 ports and sets the SD sensitivity.</li> </ul> <table border="1" data-bbox="535 496 701 874"> <thead> <tr> <th>SDC0</th> <th>SDC1</th> <th>SD sensitivity (typ)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>42 dB<math>\mu</math>V</td> </tr> <tr> <td>0</td> <td>1</td> <td>45 dB<math>\mu</math>V</td> </tr> <tr> <td>1</td> <td>0</td> <td>51 dB<math>\mu</math>V</td> </tr> <tr> <td>1</td> <td>1</td> <td>56 dB<math>\mu</math>V</td> </tr> </tbody> </table>	SDC0	SDC1	SD sensitivity (typ)	0	0	42 dB $\mu$ V	0	1	45 dB $\mu$ V	1	0	51 dB $\mu$ V	1	1	56 dB $\mu$ V	
SDC0	SDC1	SD sensitivity (typ)																
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**Structure of the DO Control Data (Serial Output Data)**

(1) OUT mode



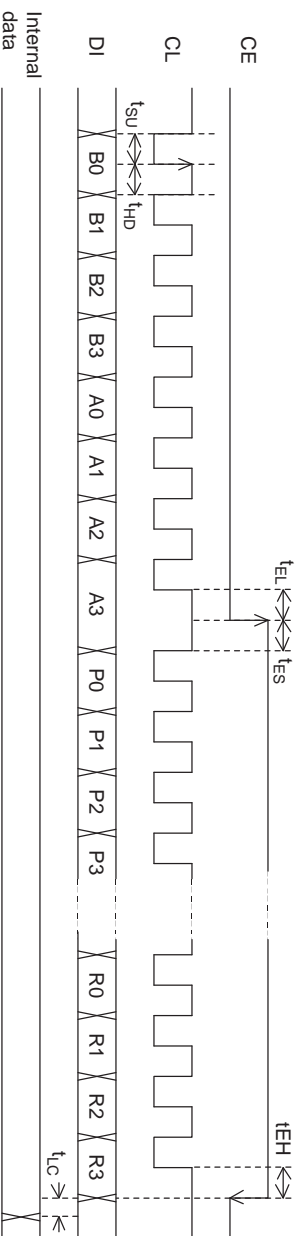
**DO Output Data**

No.	Control block/data	Description	Related data
(1)	Stereo indicator SD indicator Control data STIND, SDIND	<ul style="list-style-type: none"> <li>Indicates the states of the stereo and SD indicators at the point latched. The data is latched at the point the devices goes to data output mode (OUT mode). STIND ← Stereo indicator state: 0: ST on, 1: ST off SDINC ← SD indicator state: 0: SD on, 1: SD off</li> </ul>	
(2)	PLL unlocked data UL	<ul style="list-style-type: none"> <li>Indicates the state of the unlock detection circuit at the point latched. UL ← 0: Unlocked 1: Locked or detection stopped mode.</li> </ul>	UL0 UL1
(3)	IF counter Binary counter C19 to C0	<ul style="list-style-type: none"> <li>Indicates the content of the IF counter (20-bit binary counter) at the point latched. C19 ← MSB of the binary counter C0 ← LSB of the binary counter</li> </ul>	CTE GT0 GT1

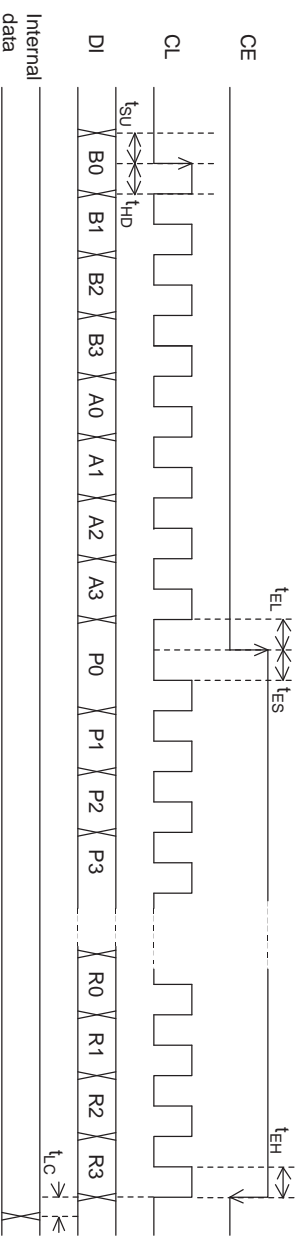


**Serial Data Input (IN1 / IN2)  $t_{SU}$ ,  $t_{HD}$ ,  $t_{EL}$ ,  $t_{ES}$ ,  $t_{EH} \geq 0.75\mu s$ ,  $t_{LC} < 0.75\mu s$**

(1) CL: Normally high

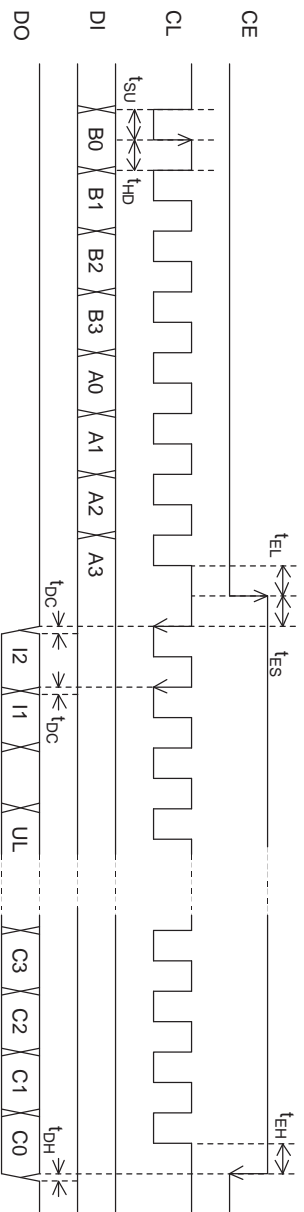


(2) CL: Normally low

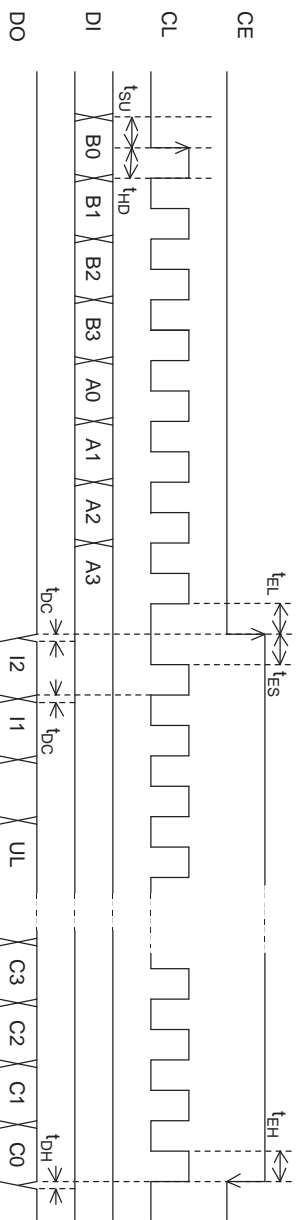


**Serial Data Output (OUT)  $t_{SU}$ ,  $t_{HD}$ ,  $t_{EL}$ ,  $t_{ES}$ ,  $t_{EH} \geq 0.75\mu s$ ,  $t_{DC}$ ,  $t_{DH} < 0.35\mu s$**

(1) CL: Normally high

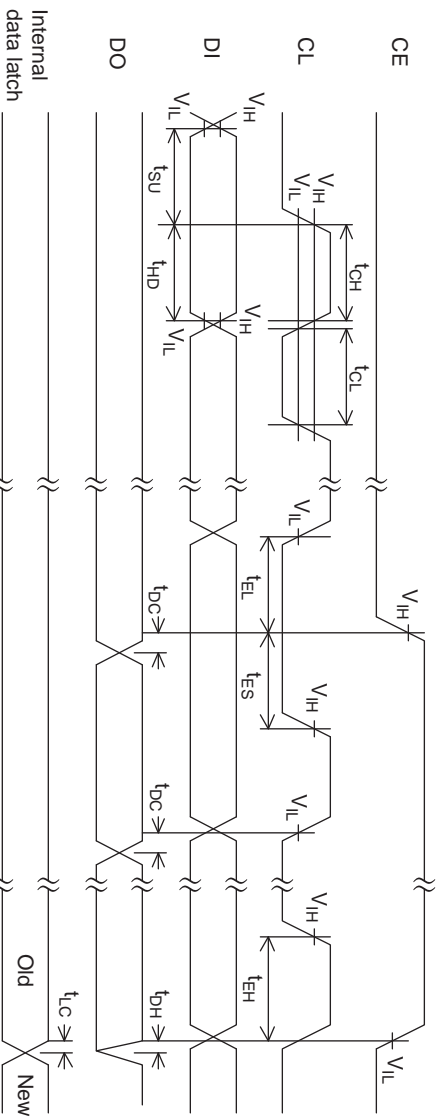


(2) CL: Normally low

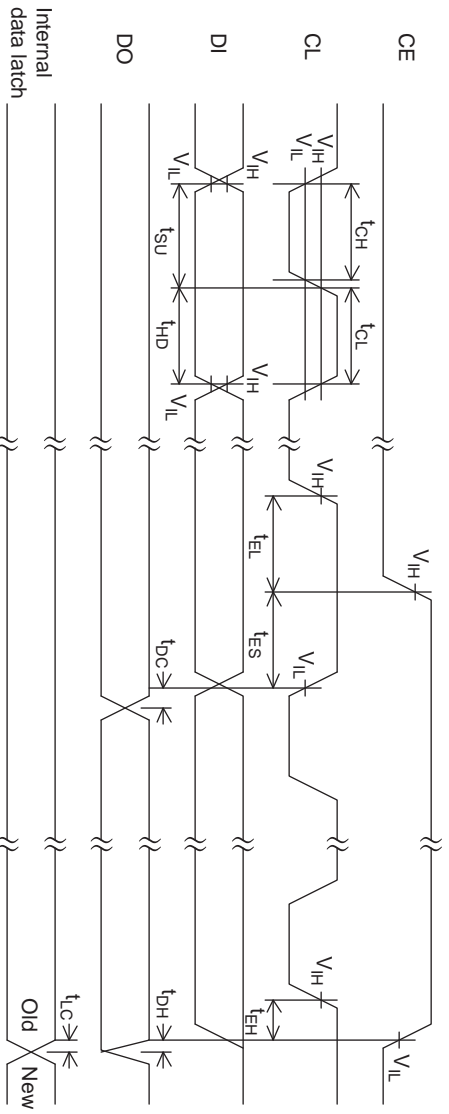


Note: Since the DO pin is an n-channel open-drain output, the data transition times ( $t_{DC}$  and  $t_{DH}$ ) depend on the value of the pull-up resistor and the printed circuit board capacitance.

Serial Data Timing

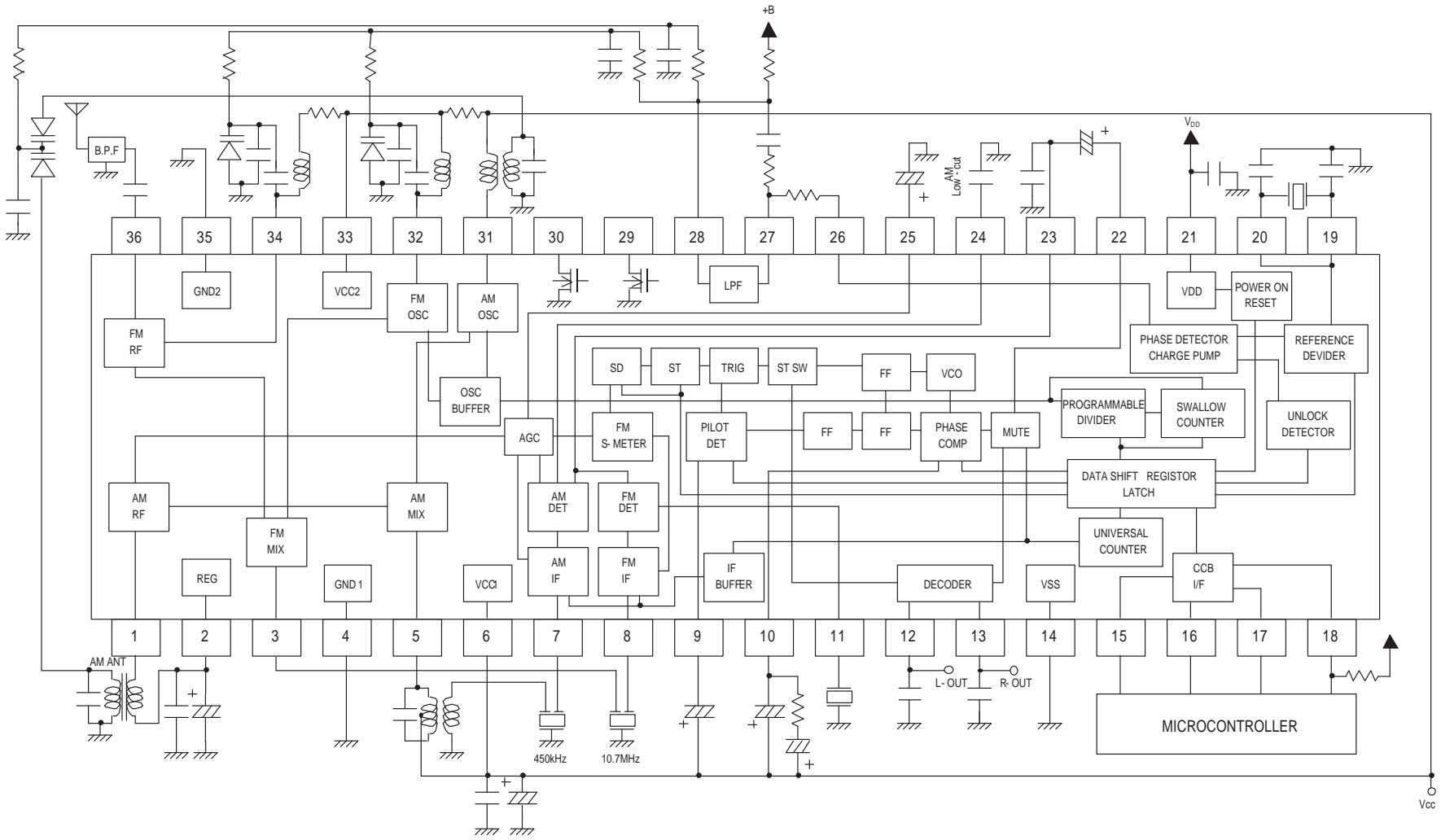


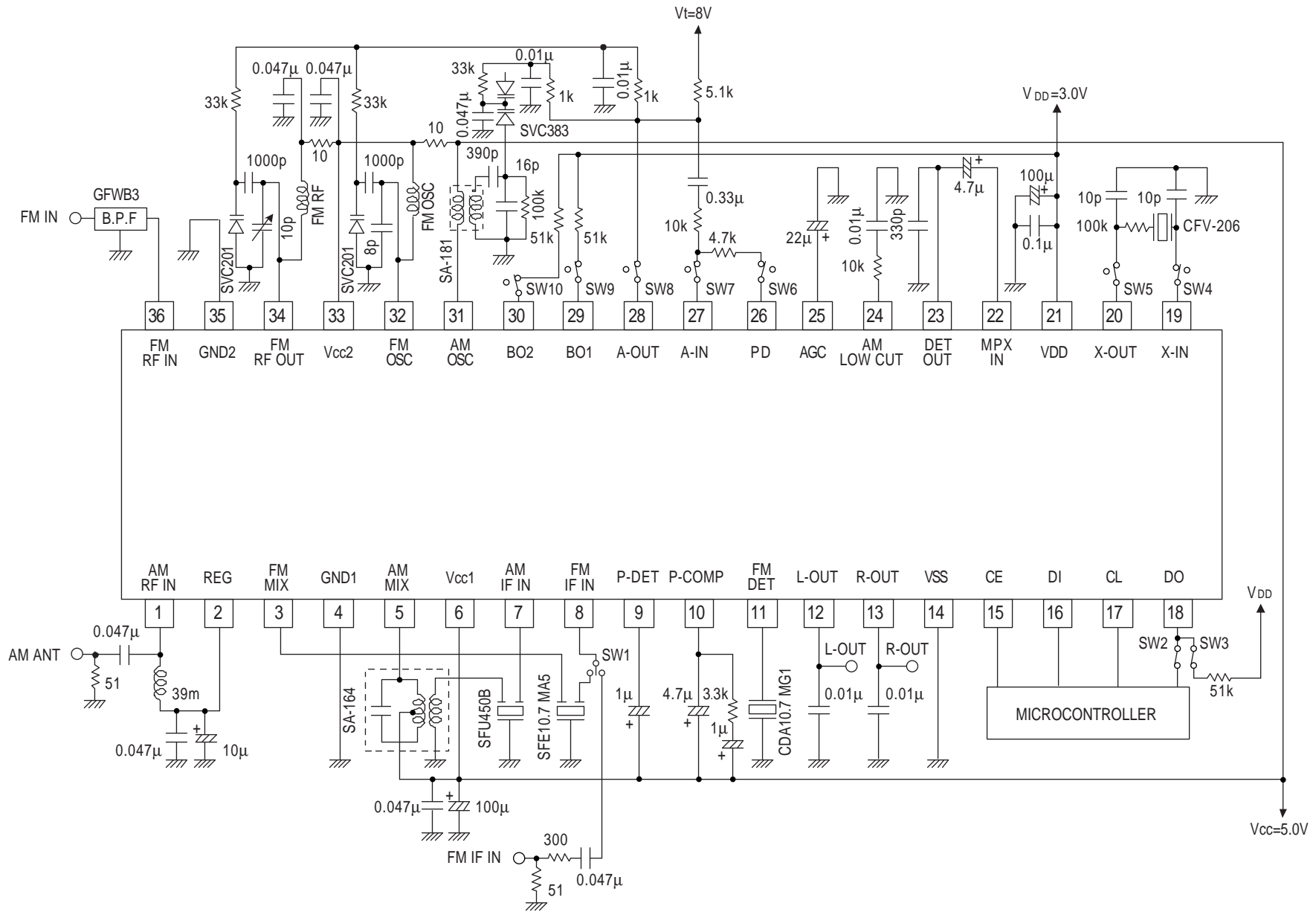
<<When CL Stops at the Low Level>>

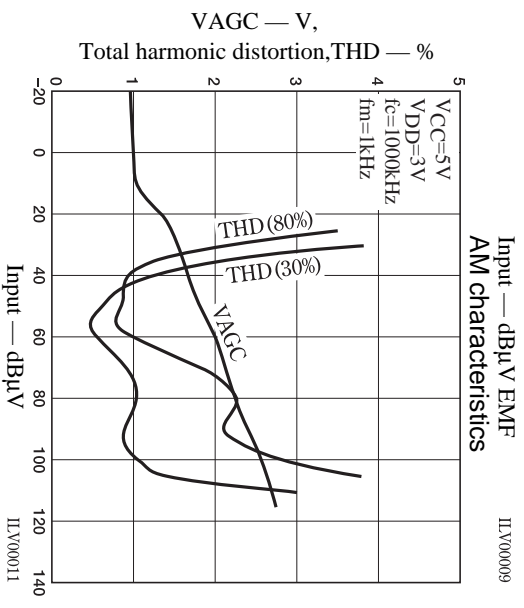
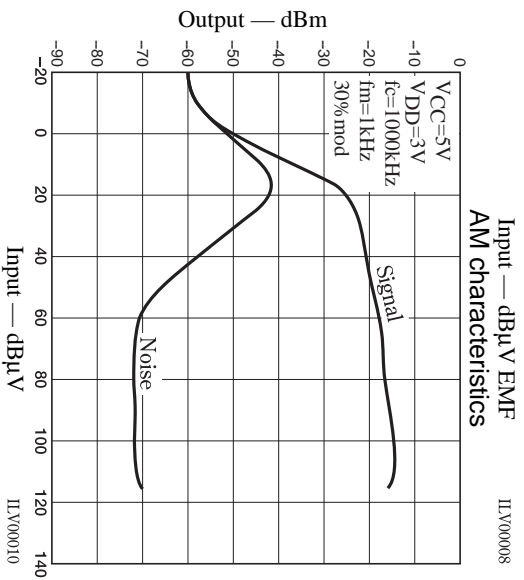
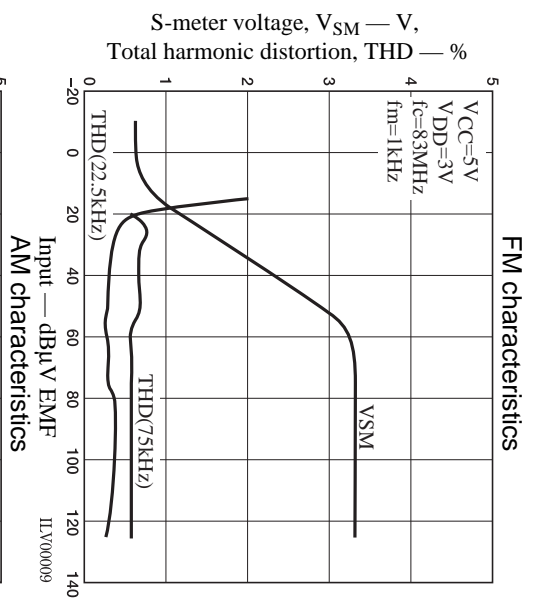
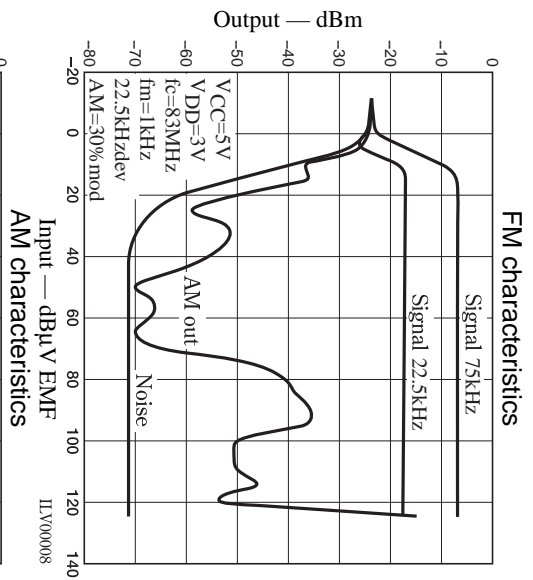


<<When CL Stops at the High Level>>

Parameter	Symbol	Pins	Conditions	Ratings			Unit
				min	typ	max	
Data setup time	$t_{SU}$	DI, CL		0.75			$\mu s$
Data hold time	$t_{HD}$	DI, CL		0.75			$\mu s$
Clock low-level time	$t_{CL}$	CL		0.75			$\mu s$
Clock high-level time	$t_{CH}$	CL		0.75			$\mu s$
CE wait time	$t_{EL}$	CE, CL		0.75			$\mu s$
CE setup time	$t_{ES}$	CE, CL		0.75			$\mu s$
CE hold time	$t_{EH}$	CE, CL		0.75			$\mu s$
Data latch transition time	$t_{LC}$					0.75	$\mu s$
Data output time	$t_{DC}$	DO, CL	These times depend on the value of the pull-up resistors and the printed circuit board capacitances.				$\mu s$
	$t_{DH}$	DO, CE				0.35	







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